International
IOR Rectifier

ADVANCE INFORMATION **Data Sheet No. PD60164A**

IR1110

SOFT START CONTROLLER IC

Features

- Self-contained soft charging of DC bus capacitor
- DC bus voltage regulation
- 3-phase or 1-phase AC input
- Applicable to 115/230/380/460/575V AC input
- Drives SCR phase controlled half bridge
- Programmable ramp rate
- Protection against DC bus short circuit
- Fast power dip ride through with automatic ramp back
- Selectable shutdown on single phase loss
- 1-phase and 3-phase loss fault output
- Insensitive to phase rotation
- High line or low line fault output
- Low power consumption
- Integrated watchdog function for each phase
- 64-pin MQFP package

Description

The IR1110 is a high performance analog IC designed to control ramp rate and voltage of the DC bus from either single or three phase AC line voltage input. It controls a SCR half bridge and provides robust ride through capability in event of transient loss of line, and DC bus regulation with eternal reference input. Comprehensive line status fault output including 1/3 phase loss and high or low line fault provides versatile line diagnostic capability to the system. The IR1110 is based on advanced low power design so it can utilize the SCR snubber derived power supply.

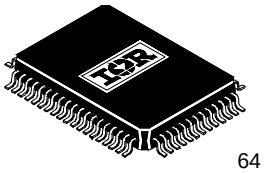
Product Summary

V_{DDS}/V_{SS}	+/- 5V
I_{SS}/I_{DD}	+/- 5mA
DC bus registration response time	100msec (typ.)
Min. DC bus regulation voltage with capacitive load	35% of V_{DCMAX}
Programmable DC bus ramp time	100msec to 330msec (typ.)

Typical Application

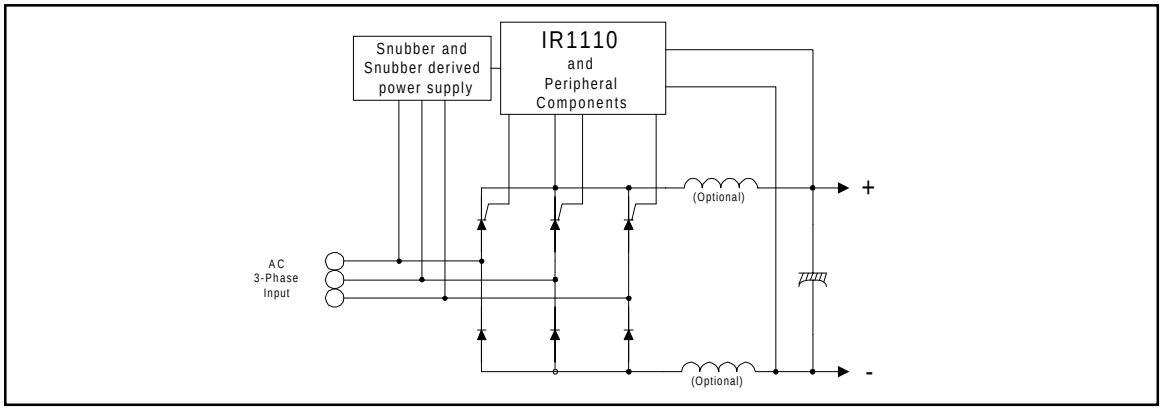
- Motor drives
- Welders
- Battery chargers
- Power supplies

Package



64 Lead MQFP

System Block Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to AGND and DGND, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_{DD}	Positive supply voltage	—	6.0	V
V_{SS}	Negative supply voltage	—	-6.0	
V_{IN}	Operating input voltage range on UIN,VIN & WIN pins	(V_{SS} + 0.4)	(V_{DD} - 0.4)	
V_{BIN}	Operating input voltage on VBOS and VBNEG	- 4.5	3.0	
V_{LED}	Operating input voltage on 1PHLED, LNLED, and LNLSLED pins	—	V_{DD}	
V_{LNSET}	Operating input voltage on LNSET	—	(V_{DD} - 0.4)	
I_{LED}	Sinking current on 1PHLED, LNLED, and LNLSLED pins	—	3	mA
Rth_{JA}	Thermal resistance, junction to ambient	—	60	°C/W
T_A	Operating ambient temperature	-40	85	°C
T_J	Junction temperature	—	150	
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Component Values

All capacitors are rated 6.3V unless otherwise specified. All resistors are rated 1/16W unless otherwise specified. The typical connection diagram is shown in figure 3. For proper operation the device should be used with the recommended components specified below.

Symbol	Definition	Typ.	Tolerance	Units	Comments
Q_U Q_V Q_W	Phase U/V/W complementary MOSFET	IRF7509			Complementary NMOS/PMOS Driver
R_{U1} R_{V1} R_{W1}	Resistor divider for input voltage	3.4 X VACrms max	1% .25W	kΩ	Note 1
R_B	Bias resistor	249k	1%	Ω	
R_{U2} R_{V2} R_{W2}	Resistor divider for input voltage	9.09k	1%		
R_{ERR}	DC bus regulation error resistor	2M	5%		
R_{CLAMP1}	Ramp clamp resistor 1	430k	5%		
R_{CLAMP2}	Ramp clamp resistor 2	100k	5%		
R_{RAMP}	Ramp resistor	82k	5%		

Recommended Operating Conditions cont.

All capacitors are rated 6.3V unless otherwise specified. All resistors are rated 1/16W unless otherwise specified. The typical connection diagram is shown in figure 3. For proper operation the device should be used with the recommended components specified below.

Symbol	Definition	Typ.	Tolerance	Units	Comments
R_{PKLL1}	Line voltage peak holding resistor 1	2.2M	5%		
R_{PKLL2}	Line voltage peak holding resistor 2	6.8M	5%	Ω	
R_{DIP1}	Voltage dip resistor 1	332k	1%		
R_{DIP2}	Voltage dip resistor 2	1.0M	1%		
R_{DFIL}	Voltage dip filter resistor	15k	5%		
R_{PKD}	Timing wave peak voltage discharge resistor	1M	5%		
R_{PKFIL}	Timing wave peak voltage filter resistor	56k	5%		
R_{POS1} R_{NEG1}	Resistor divider for DC bus voltage input	3.2 X VACrmsmax	1% .5W	kΩ	Note 1,2
R_{POS2}	Feedback resistor for DC bus voltage Amp	9.09k	1%		
R_{NEG2}	Resistor divider for DC bus voltage	9.09k	1%		
R_{WDU} R_{WDV} R_{WDW}	Phase U/V/W watchdog resistor	845k	1%		Note 3
R_{LS1}	Line fault output reference divider resistor 1	357k	1%		
R_{LS2}	Line fault output reference divider resistor 2	78.7k	1%		
R_{SG1}	SCR firing anode voltage reference resistor 1	0.82k X VACrmsmax	1%		Note 4
R_{SG2}	SCR firing anode voltage reference resistor 2	10k	1%		
R_{INTU} R_{INTV} R_{INTW}	Phase U/V/W integrator resistor	1M	1%	Ω	
R_{INTRU} R_{INTRV} R_{INTRW}	Phase U/V/W integrator reset resistor	33.2k	1%		
R_{LED1}	LNLSLED pin resistor for opto interface	6.2k	5%		
R_{LED2}	LNLED pin resistor for opto interface	6.2k	5%		
R_U, R_V, R_W	Phase U/V/W SCR driver pull-up resistor	5.6k	5%		
R_{GU} R_{GV} R_{GW}	Phase U/V/W SCR driver output resistor	33	5% .25W		
R_{DU} R_{DV} R_{DW}	Phase U/V/W SCR driver filter resistor	470	5% .		

Recommended Operating Conditions cont.

All capacitors are rated 6.3V unless otherwise specified. All resistors are rated 1/16W unless otherwise specified. The typical connection diagram is shown in figure 3. For proper operation the device should be used with the recommended componens specified below.

Symbol	Definition	Typ.	Tolerance	Units	Comments
C_{UVLO}	Capacitor on UVLOCAP pin	.1	5%		
C_{1PH}	Capacitor on 1PHCAP pin	.001	5%		
C_{3PH}	Capacitor on 3PHCAP pin	.022	5%		
C_{ERR}	Capacitor on DCREGC pin	.22	10%	µF	
C_{RAMP}	Capacitor on CRAMP pin	1.0	10%		
C_{PKLL}	Capacitor on VPKLL pin	.1	10%		
C_{BDIP1}	Capacitor on BDIP1	3300	5%		
C_{BDIP2}	Capacitor on BDIP2	1000	5%	PF	
C_{HOLD}	Capacitor on BDIPHLD	.33	10%		
C_{PK}	Capacitor on VPK	.33	10%		
C_{WDU} C_{WDV} C_{WDW}	Capacitor on WDCAPU, WDCAPV, and WDCAPW	.027	2%	µF	
C_{INTU} C_{INTV} C_{INTW}	Capacitor between CINTU/V/W and INTNU/V/W	.0082	2%		
C_U, C_V, C_W	Capacitor in SCR driver circuit	.0047/25V	10%		
D_{RAMP}	Diode in series with RRAMP	IN4148			
Opto1,Opto2	Fault output opto couplers	HCPL0701			

Note 1) Power rating is based on 550VAC rms maximum. For lower AC line voltage, power can be reduced proportionally. Vac rms max = Maximum operating RMS value of AC line voltage. Use the nearest standard 1% value to calculated value. Resistor must be rated for peak line voltage.
Note 2) R_{POS2} is not required if no series inductor(s) in place on positive DC bus. Resistor must be rated for peak line voltage.
Note 3) V_{DD} = 5.0V±2.5%. If 5.1V±2% zener diode sets V_{DD}, use 866k 1%.
Note 4) With these values LNLED is used for low line detection and is low at line voltage greater than approximately 57% of Vacrms maximum voltage.
Note 5) Use the nearest standard 1% value to calculated value.
Note 6) C_{RAMP} and R_{RAMP} sets the bus voltage ranp-up time. Minimum value of C_{RAMP} is 0.68µF, maximum value is 3.3µF. See Operation Description - Ramp Circuit.

Special Mode of Operation

1. Dedicated single phase operation

For operation with a one-phase bridge, connect 1PHSEL (pin12) to V_{SS}. Use the U and V inputs. Connect WIN (pin3) to ground. Use the SCRU (pin47) and SCRV (pin46) outputs. Use R_{PKD} = 3.0MΩ, R_{WDU}, R_{WDV} = 1.0MΩ , CINTU,CINTV = 0.0068υF 2%.
The following components can be omitted: R_{W1}, R_{W2}, R_{WDW}, C_{WDW}, R_{INTW}, R_{INTRW}, C_{INTW}.

2. Operation without DC bus voltage regulation

For operation without bus voltage, ie. maximum DC bus voltage only, connect VBREF (pin8) to VSS. RERR and CERR can be omitted. Connect DCREGC (pin10) to ground.

DC Electrical Characteristics

R_{BIAS} = 249K/1%, V_{DD} = 5.1V, V_{SS} = 5.1V and T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{DD}	Positive Supply Voltage	4.8	5.1	5.6	V	Note 3
V_{SS}	Negative Supply Voltage	-4.8	-5.1	-5.6		Note 3
I_{DD}	V_{DD} Supply Current	—-	3.0	6.0	mA	Note 4
I_{SS}	V_{SS} Supply Current	—-	-3.0	-5.0		Note 4
V_{IN}	Input Voltage Range for UIN, VIN, and WIN	1.5	—-	4.0		
V_{BREF}	Input Voltage Range for VBREF	0	—-	5.0		Note 1
V_{IL1}	Input logic low voltage on 1PHEN, LNLSSL	—-	—-	-2.0	V	
V_{IH1}	Input logic high voltage on 1PHEN, LNLSSL	2.2	—-	—-		
V_{PCINT}	Positive Output Voltage Swing at CINTU, CINTV, and CINTW Pins	—-	4.0	4.5		Peak voltage of Vin = 4.0V
V_{PCR+}	Positive Output Voltage Swing at CRAMP Pin	—-	4.0	4.5		
V_{PCR-}	Negative Output Voltage Swing at CRAMP Pin	0	—-	—-		
$I_{1PHCAP+}$	Sourcing Current at 1PHCAP pin	—-	2.0	—-	µA	1PHCAP=VSS
$I_{1PHCAP-}$	Sinking Current at 1PHCAP pin	—-	5.0	—-		1PHCAP=GND
$I_{3PHCAP+}$	Sourcing Current at 3PHCAP pin	—-	3.0	—-		3PHCAP=VSS
$I_{3PHCAP-}$	Sinking Current at 3PHCAP pin	—-	15.0	—-		3PHCAP=GND
VOL_{LED}	Output Low Voltage at 1PHLED, LNLSLED, and LNLED pins	0	0.12	.4	V	Output sinking current = 3.0mA
VOH_{LED}	Output High Voltage at 1PHLED, LNLSLED, and LNLSLED pin	V_{DD} 0.4	—-	V_{DD}		Output sourcing current = 3mA
UVLO	Undervoltage lockout between VDD-GND	4.1	4.4	4.6		
I_{UVLO+}	Sinking Current at UVLOCAP pin	60	86	110	uA	VUVLOCAP=VDD
VHSCR	Output Voltage at High level at SCRU, SCRV, and SCRW pins	—-	4.5	—-	V	I_O = 1mA
VLSCR	Output Voltage at Low level at SCRU, SCRV, and SCRW pins	—-	0.1	0.31		I_O = -1mA
VRAMPBUF	Output Voltage at VRAMP pin	—-	4.0	—-		
RVBREF	Input Resistance On VBREF pin	—-	400	—-	kΩ	
$I_{BDIPCAP}$	Sourcing Current of BDIPCAP pin	—-	5	—-	uA	BDIPCAP=VSS
$V_{tLNLED+}$	Peak threshold voltage on UIN/VIN/WIN pins for LNLED to switch low	2.2	2.3	2.4		VLNSET = 1.0V
$V_{tLNLED-}$	Peak threshold voltage on UIN/VIN/WIN pins for LNLED to switch high	2.0	2.1	2.2	V	Note 2
V_{tLNLS}	Peak threshold voltage on UIN/VIN/WIN pins for LNLSLED to stay low	—-	.5	—-		All input voltages present
V_{t1PH}	Peak threshold voltage on UIN/VIN/WIN pins for 1PHLED to stay low	—-	.5	—-		All input voltages present

See notes on page 6

Notes for DC Electrical Characteristics

Note 1) VBREF=5.0V will assure full SCR firing on to produce the maximum amount of DC bus voltage and faster convergence to the maximum DC bus voltage. Although VBREF=4.0V corresponds to the maximum voltage, it will take longer time to converge to the maximum DC bus voltage.
Note 2) These voltage values are linearly proportional to VLNSET. For example, if VLNSET = 2.0V, then all values are twice of those values listed in the table.
Note 3) VDD must be regulated within ±2.5%. VSS must be regulated within ±5%.

AC Electrical Characteristics

V_{DD} = 5.1V, $V_{SS,}$ = 5.1V, CL = 1000pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_r	Turn-on rise time on SCRU, SCRV, and SCRW	—-	500	—-	ns	
t_f	Turn-off fall time on SCRU, SCRV, and SCRW	—-	500	—-		
t_{WSCR}	Output pulse width of SCRU,SCRV, and SCRW	—-	15	—-	µs	
t_{DLL}	LNLSLED propagation delay	—-	30	—-		LNLSSL=VDD, C3PH =.022uF, (note 1)
t_{D1PH}	1PHLED propagation delay	—-	8.3	—-	ms	C1PH = .001uF
t_{LN}	LNLED propagation delay	—-	150	—-		(note 2)
t_{S1PH}	Shutdown time after loss of single phase	—-	15	20	ms	1PHEN = VDD,
						CUVLO = .1mF, C1PH = .001mF, (note 3)
t_{fFO}	Fall time from high to low on LNLSLED, 1PHLED, LNLED	—-	50	—-	ns	Pull-up resistor = 6.2kW
tW1PH	1PHLED pulse width	—-	2	—-		C1PH =.001mF, (note 4)
t_{UVLCK}	Power up UVLOCK delay		60		msec	CUVLCK=.1uF, (note 5)
tRAMP	DC bus ramp time		150			CRAMP=1uF, RRAMP=82k,(note 6)
V_{ENSCR}	Minimum input voltage on UIN, VIN, and WIN for enabling SCR firing	—-	R_{U2}/R_{U1} X 12	—-	V	(note 7)
P_{PUBAL}	Phase-to-phase unbalance between pulses on SCRU, SCRV, and SCRW	—-	±1.5	—-	°	Firing angle = 90° Notes 8 and 9
		—-	±3	—-		Firing angle = 140° Note 9

See Notes on page 7

Notes for AC Electrical Characteristics

Note 1) Delay is proportional to the capacitor values with minimum allowed value of C_{3PH} = .01µF
Note 2) Depends on C_{PKLL} charge condition
Note 3) C_{UVLO} = .1µF, C_{1PH} = .001µF. Increasing C_{UVLO} increases the delay/response time of the 1phase lockout.
Note 4) Pulse width is proportional to C1PH. Maximum allowed values of C_{1PH} is .001µF.
Note 5) Power up delay is set by C_{UVLO} or by V_{DD} rise time whichever takes longer. In this condition, V_{DD} rise time must not be less than 100msec, and 1-phase shutdown must be enabled. If this is less than 100msec or 1-phase shut down is disabled, C_{UVLO} must be increased to 0.22µF in order to increase the undervoltage lockout time to greater than 100msec. See Note 3) above on additional effect of increasing C_{UVLO}.
Note 6) Ramp time is proportional to the capacitor value.
Note 7) This value corresponds approximately to 15V minimum SCR firing voltage. For 15V minimum SCR firing voltage, (R_{SG2}/R_{SG1}) X V_{DD} = (R_{U2}/R_{U1}) X 15.
Note 8) PPUBAL applies to steady operation, is deviation of any firing point to closest balanced set of firing points.
Note 9) Firing angle is defined with respect to zero delay (ie. max output voltage.

System Operating Characteristics and Specifications

All peripheral component values are those listed in the recommended operating condition unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{AC}	Line-to-line AC voltage range (1%)	80	120	140		R_{u1},R_{v1},R_{w1}=475K R_{POS1},R_{NEG1}=453K
		161	230	276	V_{RMS}	R_{u1},R_{v1},R_{w1}9537K R_{POS1},R_{NEG1}=887K
		322	460	552		R_{u1},R_{v1},R_{w1}=2X953K R_{POS1},R_{NEG1}=887K
f_{LINE}	Input line frequency	47	50/60	63	Hz	
V_{BRANGE}	DC bus voltage controllable range	35	—-	99.8	%	V_{BREF}=1.4V to 4V
V_{BREG}	DC bus voltage regulation	—-	2	—-	%	
V_{BRES}	DC bus voltage step response time	—-	100	—-	msec	V_{BUS}=35% to 100% Note 6
t_{RAMP1}	DC bus voltage ramp up time at power up	—	150	—-	msec	C_{RAMP} = 1µF R_{RAMP} = 82k (Note 7)
t_{RAMP2}	DC bus voltage ramp up time at power dip ride through	—-	75	—-	msec	C_{RAMP} = 1µF R_{RAMP} = 82k (Note 7)
t_{dPWR}	Power up delay time before ramp up	—-	190	—-	msec	C_{RAMP} = 1µF C_{UVLO} = 0.1µF Note 9)
t_{dDIP1}	Delay time to start ramp-up after recovery from a transient loss of line voltage		15		msec	Voltage drop below the reference voltage at B_{DIP2} pin
a_{FIRE}	Firing angle range	1.5	—-	160	°	Figure 2, Note 14
t_{d1PHS}	Delay time to shutdown SCR firing pulses after loss of one phase input	15	—-	30	msec	1PHEN = V_{DD}
t_{d1PHE}	Delay time to start ramp-up after recovery from a loss of one phase input	—-	30	—-	msec	1PHEN = V_{DD}

System Operating Characteristics and Specifications

All peripheral component values are those listed in the recommended operating condition unless otherwise specified.

t_{d1FIRE}	First SCR firing angle at ramp-up	—	20	32	°	CRAMP=1µF, R_{RAMP} = 82k (Note 10)
			16	25	°	CRAMP=2.2µF, R_{RAMP} = 47k (Note 10)
			14	22	°	CRAMP=3.3µF, R_{RAMP} = 30k (Notes10,12, 13)
$RLIM_{FIRE}$	Rate of advance of firing angle from last max firing angle during ramp-up	—-	10	20°		CRAMP = 1µF, R_{RAMP} = 82k
			7	14		CRAMP=3.3µF, R_{RAMP} = 30k (Notes 11 and 13)

Notes for System Operating Characteristics

Note 6) Step change of V_{BREF} may result in excessive bus capacitor charging current. Rate of change of V_{BREF} should be decreased in order to limit bus capacitor charging current for practical application.

Note 7) Time to ramp up to 99.8% DC bus level at a power up. It does not include the power up delay time. The practical limitation of the minimum time (50msec) depends on the inrush current to the DC bus capacitor. Ramp time is proportional to C_{RAMP}.

Note 8) Time to ramp back to 99.8% DC bus level from 50% DC bus level at a momentary power dip. This does not include the delay time to start ramp-up (t_{DDIP})

Note 9) The value depends on C_{UVLCK}

Note 10) The value depends on C_{RAMP}, R_{PK}, R_{RAMP}

Note 11) The value depends on C_{RAMP}

Note 12) See operation description - Ramp Circuit

Note 13) Firing angle defined with respect to fully off (zero output voltage) firing angle.

Note 14) Firing angle defined with respect to zero delay.

Operating Mode/Fault Output Matrix Chart

Mode	Fault condition	Fault output indicator	Description	External setting
3-phase Input operation	Normal	Non-multiplexed	SCR output firing active. LNLSLED = low, 1PHLED = high	LNLSSL = VDD 1PHEN = VDD or VSS 1PHSEL = VDD
		Multiplexed	SCR output firing active. LNLSLED = low, 1PHLED = high	LNLSSL = VSS 1PHEN =VDD or VSS 1PHSEL = VDD
	3-phase loss	Non-multiplexed	SCR output firing disabled for period of loss. LNLSLED = high, 1PHLED = high	LNLSSL = VDD 1PHEN =VDD or VSS 1PHSEL = VDD
		Multiplexed	SCR output firing disabled for period of loss. LNLSLED = high, 1PHLED = high (Note 1)	LNLSSL = VSS 1PHEN =VDD or VSS 1PHSEL = VDD
	1-phase loss without shutdown	Non-multiplexed	SCR output firing active. LNLSLED = low, 1PHLED = toggles low for 2msec once or twice per line cycle	LNLSSL = VDD 1PHEN = VSS 1PHSEL = VDD
		Multiplexed	SCR output firing active.LNLSLED toggles high while 1PHLED toggles low for 2msec once or twice per line cycle. (Note 2)	LNLSSL = VSS 1PHEN = VSS 1PHSEL = VDD
	1-phase loss with shutdown	Non-multiplexed	SCR output firing disabled for period of loss. LNLSLED = low, 1PHLED = toggles low for 2msec once or twice per line cycle	LNLSSL = VDD 1PHEN = VDD 1PHSEL = VDD
		Multiplexed	SCR output firing disabled for period of loss. LNLSLED toggles high while 1PHLED toggles low for 2msec once or twice per line cycle. (Note 2)	LNLSSL = VSS 1PHEN = VDD 1PHSEL = VDD
	High/Low AC line	LNLED	If line voltage exceeds the specified level on LNSET voltage, then LNLED = low. Otherwise LNLED = high	LNSET=desired voltage, 1PHEN =VDD or VSS 1PHSEL = VDD
1-phase input operation	1-phase loss	Non-multiplexed	SCR output firing disabled for period of loss. LNLSLED = high, 1PHLED = high	LNLSSL = VDD 1PHEN =VDD or VSS 1PHSEL = VSS
		Multiplexed	SCR output firing disabled for period of loss. LNLSLED = high, 1PHLED = high	LNLSSL = VSS 1PHEN =VDD or VSS 1PHSEL = VSS
	Normal	Non-multiplexed	SCR output firing active. LNLSLED = low. 1PHLED toggles low for 2msec once or twice per line cycle	LNLSSL = VDD 1PHEN =VDD or VSS 1PHSEL = VSS
		Multiplexed	SCR output firing active. LNLSLED toggles high while 1PHLED toggles low for 2msec once or twice per line cycle. (N ote 2)	LNLSSL = VSS 1PHEN =VDD or VSS 1PHSEL = VSS
	High/Low AC line	LNLED	If line voltage exceeds the specified level on LNSET voltage, then LNLED = low. Otherwise LNLED = high	LNSET=desired voltage, 1PHSEL= VSS 1PHEN =VDD or VSS

Note 1) LNLSLED may toggle high once for 2msec after event of phase loss.

Note 2) 1PHLED and LNLSLED are completely synchronized and complementary.

Functional Block Diagram

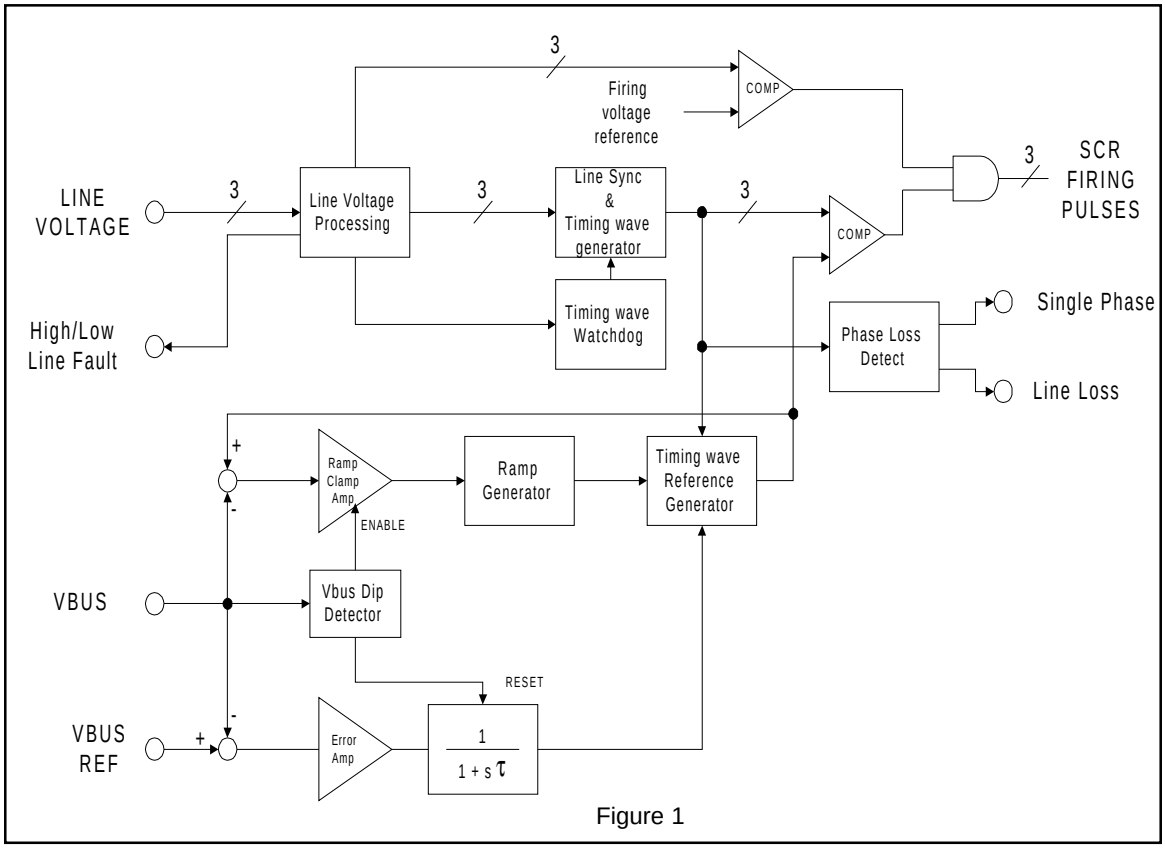
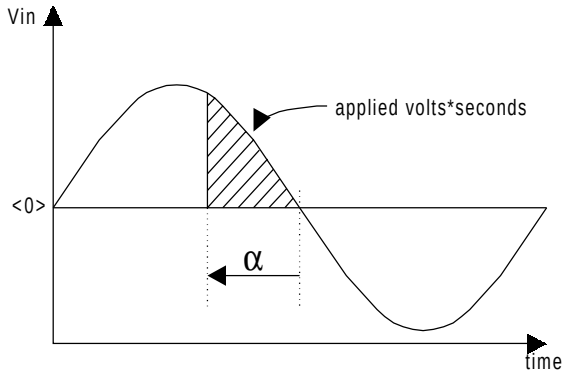


Figure 1

Firing Angle, *a*

Figure 2



Typical Connection Diagram

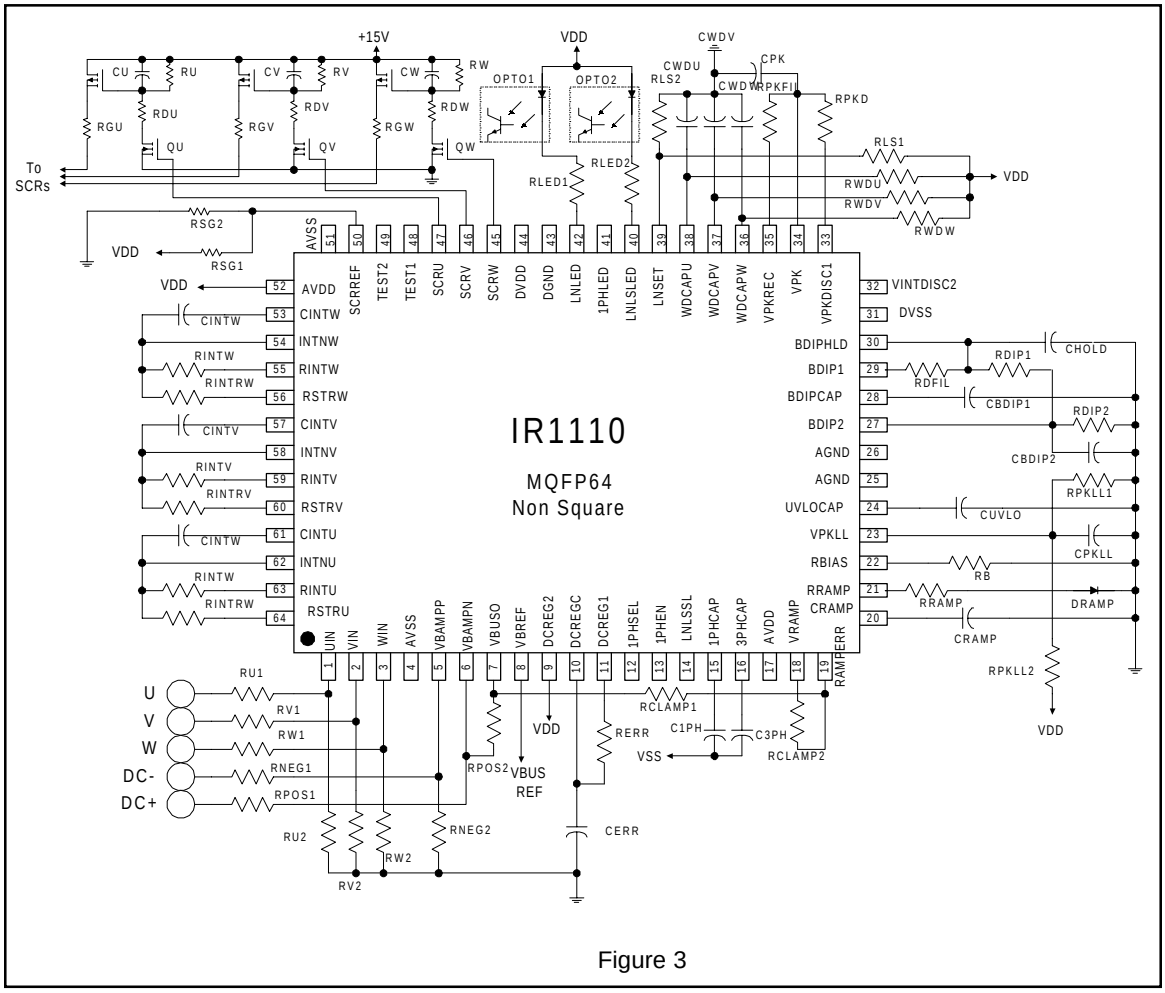


Figure 3

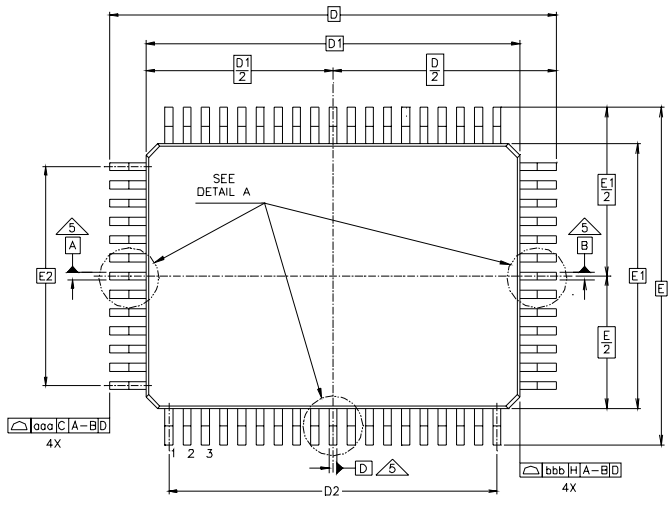
Lead Definitions

Symbol	Pin #	Description
DVDD	44	Logic positive supply voltage.
DGND	43	Logic ground
DVSS	31	Logic negative supply voltage
AVDD	17	Analog positive supply voltage
AGND	25,26,43	Analog ground
AVSS	4,31,51	Analog negative supply voltage
UIN/VIN/WIN	1,2,3	Phase U/V/W voltage inputs
VBAMPP	5	DC bus OP Amp. positive input, connect to DC bus(-) via resistor
VBAMPN	6	DC bus OP Amp. negative input, connect to DC bus (+) via resistor
VBUSO	7	DC bus OP Amp. output
VBREF	8	DC bus regulation voltage reference input
DCREG2	9	DC bus error amplifier output via series diode
DCREG1	11	DC bus error amplifier output
DCREGC	10	DC bus error compensation (External capacitor connection pin)
1PHSEL	12	Single phase input mode select. Note 1) on page 12
1PHEN	13	Single phase shutdown mode enable. Note 2) on page 12
LNLSSL	14	Phase loss Fault Output Select. Note 3) on page 12
1PHCAP	15	Single phase loss detect timing capacitor
3PHCAP	16	Three phase loss detect timing capacitor
VRAMP	18	Buffered voltage ramp circuit output
RAMPERR	19	Ramp error amplifier input
CRAMP	20	Ramp timing capacitor
RRAMP	21	Ramp timing resistor
RBIAS	22	Bias current resistor
VPKLL	23	Line-to-line peak voltage holding capacitor
UVLOCAP	24	Under voltage lockout delay capacitor
BDIP1	29	DC bus voltage dip detection 1
BDIP2	27	DC bus voltage dip detection 2
BDIPHLD	30	DC bus voltage dip hold capacitor
BDIPCAP	28	DC bus voltage dip timing capacitor
VPKDISC1	33	Line synchronization timing wave peak voltage discharging resistor
VPKDISC2	32	No connection
VPK	34	Line synchronization timing wave peak voltage
VPKREC	35	Line synchronization timing waveform
WDCAPU/V/W	38,37,36	Watchdog timing capacitor for phase U, V, and W
LNSET	39	Line voltage comparator reference input
LNLSLED	40	Line Loss Fault Output
1PHLED	41	Single Phase Loss Fault Output
LNLED	42	High/Low line status Output
CINTU/V/W	61,57,53	Phase U/V/W integral amplifier output
INTNU/V/W	62,58,54	Phase U/V/W integral amplifier negative input
RINTU/V/W	63,59,55	Phase U/V/W integral amplifier resistor connection
RSTRU/V/W	64,60,56	Phase U/V/W integral discharge resistor
SCRU/V/W	47,46,45	Phase U/V/W SCR gate signal
TEST1	48	Test purpose pin (Should be tied to VDD)
TEST2	49	Test purpose pin (No connection should be made)
SCRREF	50	SCR gate signal reference

Lead Definitions

Note 1) 1PHSEL = VDD for 3 phase operation, 1PHSEL = VSS for 1 phase operation. See Operating Mode/Fault Output Matrix Chart for the detail.
Note 2) 1PHEN = VDD for enable, 1PHEN = VSS for disable. See Operating Mode/Fault Output Matrix Chart for the detail.
Note 3) LNLSSL = VDD for total line loss only, LNLSSL = VSS for multiplexing total line loss/1 phase loss. See Operating Mode/Fault Output Matrix Chart for the detail.

Package Dimensions - 64 Lead MQFP



SYMBOL	DIMENSIONS					
	MILLIMETERS			INCHES		
	MS-022GA-2			MS-022GA-2		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.50	2.83	3.15	.098	.111	.124
A1	0.00	0.13	0.25	.000	.005	.010
A2	2.50	2.70	2.90	.098	.106	.114
b	0.35	---	0.50	.014	---	.020
b1	0.35	0.40	0.45	.014	.016	.018
c	0.09	---	0.20	.004	---	.007
c1	0.09	---	0.16	.004	---	.006
D	23.20 BSC			.913 BSC		
D1	20.00 BSC			.787 BSC		
D2	18.00 REF			.709 REF		
E	17.20 BSC			.677 BSC		
E1	14.00 BSC			.551 BSC		
E2	12.00 REF			.472 REF		
e	1.00 BSC			.039 BSC		
L	0.73	0.88	1.03	.029	.035	.040
L1	0.25 BSC			.010 BSC		
α	0°	---	7°	0°	---	7°
aaa	0.25			.010		
bbb	0.20			.008		
ccc	0.20			.008		
ddd	0.10			.004		

NOTES

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS AND INCHES.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
5. DATUM A - B AND D TO BE DETERMINED AT DATUM PLANE H.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSIONS, ALLOWABLE PROTRUSION IS 0.25mm PER SIDE, D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. OUTLINE CONFORMS TO JEDEC OUTLINE MS-022GB1.

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Operation Description

Overall Functional Diagram

A detailed functional diagram of the IR1110 and peripheral components is shown in Figure 4.

The IR1110 receives signals from the AC input lines U, V, W, and DC bus voltage, DC+, DC-, via resistor dividers, and delivers line-synchronized pulses SCRU, SCRV, SCRW to external SCR gate driver circuits. The timing of these pulses controls the DC bus voltage.

The IR1110 also delivers Status Feedback signals, that denote loss of all input phases, loss of one input phase and low/high AC line voltage.

The "ground" of the IR1110 is common with the SCR cathodes.

Line Voltage Processing circuit

The inputs to the line voltage processing circuit represent the voltage across the SCRs.

Each of the three outputs of this circuit, RINTU, RINTV, RINTW is a voltage waveform that is negative over the range of control of firing angle of the associated SCR, and positive outside this range.

The possible portion only of these waveforms appears at RSTRU, RSTRV, RSTRW.

Timing Wave Integrators

Each Timing Wave Integrator integrates the negative portions of the output waveforms of the Line Voltage Processing circuit, via R_{INT}, and the positive portions, via R_{INT} and R_{INTR} in parallel.

The outputs, CINTU, CINTV, CINTW are a set of line synchronized "sawtooth" timing waves. These have the desired phase relationship to the line voltages, so that intersection of these waves with the Timing Wave Reference defines the SCR firing instants. See Figure 5.

V_{PKL-L} Store

Voltages U_{IN}-V_{IN}, V_{IN}-W_{IN}, W_{IN}-U_{IN} are rectified and the peak value, proportional to the peak line voltage, is stored on C_{PKLL}. The time constant of R_{PKLL1} and R_{PKLL2} with C_{PKLL} allows V_{PLL} to track changes of line voltage that take place over a number of cycles, while maintaining an essentially smooth waveform.

Watchdog

The watchdog resets the Timing Wave Integrator within a few milliseconds of the normal reset point, should an abnormality in the line voltage waveshapes, such as one or all input phases missing, prevent resetting at the normal time.

In the normal operation, the watchdog circuit plays only a passive role.

V_{PK} Store

C_{PK} stores a voltage, V_{PK}, that is essentially equal to the peak of the timing waves. R_{PKD} is normally connected to ground via Q1. The time constant of R_{PKD} with C_{PK} allows V_{PK} to track changes of amplitude of the timing waves that take place over a number of cycles, while maintaining an essentially smooth waveform.

Ramp Circuit

The current source, IRAMP, creates an increasing voltage, VRAMP, across CRAMP, whenever Q3 has been conducting, then switches OFF. The maximum value of VRAMP is clamped at VPK.

VRAMP controls the ramp-up rate of the bus voltage. RRAMP shapes VRAMP to a parabolic form, which gives an approximately linear rise of DC bus voltage with a capacitive load.

The rate of change of VRAMP at the start of the ramp is set by CRAMP. RRAMP also has some influence on the initial rate of change, but more influence later during the ramp-up period.

The greater the initial rate of rise of VRAMP, the greater the maximum first firing angle.

Typical relationships between C_{RAMP},R_{RAMP},t_{DPWR}, t_{RAMP1}, and t_{D1FIRE} are as follows:

C_{RAMP} uF	R_{RAMP} kΩ	t_{DPWR} (typical) msec	t_{RAMP} (typical) msec	t_{D1FIRE} (max) degrees
0.68	130	165	100	35
1	82	190	150	32
2.2	47	230	220	25
3.3	30	270	330	22

The minimum and maximum permissible values of C_{RAMP} are 0.68uF and 3.3uF respectively. Total ramp-up time can be increased above the values shown by increasing R_{RAMP}. For example, with C_{RAMP}=3.3uF and R_{RAMP} open, ramp-up time increases to about 1.2 seconds.

The maximum first firing angle is specified at maximum AC input voltage, and assumes that worst case cumulative tolerances of the governing external components cause sufficient phase-to-phase unbalance that firing on one phase only occurs during the early part of ramp-up.

The circuit in Figure 15(a) will reduce the maximum first firing angle to 17°, if desired. If the voltage regulation function is not used, and the circuit of Figure 13 is not used, the Figure 15(b) circuit can be used in place of the Figure 15(a) circuit for the same purpose. With either circuit, both t_{DPWR} and t_{RAMP} will increase to about 400msec.

Ramp Clamp Circuit

When Q4 is OFF, the ramp clamp is enabled, and Q3 is controlled by the output of the Ramp Error Amplifier. This amplifier compares $|V_{BUSO}|$, via R_{CLAMP1}, with V_{RAMP}, via R_{CLAMP2}. The amplified output drives Q3 in a linear mode, diverting I_{RAMP} from C_{RAMP} and forcing V_{RAMP} to be essentially equal to V_{BUSO} x R_{CLAMP2}/R_{CLAMP1}.

During transient line voltage outage, the Ramp Clamp is enabled. V_{RAMP} is then forced into the above relationship with V_{BUSO}. The amplitude of V_{RAMP} is thereby preset when the line voltage returns, so that the bus voltage ramps back without significant delay, but also without unacceptable jump of bus voltage.

The choice of R_{CLAMP2}/R_{CLAMP1} is a compromise between the delay in starting ramp-back of the output voltage, and the initial jump of voltage when the line voltage returns after outage.

With an inductive filter at the output of the rectifier, R_{CLAMP2}/R_{CLAMP1} can be set to a higher value than with just a bus capacitor, to minimize the response time in restoring the DC bus voltage after line outage.

Timing Wave Reference Summing Amplifier

The output of the Timing Wave Reference Summing Amplifier is the Timing Wave Reference; this is essentially the difference between VPK and VRAMP, so long as the output of Error Amplifier 2 is zero. Thus, when VRAMP is zero, the Timing Wave Reference voltage is essentially equal to VPK, and SCR firing angle is close to the zero crossing of the line-to-line voltage; as the ramp increases, the firing angle advances. Refer to Figure 5.

Closed Loop Bus Voltage Regulation

The bus voltage reference, $-V_{BUSREF}$, sets the amplitude of the steady bus voltage. This external reference is negative with respect to “ground”, i.e., with respect to the positive output terminal of the rectifier bridge. This facilitates derivation of V_{BUSREF}, if required, via a level shift circuit that is referenced to the negative DC bus.

If bus voltage control is not used, and steady operation at the maximum DC bus voltage only is required, V_{BUSREF} should be connected to V_{SS}.

The Inverting Amplifier inverts the reference to $+V_{BUSREF}$. If the maximum possible value of $|V_{BUSO}|$ is less than $|V_{BUSREF}|$, the voltage regulation loop is inactive. The average output of Error Amplifier 1 is always negative, the voltage across C_{ERR} is clamped to zero by the parallel diode, the output of Error Amplifier 2 is always zero, and the bus voltage ramps to the maximum possible value.

If $|V_{BUSO}|$ becomes greater than $|V_{BUSREF}|$, the average output of Error Amplifier 1 becomes positive. This output is filtered by R_{ERR} and C_{ERR}, and a smooth voltage representing the dc error between $|V_{BUSO}|$ and $|V_{BUSREF}|$ appears across C_{ERR}. This voltage is amplified by Error Amplifier 2, and fed as an input to the Timing Wave Reference Summing Amplifier. The added input to the Timing Wave Reference Summing Amplifier increases the Timing Wave Reference, delaying the SCR firing angle, and forcing the bus voltage to a value proportional to $|V_{BUSREF}|$.

Since the voltage regulation circuit becomes active only when $|V_{BUSO}|$ exceeds $|V_{BUSREF}|$, the ramp rate during power-up of the bus voltage is determined solely by the rate of increase of V_{RAMP}. If $|V_{BUSO}|$ starts to exceed $|V_{BUSREF}|$ during ramp up, the output of Error Amplifier 2 starts to oppose the increasing ramp voltage, restraining further increase of bus voltage. Some overshoot occurs while the ramp continues to increase to V_{PK}.

In normal operation, after ramp up, the bus voltage is no longer controlled by the ramp, unless an event occurs that causes the ramp to be clamped.

Rise and fall rates of the bus voltage that are driven by changes in $|V_{BUSREF}|$ in normal operation are determined by the applied rise and fall rates of $|V_{BUSREF}|$, and by the characteristics

of the load connected to the DC bus. The rate of increase of applied $|V_{BUSREF}|$ should be limited if necessary, to limit the bus capacitor charging current.

Adjustment of DC loop gain

The voltage regulation loop may exhibit uneven firing angle from one SCR to the next, with loads which have unusually high ripple voltage. Such ripple instability, if it occurs, can be corrected by reducing the DC loop gain. Figure 6 shows how this is done with a voltage divider, R1 and R2, in the voltage regulation loop.

SCR Timing Comparators

Each SCR Timing Comparator delivers a high output whenever the Timing Wave is instantaneously greater than the Timing Wave Reference. The leading edge is the demanded initiation point for the SCR firing pulse.

The duration of the output pulse of the SCR timing comparator is generally much longer than needed to fire the SCR, because the Timing Wave remains higher than the Timing Wave Reference for a significant portion, if not all, of the total cycle time. See Figure 5.

SCR Voltage Comparators

Each SCR Voltage Comparator compares the instantaneous anode-cathode voltage of the SCR with a fixed reference, SCR_{REF}, which is set by R_{SG1} and R_{SG2}. This reference is set to represent an actual anode-cathode voltage of about 15V, before attenuation through the input divider resistors.

When the instantaneous SCR anode voltage is greater than 15V, the output of the SCR Voltage comparator is high. The outputs of the SCR Voltage and Timing Comparators are ANDed to obtain the output SCR timing pulses, SCRU, SCRV, SCRW.

The SCRU, SCRV, SCRW output pulses are thus controlled so that;

a) they do not occur when the Timing Wave is less than the Timing Wave Reference
b) they do not occur unless the instantaneous SCR voltage is at least 15V positive
c) they are terminated when the instantaneous anode-cathode voltage falls below 15V; -i.e. as soon as the SCR turns on

With discontinuous output current, more than one firing pulse per cycle for each SCR may be generated.

The pulse width of SCRU, SCRV, SCRW is about 6usec at maximum output voltage, and about 13usec at reduced output voltage.

SCR Gate Drivers

The SCR gate driver circuit, shown in Figure 7, amplifies and stretches the SCRU, SCRV, SCRW timing pulses. C1 and R2 stretch the duration of the output pulse to 60-80usec. This is generally necessary to ensure reliable SCR turn-on.

C2 and R4 provide an initial peak turn-on firing current of about .45A, decaying to about .2A within 5usec. The maximum average current consumed by the three SCR driver circuits is about 10mA.

If C2 and R4 are omitted, the peak firing current will be reduced to about .2A. R3 can be decreased to say 33W, to restore the peak firing current to .45A; the maximum average supply current will now increase to about 20mA.

Voltage Dip Circuit

The DC bus voltage will fall if the input line voltage dips or is lost.

For short period outage, the bus capacitor voltage may hold up sufficiently that ramp back when the line voltage returns is unnecessary.

If the bus voltage falls below a preset level, then the ramp is automatically clamped, in order to avoid an unacceptable jump of bus voltage when the line returns.

The Voltage Dip Comparator monitors dips on the DC bus voltage. The bus voltage, -V_{BUSO}, is captured on C_{HOLD}. The Voltage Dip Comparator compares a fraction of this captured voltage, with -V_{BUSO}.

In normal operation, |kV_{BUSO}| is less than |V_{BUSO}|, and the output of the Voltage Dip Comparator is high. When a short line outage occurs, the voltage captured on C_{HOLD} remains substantially equal to the pre-dip value, while |V_{BUSO}| starts to decrease as the bus capacitor discharges. If |V_{BUSO}| dips to less than k x V_{BUS1}, where V_{BUS1} is the initial bus voltage, the output of the Voltage Dip Comparator latches low, Q4 is switched off and the ramp is clamped. Q5 is turned ON, discharging the voltage on C_{ERR}.

$$kV_{BUS1} = \frac{R_{DIP2}}{R_{DIP1} + R_{DIP2}} \times V_{BUS1} - (0.1\ V_{LLMAX})$$

where V_{LLMAX} is the maximum design value of rms line voltage

The Voltage Dip Comparator remains low for a minimum period, T_{DELAY2}, of approxmately 5 milliseconds, set by C_{BDIP1}. Thereafter, so long as the line voltage is absent or remains abnormally low, the output of the Timing Wave Intersect Comparator remains low, keeping the Voltage Dip Comparator latched low.

T_{DELAY2} in milliseconds is approximately equal to (.0015 X C_{BDIP1} pF). Thus for C_{BDIP1} = 3300pF, T_{DELAY2} is about 5 milliseconds.

The total delay, T_{DELAY_TOT}, between the point of initiation of the line voltage outage, and the point at which the voltage dip comparator is allowed to reset, must be at least 10 milliseconds.

T_{DELAY_TOT} is the sum of T_{DELAY1} and T_{DELAY2}. T_{DELAY1} is the time between the point of initiation of the line outage, and the point at which the bus voltage falls to kVBUS1. Thus, with T_{DELAY2} set at 5 milliseconds, the minimum allowed value for T_{DELAY1} is 5 milliseconds.

If the bus capacitor is sized so that, at maximum DC load current, the bus voltage will fall to kVBUS1 in less than 5 milliseconds, then C_{BDIP1} should be increased to ensure that T_{DELAY_TOT} cannot fall below 10 milliseconds.

If C_{BDIP1} is increased so that T_{DELAY2} is at least 10 milliseconds, T_{DELAY_TOT} will always be greater than 10 milliseconds. This is an inherently safe design approach, though it does add a few milliseconds of potentially unnecessary delay, before ramp-back can commence during a short line outage.

After the above delay, the Voltage Dip Comparator is reset when the output of the Timing Wave Intersect Comparator goes high, which occurs when the line voltage returns to normal. Q2 is momentarily turned ON, allowing the voltage on C_{HOLD} to reset. Q4 is turned ON, unclamping the Ramp, and Q5 is turned OFF, unclamping C_{ERR}. Ramp-back of the bus voltage now occurs.

When the output of the Voltage Dip Comparator is low, Q1 is turned OFF. R_{PKD} is then disconnected from ground, allowing C_{PK} to hold its charge during the voltage dip.

Voltage Dip during Dynamic Regulation

If $|V_{BREF}|$ is rapidly decreased by a sufficient amount, this may cause a decrease of bus voltage that will set the Voltage Dip Comparator and cause the bus voltage to undershoot.

Since the timing waves are still present, the output of the Timing Wave Intersect Comparator remains high, and the Voltage Dip Comparator will be quickly reset, ramping the bus voltage back to the set value.

This undershoot of the bus voltage will be avoided if changes in $|V_{BUSREF}|$ are controlled at a rate that does not significantly "overtake" the discharge rate of C_{HOLD}, which is set by C_{HOLD}, R_{DIP1} and R_{DIP2}.

Undervoltage and Undervoltage Lockout Comparators

The UV Comparator delivers a high output when V_{DD} exceeds the internally fixed reference value.

The UV Lockout Comparator delivers a high output when the voltage C_{UVLO} exceeds a nominal value of about 1.5V. C_{UVLO} is driven from a current source of approximately 2uA.

The outputs of the UV and UV Lockout Comparators are ANDed. When the output of either comparator is low, the SCR firing pulses are inhibited, and Q4 is turned OFF, clamping the ramp.

One Phase Loss Circuit

A train of fixed duration (nominal 2msec) pulses are delivered to the gate of Q6, if one input phase is missing. With 1-phase shutdown enabled, each 1-phase loss pulse discharges C_{UVLO} by about 1.5V. During the third successive pulse, C_{UVLO} is discharged sufficiently that the output of the UV Lockout Comparator goes low.

The principle of generation of the 1-phase loss pulses is illustrated in Figure 8. These pulses are generated;

(a) during one phase loss

(b) briefly during abnormal dips of line voltage

(c) if the DC bus is short circuited and the SCR firing angle is advanced by more than about 30° from the zero crossing of the line voltage

With 1-phase shutdown enabled, generation of "1-phase loss" pulses under condition (b) reinforces the ramp clamp function. Under condition (c) it results in automatic limiting of short circuit current, as explained later.

The 1-phase loss pulses at 1PHLED output follow the output of the 1-Phase Loss Circuit.

Line Loss Circuit

The output of the line loss detection circuit is high in normal operation. If all input phases are lost, it goes low, after a delay, determined by C_{3PH}, which would typically be set to about 2 cycles.

When the output of the Line Loss circuit goes low, Q1 is turned OFF. This disconnects R_{PKD} from ground, allowing C_{PK} to hold its charge during the line outage.

The output of the line loss circuit feeds via NAND 2 to the LNLSLED output driver. If LNLSSL is connected to V_{SS}, the 1-phase loss pulses are multiplexed with the output of the line loss circuit at the LNLSLED output. If LNLSSL is connected to V_{DD}, the LNLSLED signal signifies loss of all input phase only.

Line Voltage Comparator

The output of the Line Voltage Comparator is low when V_{PKLL} exceeds a reference value that is set by R_{LS1} and R_{LS2}. The LNLED output follows the output of the Line Voltage comparator.

PWM Control of V_{BUSREF}

V_{BUSREF} can be controlled by Pulse Width Modulation (PWM). The IR1110 responds only to the average value of this waveform; suitable PWM frequency is in the range of one to several kHz.

Figure 9 shows an opto-coupler circuit for transmitting an isolated PWM input.

Control of the ON/OFF duty cycle of the opto-transistor, from 0 to 100%, controls the average value of V_{BUSREF} from V_{MIN} to V_{MAX}, where;

$$V_{MIN} = \frac{R_1}{R_1 + R_2} V_{SS}$$

$$V_{MAX} = \frac{R_1}{R_1 + R'} V_{SS}$$

$$R' = \frac{R_2 R_3}{R_2 + R_3}$$

The average value of $V_{BUSREF}(D)$ at duty cycle D is:

$$V_{BUSREF}(D) = V_{MIN} + D(V_{MAX} - V_{MIN})$$

As an example, if V_{SS} = -5.0V, R_1 = 7.32k, R_2 = 16.9k, R_3 = 1.91k, then the average value of V_{BUSREF} will be controlled from approximately -1.5V to -4.0V, corresponding to a range of control of the bus voltage from 37.5% to 100% of the maximum value at maximum operating line voltage.

Dedicated One Phase Operation

The IR1110 can be set for dedicated operation of a 1-phase half-controlled SCR bridge. The UIN and VIN input terminals are used. No connection is made to WIN.

When Pin 12 is connected to V_{SS}, the W timing wave and watchdog circuits are disabled, the watchdog reset time is optimized for 1-phase operation, and 1-phase shutdown is disabled, regardless of the connection of Pin 13.

Snubber Derived Power Supply

Snubbers will generally be required, either across the AC lines or directly across the SCRs, to limit dv/dt when the line voltage is switched on.

If SCR snubbers are used, the snubber current can be used to derive the power supply voltages for the IR1110 and SCR drivers.

With reference to Figure 10, positive snubber current flows via the three RC snubbers and the D+ diodes, to create a nominal 15V supply across ZD1 and C1, for the SCR driver.

A nominal positive 5.1V V_{DD} supply is developed across ZD2 and C2. Negative snubber current flows via D- diodes, to create a nominal -5.1V V_{SS} supply across ZD3 and C3.

The ZD1 and ZD4 protect the supply voltages against transients on the line voltages.

This power supply circuit requires that the average current consumed by the SCR driver circuits does not exceed about 10mA.

Note that an auxiliary winding on a DC bus derived switching power supply would not by itself serve the IR1110. This is because bus-derived power cannot deliver voltage until *after* charging of the DC bus capacitor has already commenced, while the IR1110 must be powered *before* charging of the bus capacitor commences.

It would be possible to use an auxiliary winding on a DC bus derived power supply to supplement the snubber derived power. This could be preferred where the AC input line inductance is high, therefore only minimal snubbers - insufficient to furnish the total power required by the IR1110 and SCR drivers - are needed for dv/dt protection of the SCRs.

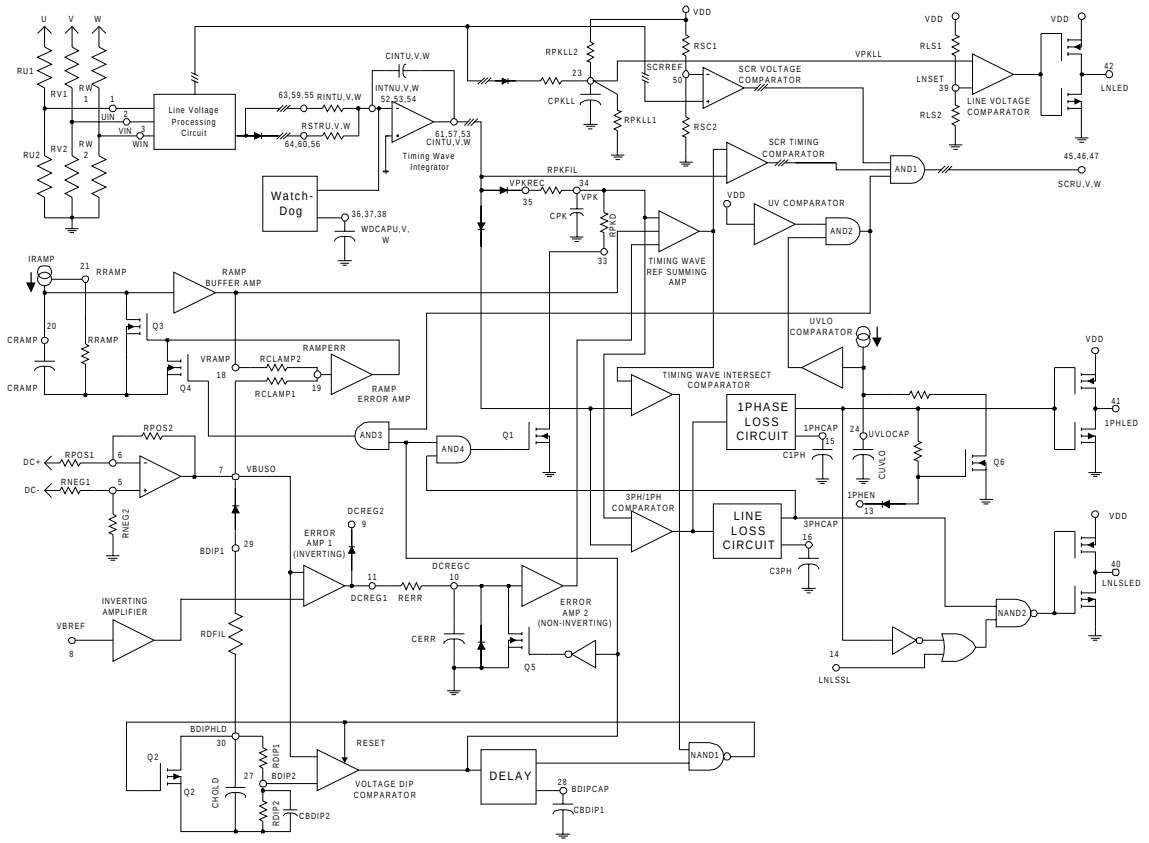


Figure 4 Detailed Functional Block Diagram

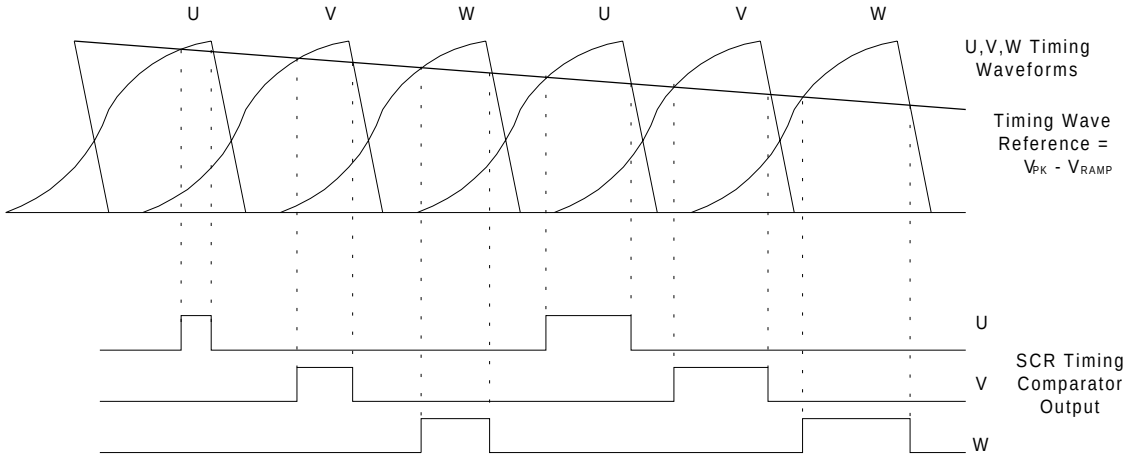


Figure 5 Timing Waveforms, Timing Wave Reference SCR Timing Comparators

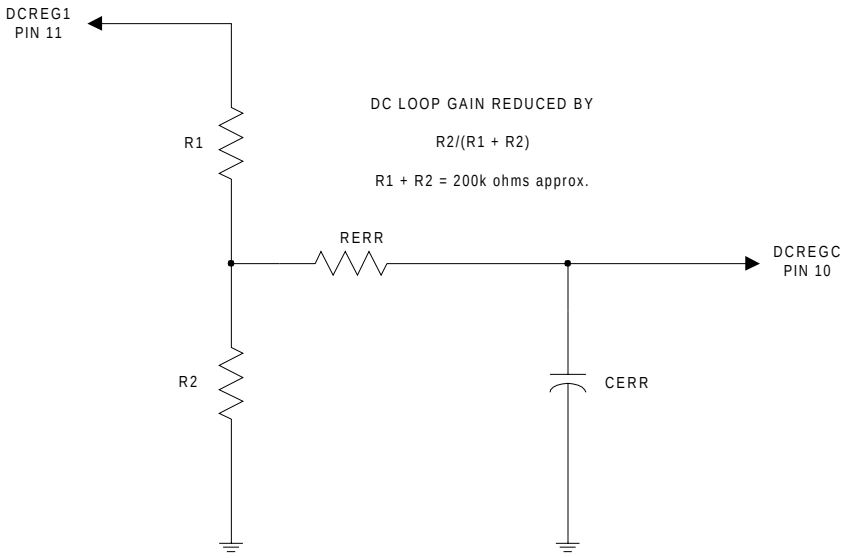


Figure 6 Circuit for Reducing the DC loop gain

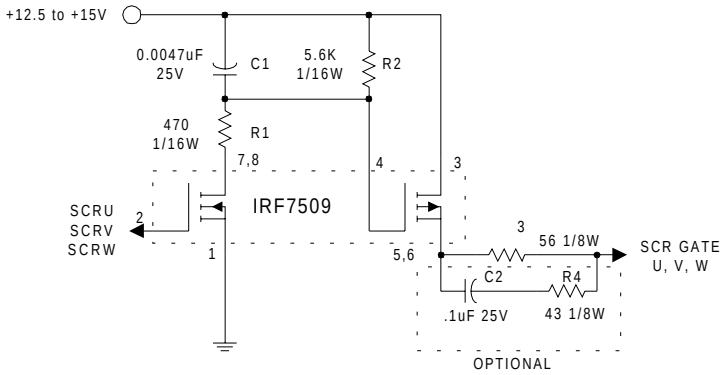


Figure 7 SCR Gate Driver Circuit

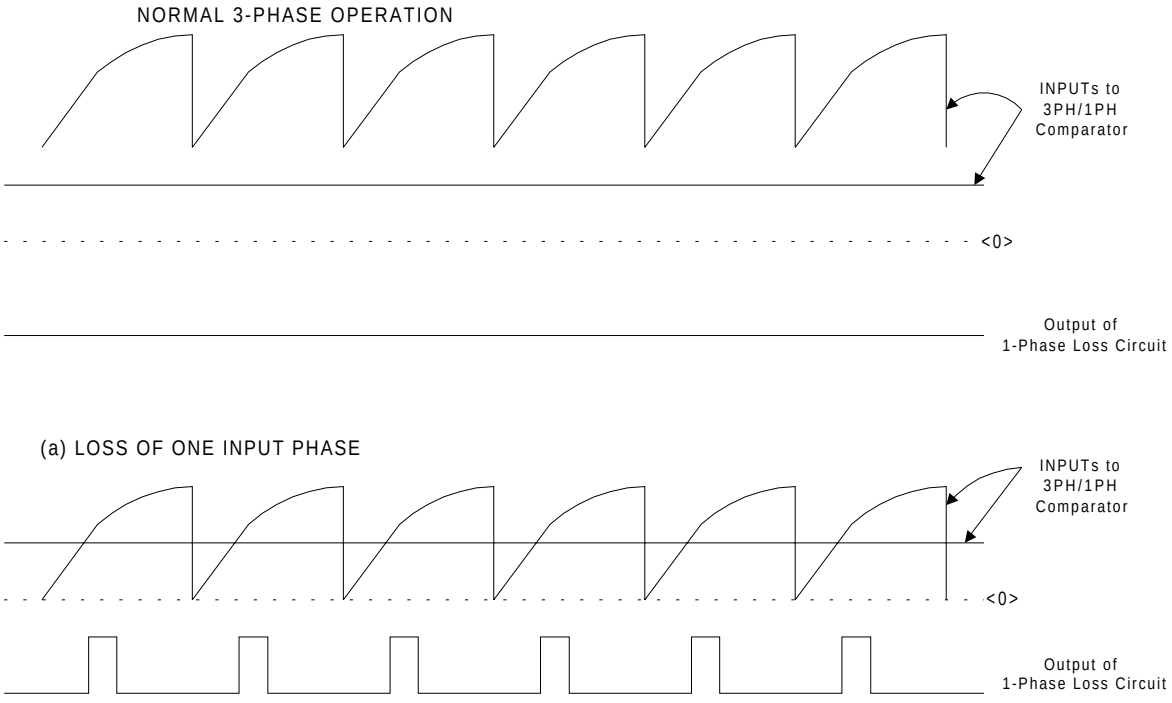


Figure 8, 8(a) Principle of Generation of 1-Phase Loss Pulses

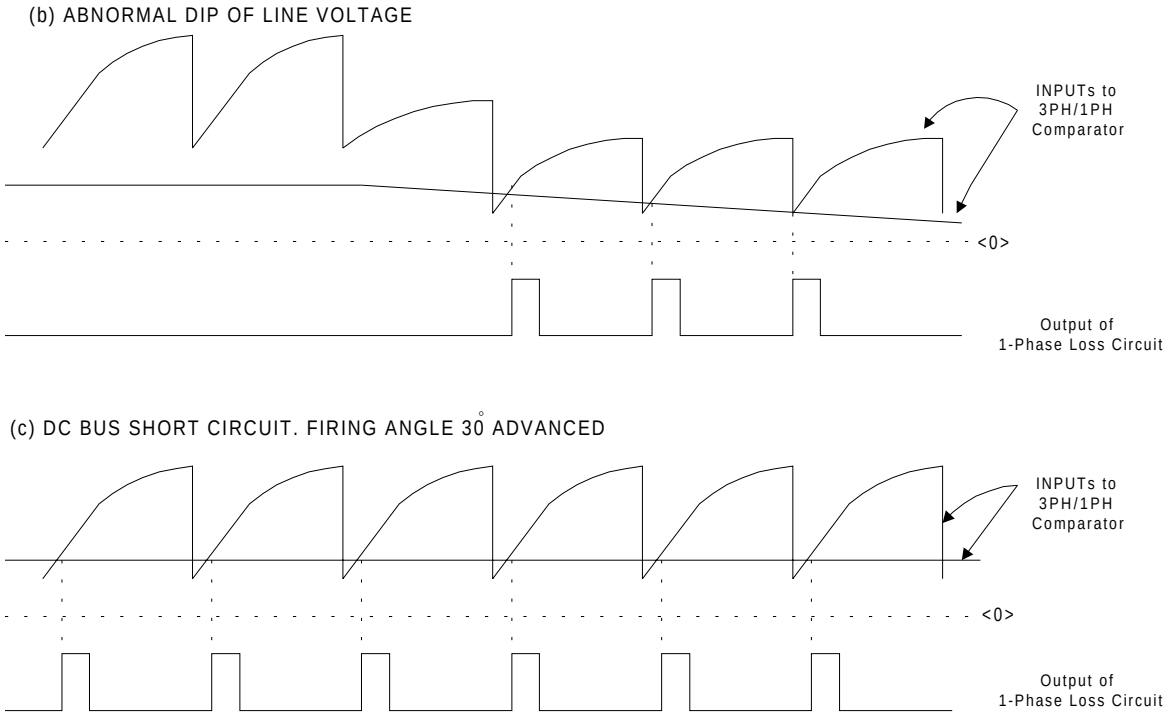


Figure 8(b), 8(c) Principle of Generation of 1-Phase Loss Pulses

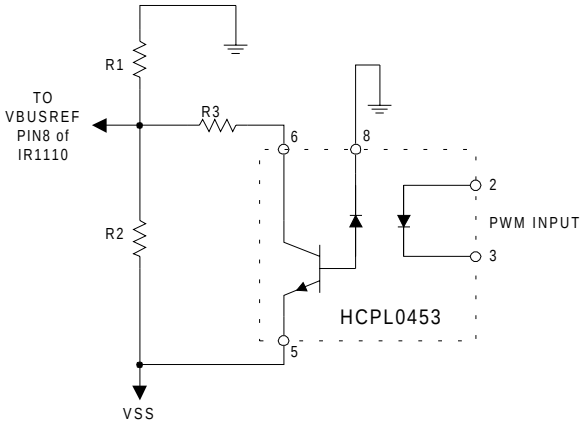


Figure 9 Circuit for PWM Control of DC Bus Voltage

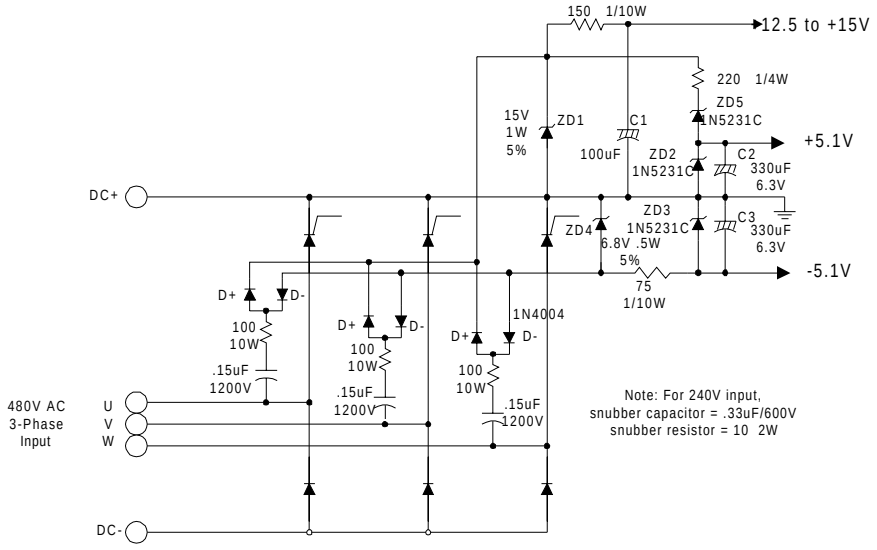
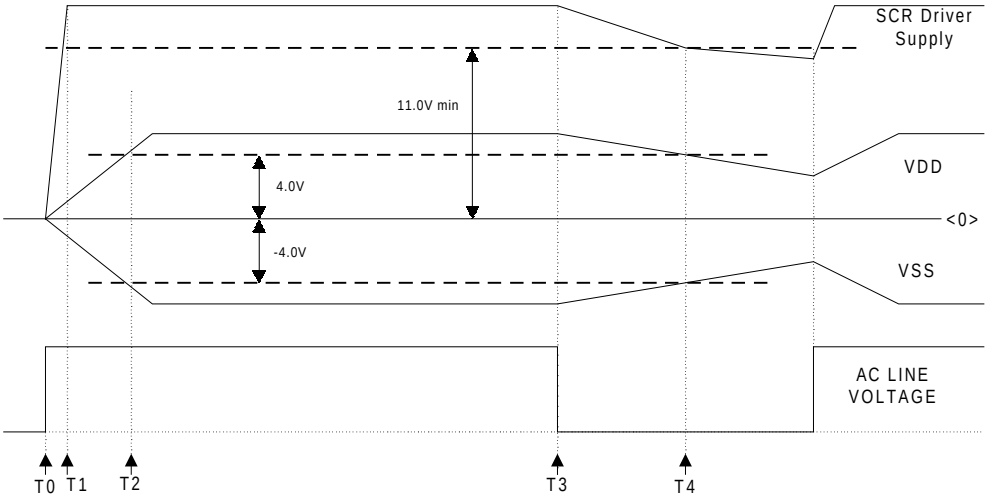


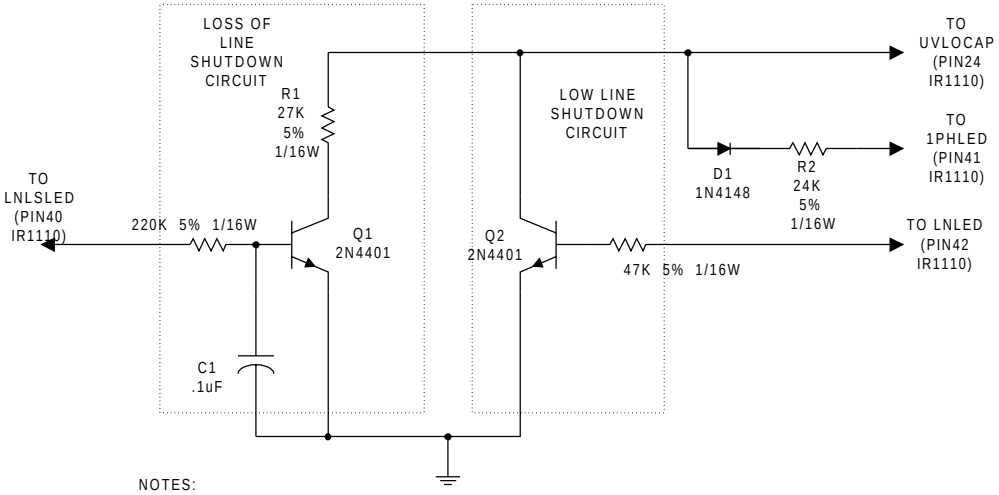
Figure 10 Snubber Derived Power Supply



1.0msec < T0 - T1 < 80msec
100msec < T1 - T2
T3 - T4 < 40msec
VSS should track VDD within +/-10% during rise/fall time

Note: T4 is the event of Undervoltage Lockout

Figure 11 Power Supply Requirement



NOTES:
(1) If Pin14 to VDD, use CUVLO=.1uF and omit D1,R2
(2) If Pin14 to VSS, use CUVLO=.22uF and omit C1,D1,R2
(3) If power supply rise time < 80msec (Figure 11), connect pin 14 to VSS, use CUVLO=.22uF, and omit C1,D1,R2.
(4) If Figure 13 circuit is used. Connect pin 14 to VDD. Use CUVLO=0.22uF and R1=0.
(5) Set RLS1, RLS2 for LNLED low above 85% of min operating voltage

Figure 12 Loss of Line and Low Line Shutdown Circuits

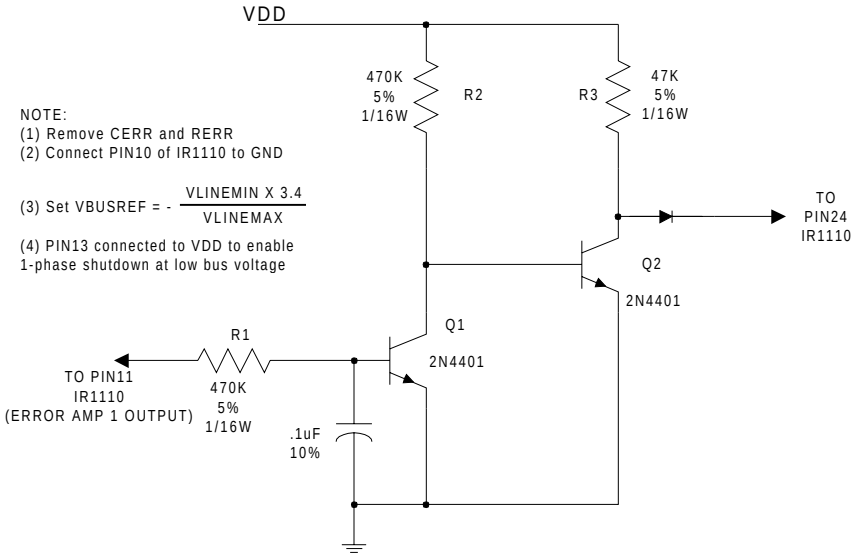


Figure 13 Circuit for Enabling 1-Phase Shutdown During Ramp-Up, Disabling During Normal Operation (Bus Voltage Control Function Not Used)

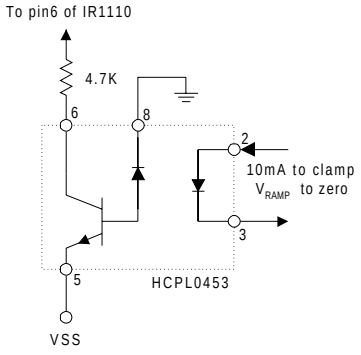


Figure 14 Circuit for Externally Clamping V_{RAMP} to zero

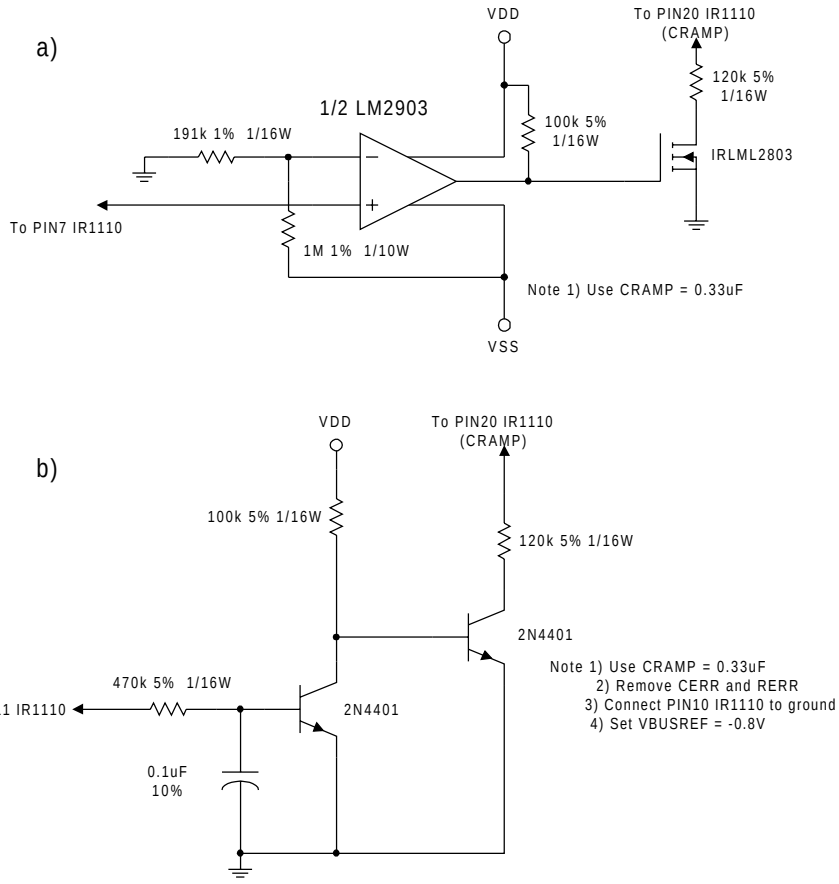


Figure 15 Circuits for reducing t_{D1FIRE}

Operating Scenarios and Design Options

Power Supply Response Characteristics

The UV comparator responds to the amplitude of the V_{DD} supply, to control the ramp clamp.

In order to correctly accomplish this function, the power supply should have the response characteristics illustrated in Figure 11, and 1-phase shutdown must be enabled. A minimum rise time of 100msec during initial power-up is required to provide sufficient delay time, before the output of the UV comparator goes high, for V_{PK} to become established before ramp-up commences.

During loss of line voltage, V_{DD} should not hold up above 4.0V for more than 40msec, to ensure timely clamping of the ramp via the UV comparator.

The snubber derived power supply in Figure 10 has the required rise time, however hold-up time exceeds 40msec. Timely clamping of the ramp can instead be accomplished by the external Loss of Line Shutdown circuit, described below.

If 1-phase shutdown is disabled, the rise time of VDD must be increased to about 200msec to control the ramp clamping function. In this case it may generally be better to control the ramp clamp via the UVLO comparator, by increasing CUVLO to 0.22uF. The rise time of VDD is no longer critical, and can have a minimum value of 1msec.

Loss of Line Shutdown circuits

The Loss of Line Shutdown circuit in Figure 12 clamps the ramp during line outage, via the Undervoltage Lockout Comparator.

The Note (3) option of Figure 12 also eliminates dependence on a minimum power supply rise time of 80msec. C_{UVLO} is increased to 0.22uF, to provide sufficient delay during power-up, via the UVLO Comparator. The rise time of the power supply is not now critical, and can have a minimum value of 2.0msec.

A side effect of increasing C_{UVLO} is to increase the shutdown time when one phase is lost. With Pin 14 connected to V_{SS}, this is corrected by Q1 being turned on during each 1-phase loss pulse, which adds to the discharge current for C_{UVLO}, via R1.

Low Line Shutdown circuit

The Low Line Shutdown circuit in Figure 12 clamps the ramp and removes the SCR firing pulses if the line voltage falls to less than 85% of the minimum normal operating level. This circuit may not be necessary for all applications, but its inclusion will provide added insurance of correct operation during abnormal low line conditions.

Loss of one phase during three phase operation

The 1-Phase Shutdown circuit clamps the ramp and removes the SCR firing pulses if one input phase is lost for more than about one cycle. When the missing phase returns, the ramp is unclamped and the bus voltage ramps back to the set value.

If 1-Phase Shutdown is disabled, the IR1110 will continue to deliver DC bus voltage when one input phase is lost. A potential problem arises, however, if the bus voltage is being regulated significantly below the maximum value. If one phase is lost and the ramp remains unclamped for more than one or two cycles, when the missing phase returns the bus voltage may transiently jump to almost the maximum possible value, before it is regulated back to the set value. This can

result in excessive bus capacitor charging current.

For this reason it is recommended that *the 1-Phase Shutdown circuit is enabled, (Pin 13 connected to VDD) in designs where the voltage control function of the IR1110 is used*.

For designs where the voltage control function is not used, operation at full bus voltage, with 1 Phase Shutdown disabled, allows natural transitioning from 3-Phase to 1-Phase operation, and vice versa, without excessive voltage jumps.

With 1-Phase Shutdown disabled, however, transient loss of one phase, during the early part of ramp-up, could cause a jump of bus voltage and a high instantaneous bus capacitor charging current, if the missing phase returns before ramp-up has finished, while the instantaneous bus voltage is still low.

The likelihood is remote of one phase being lost and then returning during the infrequently occurring first 50 to 100ms window of the initial ramp-up period. Given the improbability of such an event, provided the instantaneous charging current cannot exceed the surge capability of the SCRs, no additional remedy may generally be necessary.

The circuit shown in Figure 13 can be used to protect against this unlikely event, if judged necessary. The polarity of the Error Amplifier 1 average output signifies whether the instantaneous bus voltage is above or below a fixed level, set by VBREF.

If one phase loss occurs during ramp-up, when the bus voltage is instantaneously below the set level, the output of Error Amplifier 1 is negative, and Q2 is ON, 1-Phase Shutdown is enabled. If one phase loss occurs at instantaneous bus voltage above the set level, Q2 is OFF and the voltage on C_{UVLO} is pulled high by R3, disabling 1-Phase Shutdown.

DC bus Short Circuit

With a short circuit across the DC bus, the line-to-line voltages collapse to zero at the SCR firing instants, causing the timing waves to terminate prematurely.

If a short circuit is present at start up, 1-phase loss pulses start to be generated as the ramp increases, and the firing angle advances by more than about 30°. See Figure 8. With 1-Phase Shutdown enabled, these pulses set the UV lock comparator and clamp the ramp.

The overall result is that the short circuit current is automatically limited to a relatively low pulsatingt level, as the ramp repeatedly tries to increase, then is rest each time the firing angle attempts to advance by more than 30°.

If a short circuit occurs during normal operation, the bus dip comparator resets the ramp to zero, limiting the short circuit current within less than half cycle. Thereafter, the short circuit current is automatically limited to relatively low pulsating level, as described above.

The short circuit condition is signified by 1-phase loss pulses appearing and disappearing, as the ramp increases then resets, accompanied by essentially zero bus voltage. The interval between pulses depends upon C_{RAMP}.

If 1-Phase Shutdown is disabled, and a short circuit exists at start up, the ramp increases, advancing the SCR firing angle, until the line fuses blow, or other external action occurs. For

example, CRAMP could be clamped via an opto-coupler device to limit the short circuit current.

If a short circuit occurs during normal operation, the voltage dip comparator resets the ramp, limiting the short circuit current within less than half a cycle. The ramp will then increase again, until the line fuses blow or other action is taken.

The short circuit condition is signified by a train of 1-phase loss pulses, accompanied by essentially zero bus voltage.

Externally controlled shutdown of the rectifier

The circuit in Figure 14 can be used, if desired, to externally clamp the ramp voltage, hence also the output voltage of the rectifier, to zero.

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