Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of http://www.nxp.com, http://www.philips.com/ or http://www.semiconductors.philips.com/, use **http://www.nexperia.com**

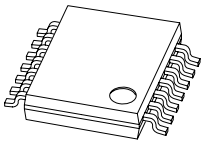
Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use **salesaddresses@nexperia.com** (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:
- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved
Should be replaced with:
- **© Nexperia B.V. (year). All rights reserved**.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia



IP4769CZ14

VGA interface ESD protection with integrated termination resistors

Rev. 1 — 17 January 2011 Product data sheet

1. Product profile

1.1 General description

The IP4769CZ14 connects between the Video Graphics Adapter (VGA)/Digital Video Interface (DVI) and the video transmitter like e.g. a PC graphic card or the VGA receiver like e.g. a PC Monitor.

The IP4769CZ14 includes ElectroStatic Discharge (ESD) protection for the Data Display Channel (DDC) signals, DDC level shifting and ESD protection for both SYNChronization (SYNC) lines as well as high-level ESD protection diodes for the Red-Green-Blue (RGB) signal lines.

The DDC level shifting can be used to shift the 5 V DDC bus at the connector side to 3.3 V or 2.5 V on the internal side.

1.2 Features and benefits

- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- Integrated high-level ESD protection and level shifting
- DDC level shifting from 5 V to 3.3 V or 2.5 V
- IEC 61000-4-2, ±4 kV rail-to-rail clamping for each I/O line
- Channel capacitance C_{ch} < 4 pF

1.3 Applications

- To reduce ElectroMagnetic Interferences (EMI)/Radio Frequency Interferences (RFI) and to provide downstream ESD protection for:
  - VGA interfaces including DDC channels
  - Desktop and notebook PCs
  - Graphics cards
  - Set-top boxes

2. Pinning information

2.1 Pinning

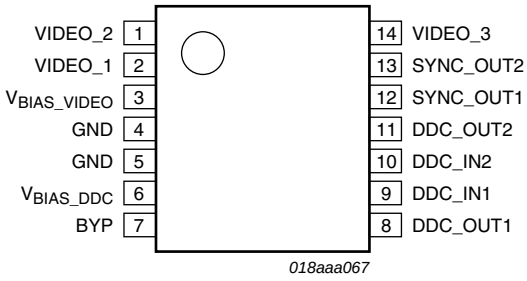


Fig 1. Pin configuration

2.2 Pin description

Table 1. Pin description

Symbol	Pin	Description
VIDEO_2	1	video signal ESD protection channel 2
VIDEO_1	2	video signal ESD protection channel 1
V_{BIAS_VIDEO}	3	ESD bias voltage for VIDEO_1, VIDEO_2 and VIDEO_3 protection circuit
GND	4	ground
GND	5	ground
V_{BIAS_DDC}	6	bias voltage for DDC level shifter N-FET gates
BYP	7	optional external 100 nF bypass capacitor to enhance internal zener performance on SYNC_OUT1, SYNC_OUT2, DDC_OUT1 and DDC_OUT2
DDC_OUT1	8	DDC signal output 1; connector side
DDC_IN1	9	DDC signal input 1; VGA controller side
DDC_IN2	10	DDC signal input 2; VGA controller side
DDC_OUT2	11	DDC signal output 2; connector side
SYNC_OUT1	12	SYNC signal output 1; ESD clamp; connector side
SYNC_OUT2	13	SYNC signal output 2; ESD clamp; connector side
VIDEO_3	14	video signal ESD protection channel 3

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP4769CZ14	TSSOP14	plastic shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

4. Functional diagram

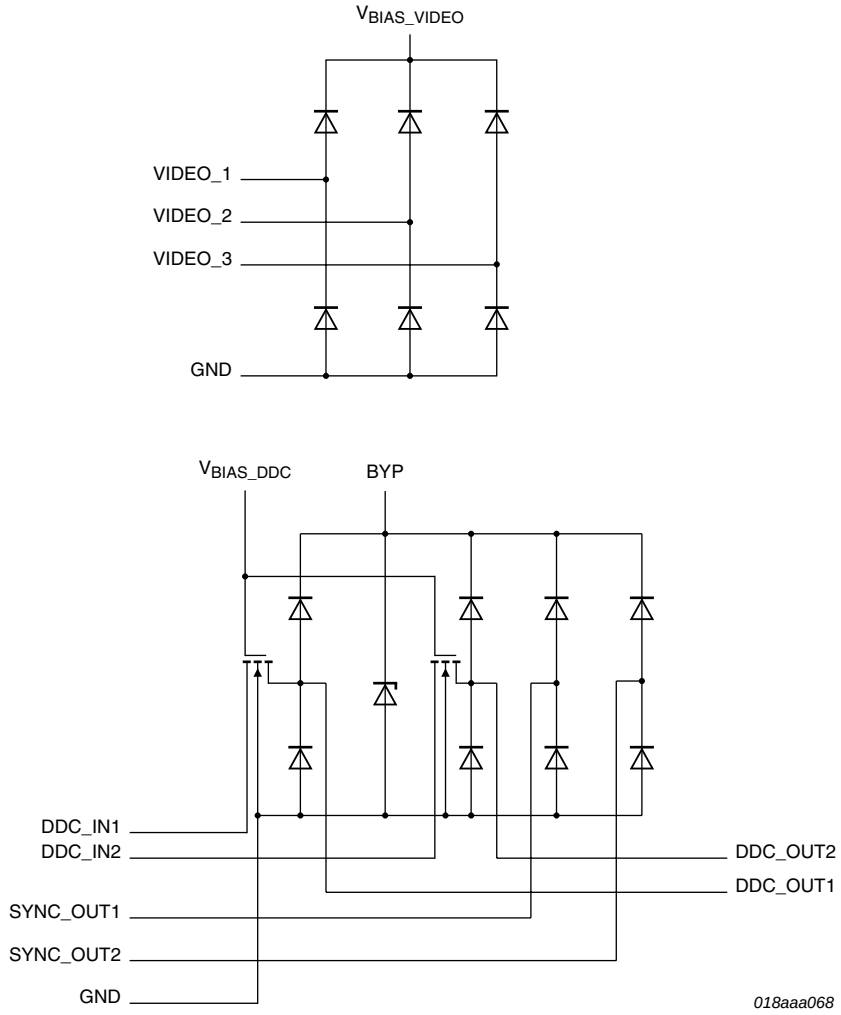


Fig 2. Functional diagram

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

5. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	all pins	[1][2]	-	±6	kV
			[3]	-	±200	V
			[4]	-	±2	kV
$V_{CC(VIDEO)}$	video supply voltage			–0.5	5.5	V
$V_{CC(DDC)}$	data display channel supply voltage			–0.5	5.5	V
$V_{I(VIDEO_2)}$	input voltage on pin VIDEO_2			–0.5	$V_{CC(VIDEO)}$	V
$V_{I(VIDEO_3)}$	input voltage on pin VIDEO_3			–0.5	$V_{CC(VIDEO)}$	V
$V_{I(DDC_IN1)}$	input voltage on pin DDC_IN1			–0.5	5.5	V
$V_{I(DDC_IN2)}$	input voltage on pin DDC_IN2			–0.5	5.5	V
$V_{O(DDC_OUT1)}$	output voltage on pin DDC_OUT1			–0.5	5.5	V
$V_{O(DDC_OUT2)}$	output voltage on pin DDC_OUT2			–0.5	5.5	V
T_{stg}	storage temperature			–55	+125	°C

[1] BYP, VCC_VIDEO and VCC_SYNC must be bypassed to GND via a low impedance ground plane with 100 nF, low inductance, chip ceramic capacitor at each supply pin. ESD pulse is applied between the pins (VIDEO_1; VIDEO_2; VIDEO_3; SYNC_OUT1; SYNC_OUT2; DCC_OUT1; DCC_OUT2) and GND.

[2] According to IEC 61000-4-2, level 3, contact discharge.

[3] Machine model according to ESD22-A115-A.

[4] Human Body Model (HBM) according to JESD22-A-J114D.

6. Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb}	ambient temperature		–40	-	+85	°C

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

7. Characteristics

Table 5. Analog video (R, G, B) characteristics

$V_{CC(VIDEO)}$ = 5 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CC}	supply current	static input signals		-	-	10	μA
C_{ch}	channel capacitance	f = 1 MHz; V_I = 2.5 $V_{(p-p)}$; V_{bias} = 2.5 V	[1]	-	-	4	pF
$I_{i(video)}$	video input current	V_{IN} = $V_{CC(VIDEO)}$ or V_{IN} = GND		−1	-	+1	μA
V_F	forward voltage	I_F = 1 mA		-	0.7	-	V

[1] This parameter is guaranteed by design and characterization.

Table 6. DDC level shifter characteristics

$V_{CC(DDC)}$ = 5 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_{ch}	channel capacitance	f = 1 MHz; V_I = 2.5 $V_{(p-p)}$; V_{bias} = 2.5 V	[1]	-	-	4	pF
R_{dyn}	dynamic resistance	I = 1 A	[2]				
		positive transient		-	-	2.4	Ω
		negative transient		-	-	1.3	Ω
V_{CL}	clamping voltage	V_{ESD} = 8 kV; positive transient	[3]	-	8	-	V
ΔV_{on}	on-state voltage drop		[4]	-	85	140	mV
V_F	forward voltage	I_F = 1 mA		-	0.7	-	V

[1] This parameter is guaranteed by design and characterization.

[2] According to IEC 61000-4-5 and IEC 61000-4-9.

[3] According to IEC 61000-4-2, contact discharge.

[4] For level shifting N-FET.

Table 7. SYNC protection characteristics

$V_{CC(SYNC)}$ = 5 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_{ch}	channel capacitance	f = 1 MHz; $V_{CC(SYNC)}$ = 2.5 $V_{(p-p)}$; V_{bias} = 2.5 V	[1]	-	-	4	pF
V_F	forward voltage	I_F = 1 mA		-	0.7	-	V

[1] This parameter is guaranteed by design and characterization.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

8. Application information

To maximize ESD clamping performance, the IP4769CZ14 should be placed as close as possible to the VGA/DVI connector. The ESD protection channels VIDEO_1, VIDEO_2 and VIDEO_3 are identical and can be connected in any order with R, B, G signals to simplify routing, and minimize stubs and vias. The SYNC protection lines are also identical and can be used in any order for HSYNC or VSYNC signals. The DDC level shifter lines are likewise identical in function.

The pull-up resistors on the DDC lines are dictated by the application, depending on the values of the internal pull-ups provided in the Application-Specific Integrated Circuit (ASIC), etc. Weak pull-ups may be required, for example, to pull up the DDC_INx lines to VCC_5V when no monitor is connected, if the local ASIC does not include internal pull-ups. Unexpected backdrive current can flow through these resistors though, when an external monitor is powered and the local VCC_5V is powered down. Backdrive protection should be considered if this is a concern.

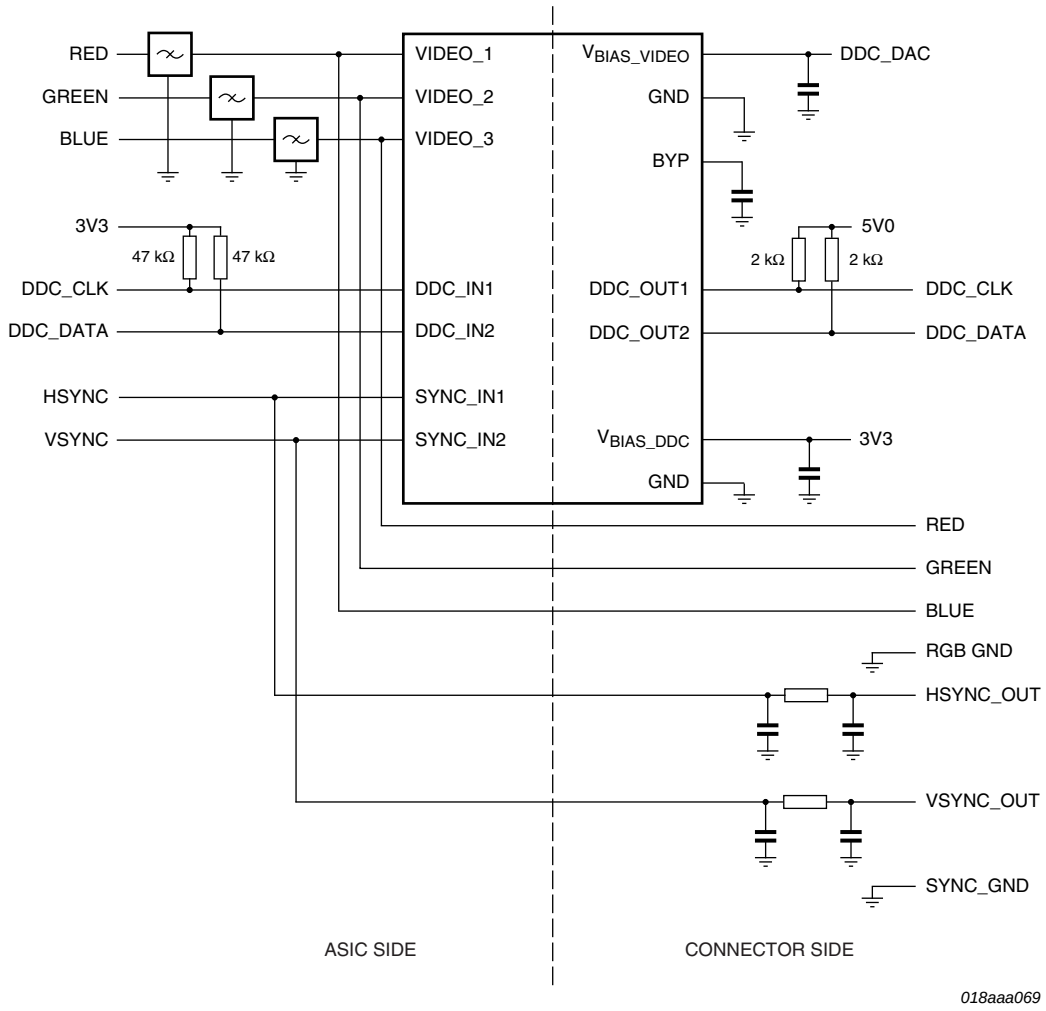


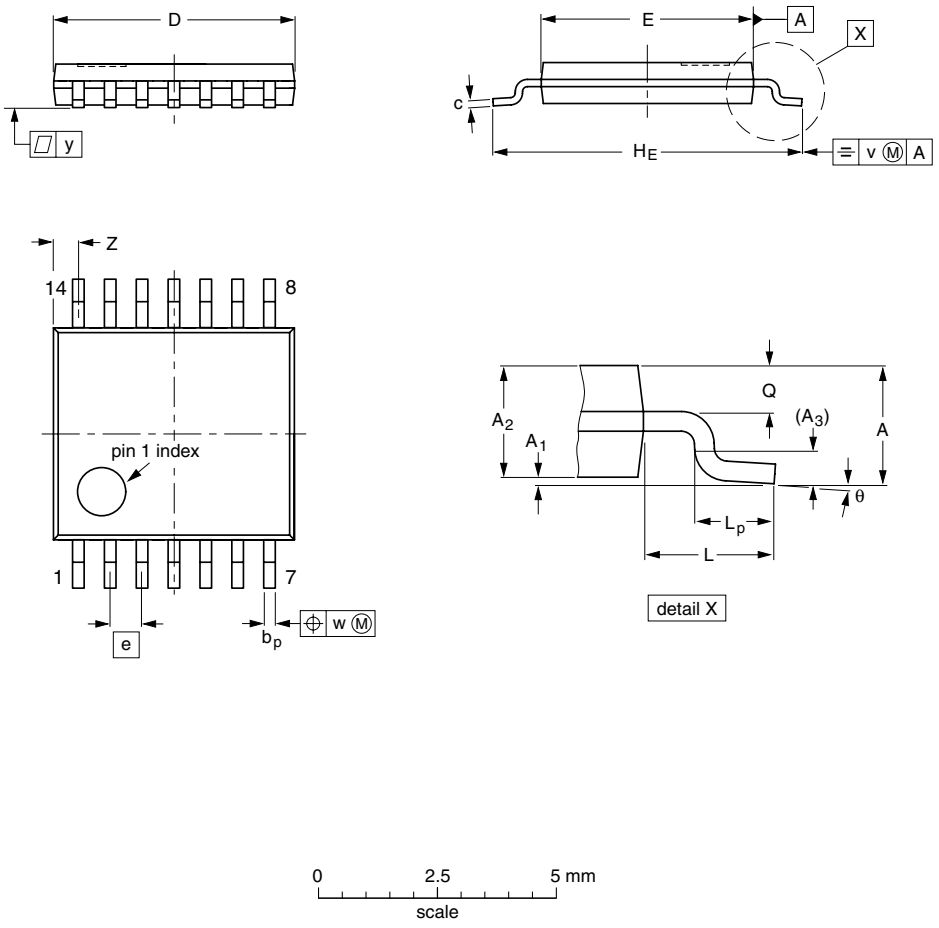
Fig 3. Application diagram

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

9. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 4. Package outline SOT402-1 (TSSOP14/MO-153)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

10. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4769CZ14 v.1	20110117	Product data sheet	-	-

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

11.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

11.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

11.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

12. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

13. Contents

1 Product profile 1
1.1 General description 1
1.2 Features and benefits 1
1.3 Applications 1
2 Pinning information 2
2.1 Pinning 2
2.2 Pin description 2
3 Ordering information 2
4 Functional diagram 3
5 Limiting values 4
6 Recommended operating conditions 4
7 Characteristics 5
8 Application information 6
9 Package outline 7
10 Revision history 8
11 Legal information 9
11.1 Data sheet status 9
11.2 Definitions 9
11.3 Disclaimers 9
11.4 Trademarks 10
12 Contact information 10
13 Contents 11

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2011. **All rights reserved.**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 17 January 2011
Document identifier: IP4769CZ14