IP4309CX9

HDMI octal channel low capacitive high-performance ESD protection

Rev. 1 — 10 March 2011 Product data sheet

1. Product profile

1.1 General description

The IP4309CX9 is a 8-channel low capacitance ElectroStatic Discharge (ESD) protection device, providing protection to downstream components from ESD voltages up to ±15 kV contact discharge and higher than ±15 kV air discharge, far exceeding IEC 61000-4-2, level 4.

The device is optimized for the protection of high-speed interfaces such as High-Definition Multimedia Interface (HDMI), Digital Video Interface (DVI) and other interfaces requiring very low capacitance ESD protection. In order to prevent any current backdrive into the adjacent channel, all eight ESD protection channels are electrically separated and share only the same ground connections.

The IP4309CX9 is fabricated using monolithic silicon technology in a single Wafer Level Chip-Size Package (WLCSP). These features make IP4309CX9 ideal for use in applications requiring component miniaturization, such as mobile phone handsets.

1.2 Features and benefits

- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (dark green compliant)
- 8 ultra low input capacitance rail-to-rail ESD protection diodes with $C_{I/O}$ = 1.3 pF
- R_{dyn} = 0.45 Ω
- Downstream ESD protection up to ±15 kV (contact), exceeding IEC 61000-4-2, level 4
- 3 × 3 pin WLCSP with 0.4 mm pitch

1.3 Applications

- High-speed interface ESD protection such as HDMI, DVI and USB etc.
- Interfaces with special requirements on low capacitive ESD protection
- Interfaces requiring separation of the positive clamping voltage / current path

2. Pinning information

2.1 Pinning

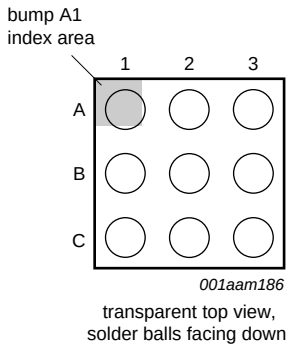


Fig 1. Pin configuration IP4309CX9

2.2 Pin description

Table 1. Pinning

Pin	Description
A1	ESD protection
A2	ESD protection
A3	ESD protection
B1	ESD protection
B2	ground
B3	ESD protection
C1	ESD protection
C2	ESD protection
C3	ESD protection

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3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP4309CX9	WLCSP9	wafer level chip-size package; 9 bumps; 1.16 × 1.16 × 0.61 mm	IP4309CX9

4. Functional diagram

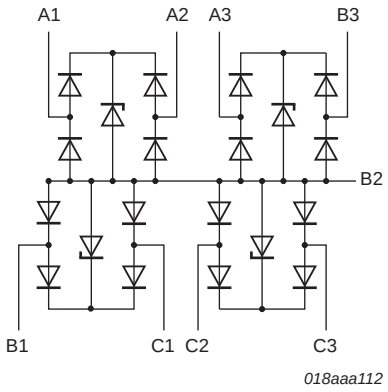


Fig 2. Schematic diagram IP4309CX9

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5. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage	at I/O pins		–0.5	+5.5	V
V_{ESD}	electrostatic discharge voltage		[1]			
		contact discharge	[2]	-	±15	kV
		air discharge	[2]	-	±15	kV
		IEC 61000-4-2, level 4				
		contact discharge		-	±8	kV
		air discharge		-	±15	kV
T_{stg}	storage temperature			–55	+150	°C
$T_{reflow(peak)}$	peak reflow temperature	$t_p \leq 10$ s		-	260	°C
T_{amb}	ambient temperature			–30	+85	°C

[1] All pins to ground.

[2] IP4309CX9 is qualified to 1000 contact discharges of ±15 kV using the IEC 61000-4-2 model, far exceeding the specified IEC 61000-4-2, level 4 (8 kV contact discharge).

6. Characteristics

Table 4. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$C_{(I/O-GND)}$	input/output to ground capacitance	V_I = 0.5 V; f = 1 MHz	[1][2]	1.0	1.3	1.5	pF
I_{LR}	reverse leakage current	V_I = 3 V	[2]	-	-	50	nA
V_{BRzd}	Zener diode breakdown voltage	I_{test} = 1 mA		6	-	11	V
V_F	forward voltage			-	0.7	-	V
R_{dyn}	dynamic resistance	I = 1 A	[3]				
		positive transient		-	0.45	-	Ω
		negative transient		-	0.5	-	Ω

[1] Guaranteed by design.

[2] Pins A1, A2, A3, B1, B3, C1 and C2 to ground.

[3] According to IEC 61000-4-5 and IEC 61000-4-9.

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7. Application information

7.1 Insertion loss

The IP4309CX9 is mainly designed as an ESD protection device for high-speed interfaces such as HDMI, DVI and USB data lines etc.

The insertion loss in a 50 Ω NetWork Analyzer (NWA) of two channels of IP4309CX9 is depicted in Figure 4. The other channels behave similar as all channels contain an identical electrical circuitry.

The insertion loss measurement configuration of a typical 50 Ω NWA system for evaluation of the IP4309CX9 is shown in Figure 3. It was measured using a test Printed-Circuit Board (PCB) utilizing laser-drilled micro-via holes that connect the PCB ground plane to the ground pins.

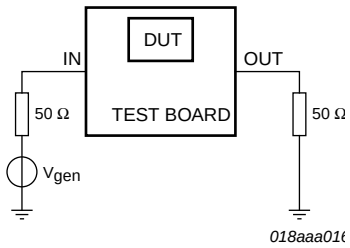
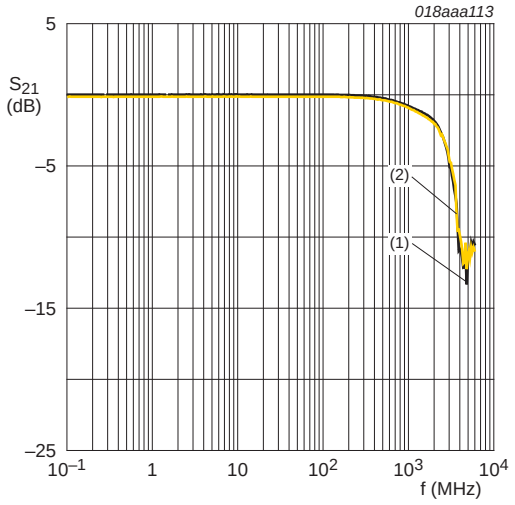


Fig 3. Frequency response setup



(1) Pin A1

(2) Pin A2

Fig 4. Typical IP4309CX9 frequency response curves

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7.2 Crosstalk

The setup for crosstalk measurements in a 50 Ω NWA system for several pin combinations reflecting the various possible physical distances is shown in Figure 5.

The crosstalk measurement results are depicted in Figure 6. Other combinations behave similar, depending on the distance between the pins.

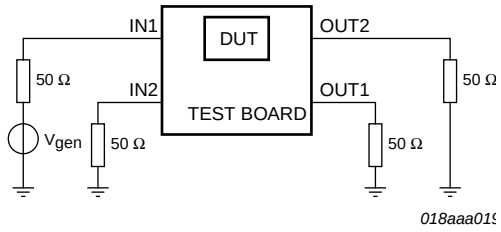
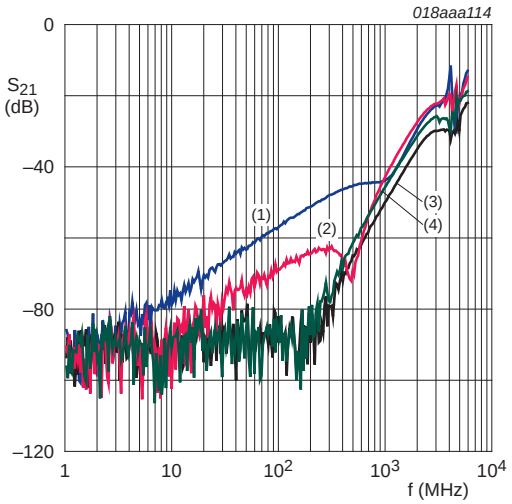


Fig 5. Crosstalk measurement configuration



(1) Pin A1 to A2
(2) Pin A1 to B1
(3) Pin A1 to C3
(4) Pin A1 to A3

Fig 6. Typical IP4309CX9 crosstalk behavior

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8. Package outline

WLCSP9: wafer level chip-size package; 9 bumps (3 x 3)

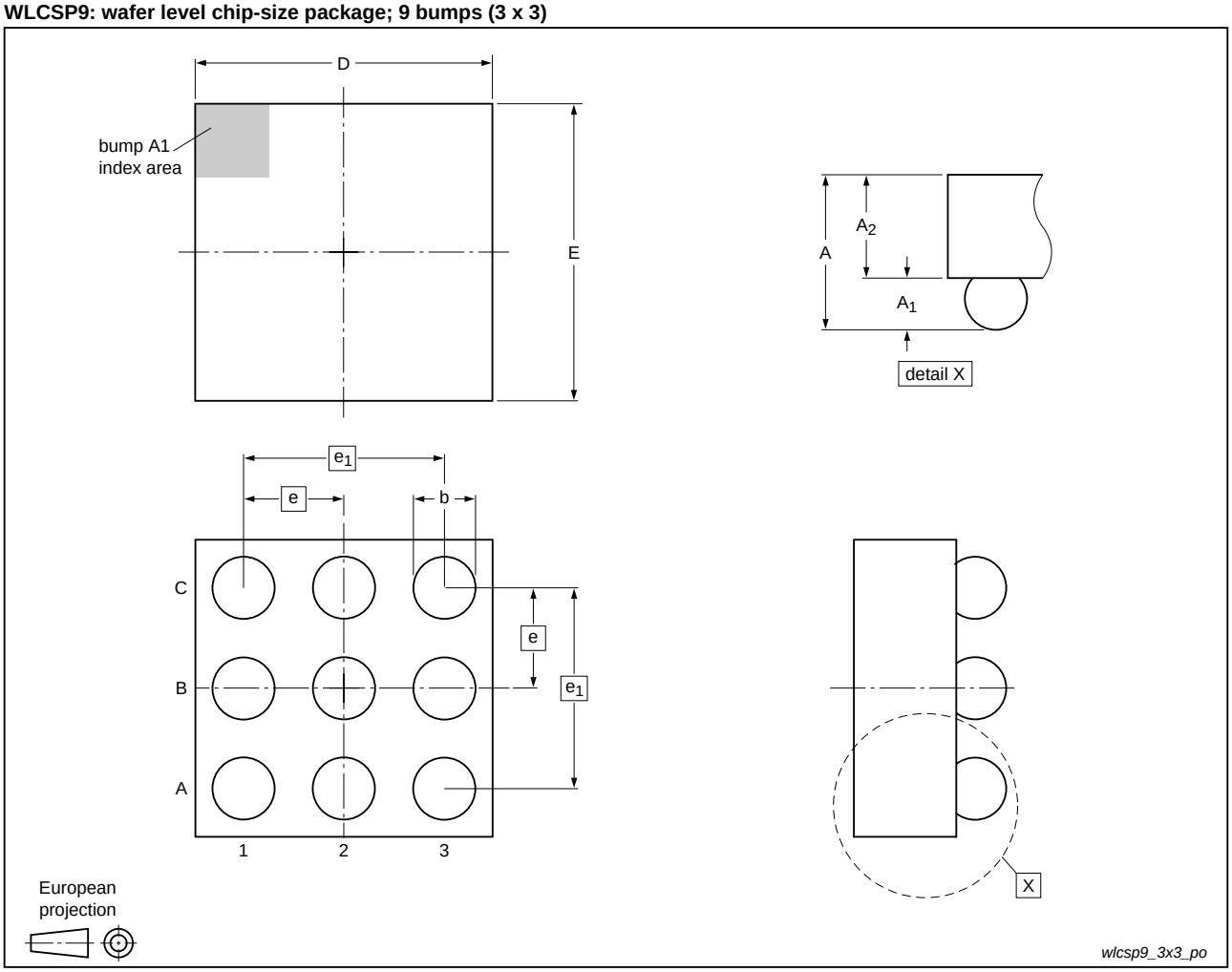


Fig 7. Package outline WLCSP9 (IP4309CX9)

Table 5. Package outline dimensions

Symbol	Min	Typ	Max	Unit
A	0.57	0.61	0.65	mm
A_1	0.18	0.20	0.22	mm
A_2	0.59	0.61	0.63	mm
b	0.21	0.26	0.31	mm
D	1.11	1.16	1.21	mm
E	1.11	1.16	1.21	mm
e	-	0.40	-	mm
e_1	-	0.8	-	mm

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9. Packing information

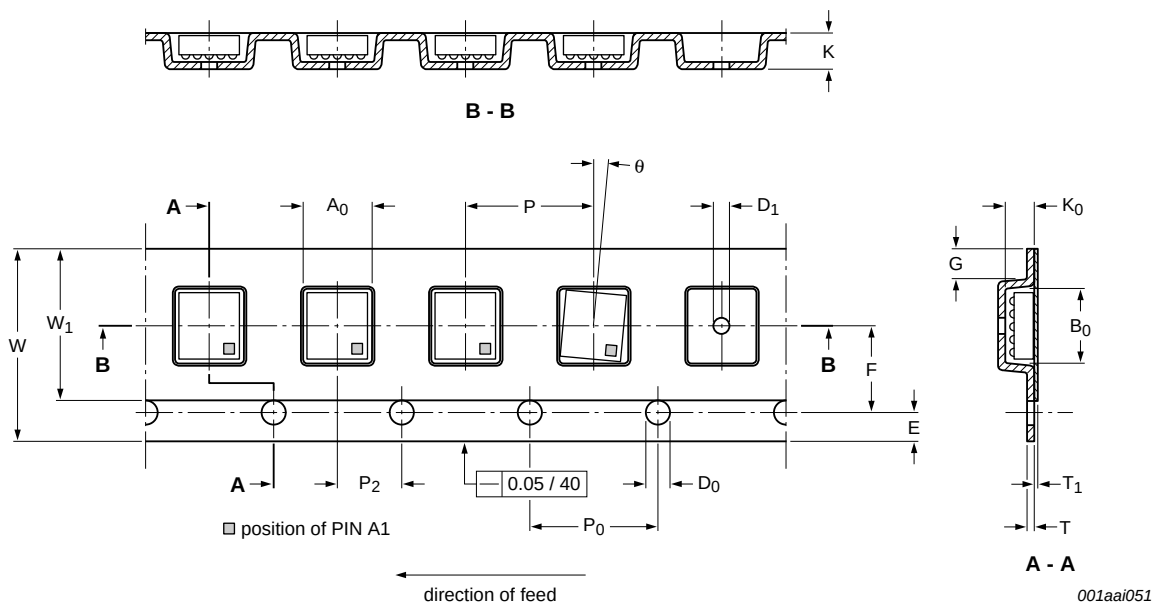


Fig 8. Tape and reel information

Table 6. Tape dimensions

Description	Item	Symbol	Specification (mm)	
			Dimension	Tolerance
Overall dimensions	tape width	W	8.00	±0.1
	thickness	K	1.20	max
	distance	G	0.75	min
Sprocket holes[1]	diameter	D_0	1.50	+0.1
	distance	E	1.75	±0.1
	pitch	P_0	4.00	±0.1
Distance between center lines	length direction	P_2	2.00	±0.05
	width direction	F	3.50	±0.05
Compartments	length	A_0	1.32	±0.05
	width	B_0	1.28	±0.05
	depth	K_0	0.80	±0.05
	hole diameter	D_1	0.50	+0.1
	pitch	P	4.00	±0.1

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Table 6. Tape dimensions *…continued*

Description	Item	Symbol	Specification (mm)	
			Dimension	Tolerance
Device	rotation	θ	20°	max
Carrier tape antistatic[2]	film thickness	T	0.25	±0.07
Cover tape[3]	width	W_1	5.75	max
	film thickness	T_1	0.1	max
Bending radius	in winding direction	R	30	min

[1] Cumulated pitch error: ±0.2 mm per 10 pitches.

[2] Carbon-loaded polystyrene 100 % recyclable.

[3] The cover tape shall not overlap the sprocket holes.

10. Design and assembly recommendations

10.1 PCB design guidelines

It is recommended, for optimum performance, to use a Non-Solder Mask Defined (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. Refer to Table 7 for the recommended PCB design parameters.

Table 7. Recommended PCB design parameters

Parameter	Value or specification
PCB pad diameter	250 μm
Micro-via diameter	100 μm (0.004 inch)
Solder mask aperture diameter	325 μm
Copper thickness	20 μm to 40 μm
Copper finish	AuNi
PCB material	FR4

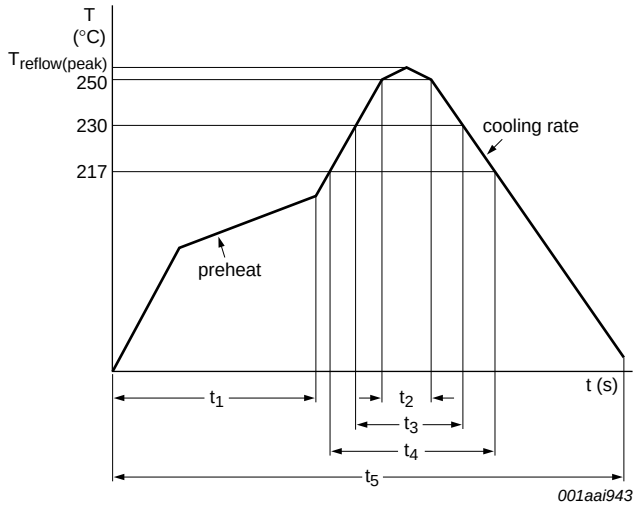
10.2 PCB assembly guidelines for Pb-free soldering

Table 8. Assembly recommendations

Parameter	Value or specification
Solder screen aperture diameter	325 μm
Solder screen thickness	100 μm (0.004 inch)
Solder paste: Pb-free	SnAg (3 % to 4 %); Cu (0.5 % to 0.9 %)
Solder to flux ratio	50 : 50
Solder reflow profile	see Figure 9

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The device is capable of withstanding at least three reflows of this profile.

Fig 9. Pb-free solder reflow profile

Table 9. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{reflow(peak)}$	peak reflow temperature		230	-	260	°C
t_1	time 1	soak time	60	-	180	s
t_2	time 2	time during T ≥ 250 °C	-	-	30	s
t_3	time 3	time during T ≥ 230 °C	10	-	50	s
t_4	time 4	time during T > 217 °C	30	-	150	s
t_5	time 5		-	-	540	s
dT/dt	rate of change of temperature	cooling rate	-	-	–6	°C/s
		preheat	2.5	-	4.0	°C/s

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11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4309CX9 v.1	20110310	Product data sheet	-	-

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