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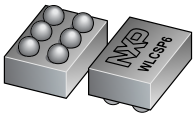
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IP4047CX6

Dual channel integrated passive filter network with ESD protection

Rev. 2 — 1 September 2014 Product data sheet

1. Product profile

1.1 General description

The IP4047CX6 is a low ohmic, dual-channel RC low-pass filter array which is designed to provide filtering of undesired RF signals. In addition, the IP4047CX6 incorporates diodes to provide protection to downstream components from ElectroStatic Discharge (ESD) voltages as high as ±15 kV contact, according to the IEC 61000-4-2 standard, far exceeding the level 4. The IP4047CX6 is fabricated using monolithic silicon technology and integrates two resistors and four pairs of back-to-back diodes in a single Wafer-Level Chip-Scale Package (WLCSP). These features make the IP4047CX6 ideal for use in applications requiring the utmost in miniaturization such as mobile phone handsets, cordless telephones and personal digital devices.

1.2 Features and benefits

- 2-channel integrated π-type RC-filter network
- Downstream ESD protection of ±15 kV contact according to IEC 61000-4-2 ESD model, far exceeding level 4
- 0.95 Ω series resistance; 280 pF channel capacitance
- WLCSP with 0.5 mm pitch

1.3 Applications

Audio line EMI-filtering and ESD protection in:

- Cellular and PCS mobile handsets
- Cordless telephones

2. Pinning information

2.1 Pinning

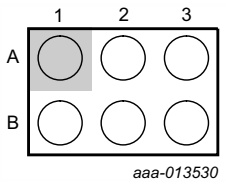


Fig 1. Pin configuration IP4047CX6

2.2 Pin description

Table 1. Pinning

Pin	Description
A1	filter channel 1 input
A2	ground
A3	filter channel 2 input
B1	filter channel 1 output
B2	ground
B3	filter channel 2 output

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP4047CX6/LF	WLCSP6	wafer level chip-size package; 6 bumps (3 × 2)	-

4. Marking

IP4047CX6 is laser-marked with the following information (see Figure 2):

- A marker indicating the pin A1 position.
- Two lines of characters or numbers:
  - The first line (placeholder <marking code>) indicates the marking code. Mapping of product type number to marking code is given in Table 3.
  - The second line (placeholder <lot ID>) indicates the production lot. This information enables tracking a device down to a particular production date.

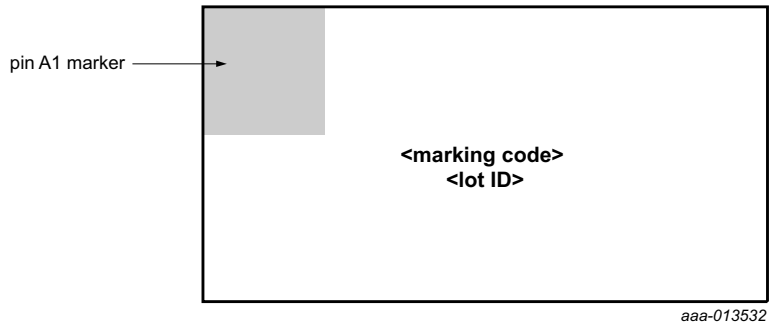


Fig 2. IP4047CX6: outline of marking

Table 3. Marking code

Type number	Marking code
IP4047CX6/LF	47

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5. Functional diagram

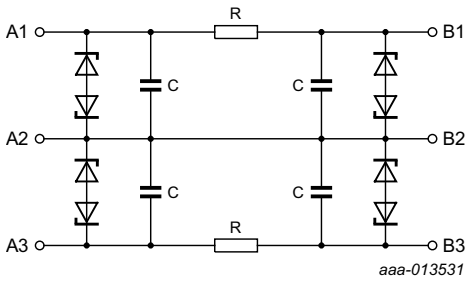


Fig 3. Schematic diagram IP4047CX6

6. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage		–6	+6	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4; all pins to ground			
		contact discharge [1]	–15	+15	kV
		air discharge	–15	+15	kV
P_{ch}	channel power dissipation	T_{amb} = 85 °C	-	70	mW
P_{tot}	total power dissipation	T_{amb} = 85 °C	-	150	mW
T_{stg}	storage temperature		–65	+150	°C
$T_{reflow(peak)}$	peak reflow temperature	10 s maximum	-	260	°C
T_{amb}	ambient temperature		–40	+85	°C

[1] Device is tested with 1000 pulses of ±15 kV contact discharges each, according to the IEC 61000-4-2 model and far exceeds the specified level 4 (8 kV contact discharge).

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7. Characteristics

Table 5. Electrical characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{s(ch)}$	channel series resistance		0.76	0.95	1.14	Ω
C_{ch}	channel capacitance	V = 0 V; f = 100 kHz	224	280	336	pF
V_{BR}	breakdown voltage	positive direction; I_{test} = +1 mA	6	-	12	V
		negative direction; I_{test} = −1 mA	−12	-	−6	V
I_{LR}	reverse leakage current	per channel; V = +3 V	-	-	+1	μA
		per channel; V = −3 V	−1	-	-	μA

Table 6. Frequency response

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_{il}	insertion loss	R_{gen} = 50 Ω; R_L = 50 Ω; 800 MHz < f_i < 2 GHz	−28	-	-	dB
		R_{gen} = 50 Ω; R_L = 5 Ω; 800 MHz < f_i < 2 GHz	−19	-	-	dB

8. Application information

8.1 Insertion loss

The setup for measuring insertion loss in a 50 Ω system is shown in Figure 4.

The insertion loss in a 50 Ω system for the two channels of the IP4047CX6 is shown in Figure 5. The insertion loss is measured on a single die mounted on an RF PCB. Unused pins are connected to ground with 50 Ω.

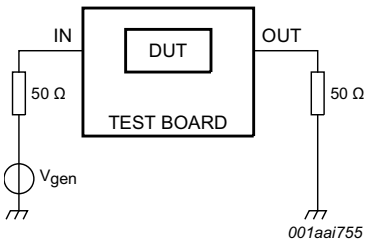


Fig 4. Frequency response measurement configuration

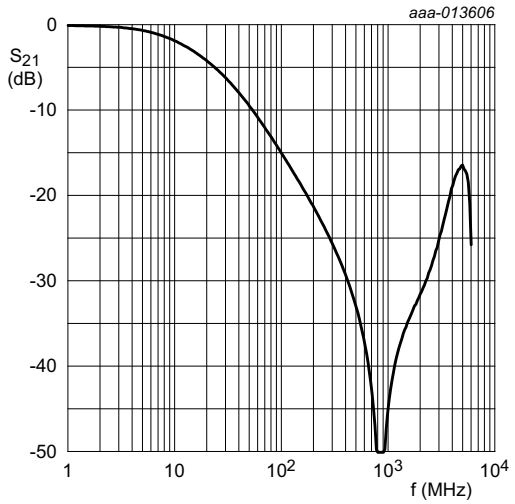


Fig 5. Measured insertion loss magnitude

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9. Package outline

WLCSP6: wafer level chip-size package; 6 bumps (3 x 2)

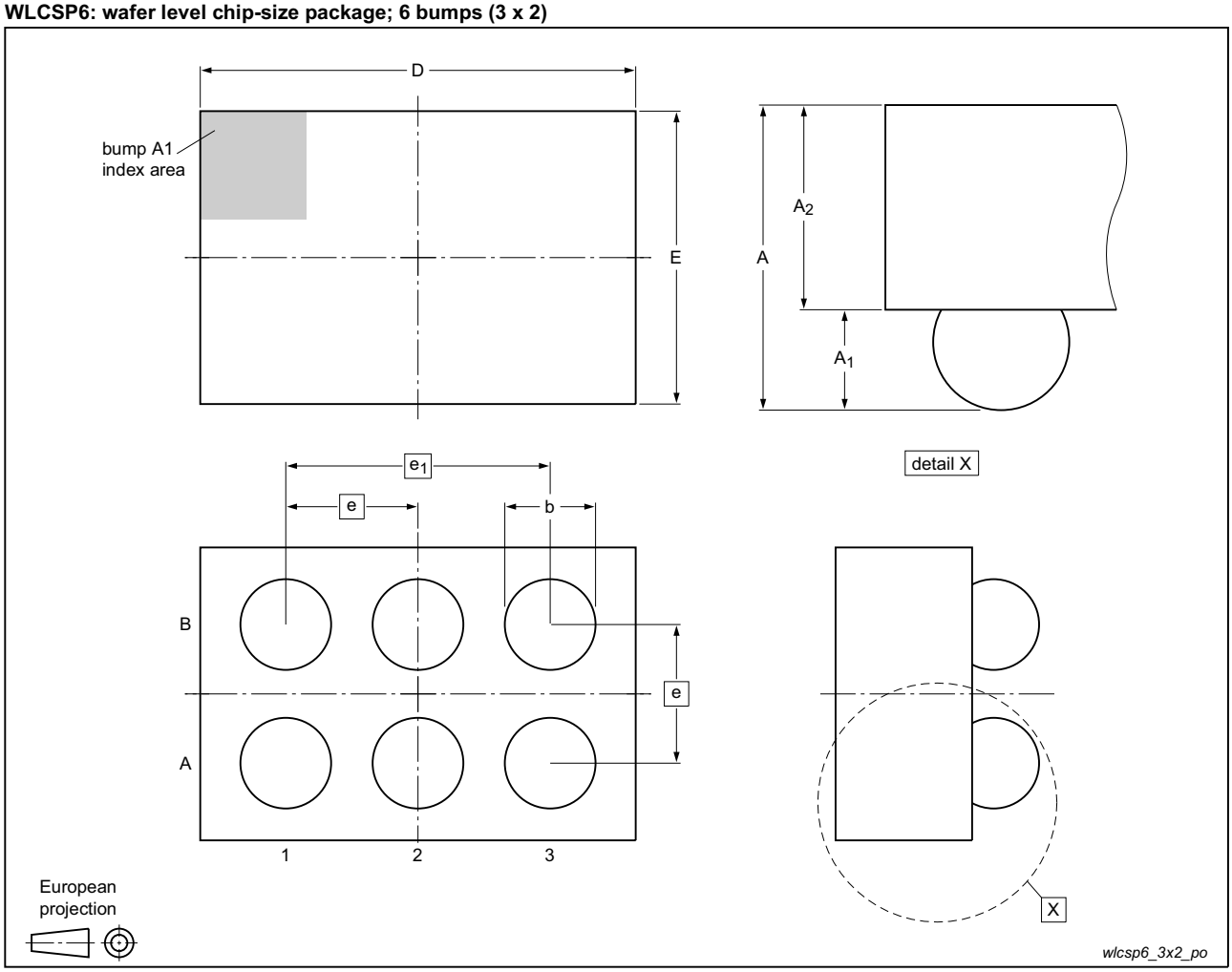


Fig 6. Package outline WLCSP6

Table 7. Dimensions for Figure 6

Symbol	Min	Typ	Max	Unit
A	0.60	0.65	0.70	mm
A_1	0.22	0.24	0.26	mm
A_2	-	0.41	-	mm
b	0.27	0.32	0.37	mm
D	1.39	1.44	1.49	mm
E	0.94	0.99	1.04	mm
e	-	0.5	-	mm
e_1	-	1.0	-	mm

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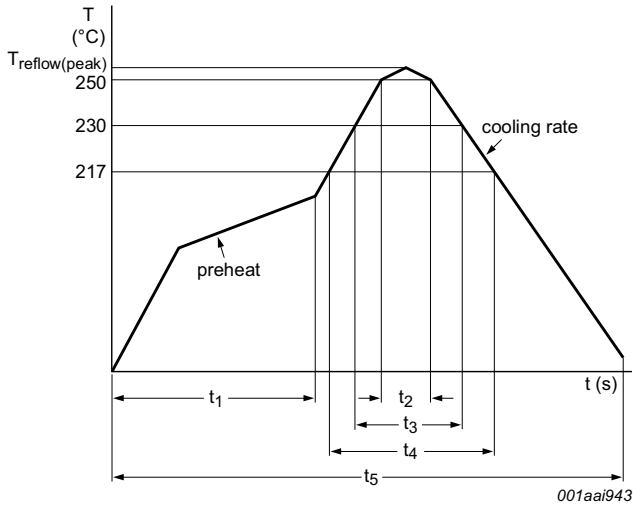
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10. Soldering

10.1 PCB assembly guidelines for Pb-fee soldering

Table 8. Assembly recommendations

Parameter	Value or specification
Solder screen aperture diameter	330 μm
Solder screen thickness	100 μm (0.004 inch)
Solder paste: Pb-free	SnAg (3 % to 4 %); Cu (0.5 % to 0.9 %)
Solder to flux ratio	50 : 50
Solder reflow profile	see Figure 7



The device can withstand at least three reflows of this profile.

Fig 7. Pb-free solder reflow profile

Table 9. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{reflow(peak)}$	peak reflow temperature		230	-	260	°C
t_1	time 1	soak time	60	-	180	s
t_2	time 2	time during T ≥ 250 °C	-	-	30	s
t_3	time 3	time during T ≥ 230 °C	10	-	50	s
t_4	time 4	time during T > 217 °C	30	-	150	s
t_5	time 5		-	-	540	s
dT/dt	rate of change of temperature	cooling rate	-	-	−6	°C/s
		preheat	2.5	-	4.0	°C/s

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11. Mounting

11.1 PCB design guidelines

For the optimum performance, a PCB Non-Solder Mask Design (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer is recommended. This connection results in the lowest possible ground inductance and provides the best high frequency and ESD performance. For this case, the following are the recommended PCB design parameters.

Table 10. Recommended PCB design parameters

Parameter	Value or specification
PCB pad diameter	200 μm
Micro-via diameter	100 μm (0.004 inch)
Solder mask aperture diameter	370 μm
Copper thickness	20 μm to 40 μm
Copper finish	AuNi
PCB material	FR4

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
FR4	Flame Retard 4
NSMD	Non-Solder Mask Design
PCB	Printed-Circuit Board
PCS	Personal Communication System
WLCSP	Wafer-Level Chip-Scale Package

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13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4047CX6 v.2	20140901	Product data sheet	-	IP4047CX6_LF v.1
Modifications:	• Package dimensions D and E corrected			
IP4047CX6_LF v.1	20080606	Product data sheet	-	-

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14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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