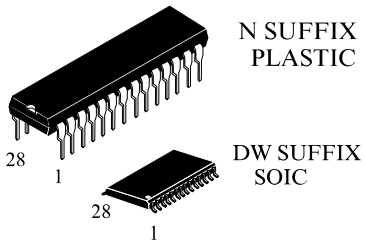
INFRARED REMOTE CONTROL TRANSMITTER (RC-5)

GENERAL DESCRIPTION

The INA3010 is intended as a general purpose (RC-5) infrared remote control system for use where a low voltage supply and a large debounce time are expected. The device can generate 2048 different commands and utilizes a keyboard with a single pole switch for each key. The command are arranged so that 32 systems can be addressed, each system containing 64 different commands. The keyboard interconnection is illustrated by Fig.1.



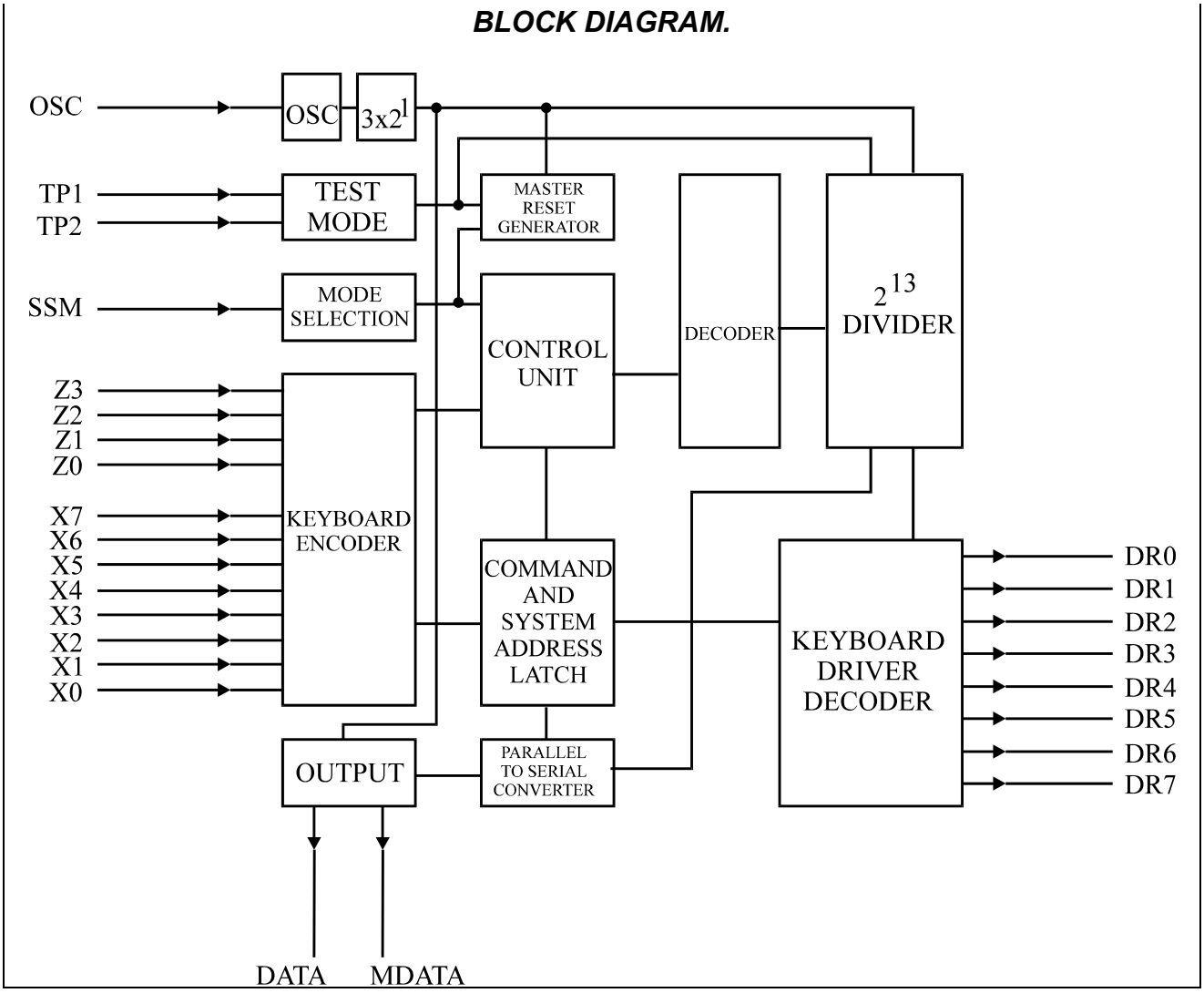
ORDERING INFORMATION

INA3010N Plastic
INA3010DW SOIC
T_A = -25° to 85° C
for all packages

FEATURES

- Low voltage requirement
- Single pin oscillator
- Biphase transmission technique
- Test mode facility

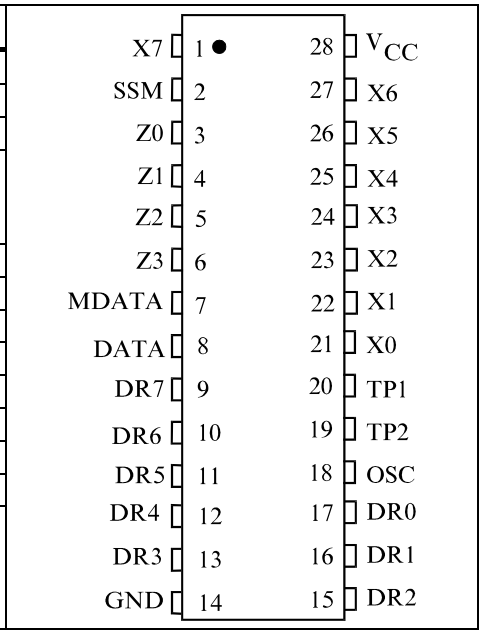
BLOCK DIAGRAM.



INTEGRAL

PINNING

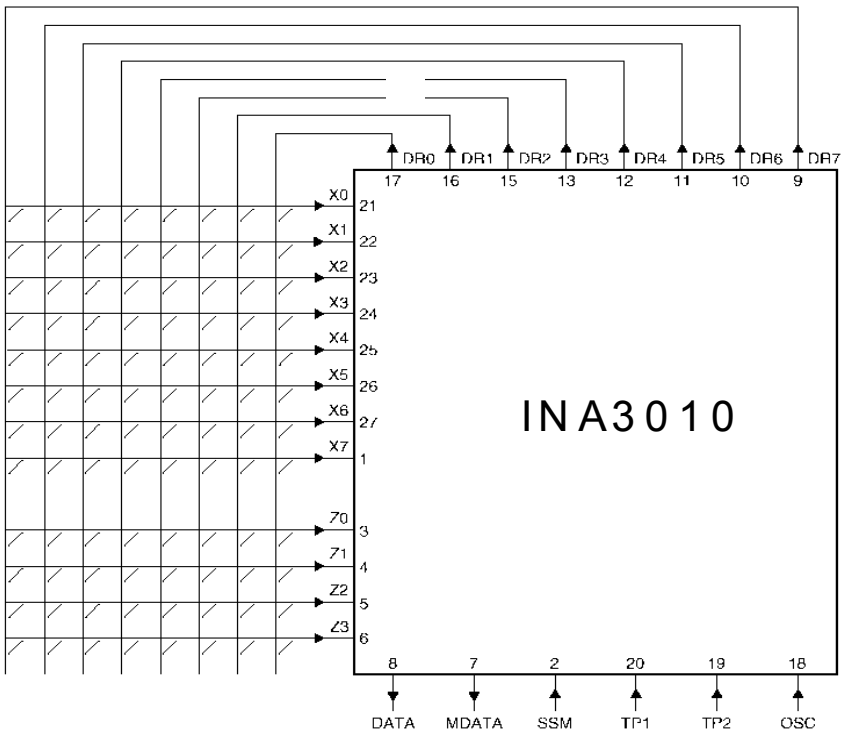
PIN No	DESIGNATION	DESCRIPTION
1	X7 (IPU)	sense input from key matrix
2	SSM (I)	system mode selection input
3-6	Z0-Z3 (IPU)	sense inputs from key matrix
7	MDATA (OP3)	generated output data modulated with 1/2 the oscillator frequency at a 25% duty factor
8	DATA (OP3)	generated output information
9-13	DR7-DR3 (ODN)	scan drivers
14	GND	ground (0V)
15-17	DR2-DR0 (ODN)	scan drivers
18	OSC (I)	oscillator input
19	TP2 (I)	test point 2
20	TP1 (I)	test point 1
21-27	X0-X6 (IPU)	sense inputs from key matrix
28	Vcc (I)	voltage supply



Note

(I) = input
(IPU) = input with p-channel pull-up transistor
(ODN) = output with open drain n-channel transistor
(OP3) = output 3-state

KEYBOARD INTERCONNECTION.



INTEGRAL

FUNCTIONAL DESCRIPTION

Keyboard operation

Every connection of one X-input and one DR-output will be recognized as a legal key operation and will cause the device to generate the corresponding code. The same applies to every connection of one Z-input to one DR-output with the7 proviso that SSM must be LOW. When SSM is HIGH a wired connection must exist between a Z-input and a DR-output. If no connection is present the system number will not be generated. Activating two or more X-inputs, Z-inputs or Z-inputs and X-inputs at the same time is an illegal action and inhibits further activity (oscillator will not start).
When one X- or Z-input is connected to more than one DR-output, the last scan signal will be considered as legal.
The maximum value of the contact series resistance of the switched keyboard is 7 kW.

Inputs

In the quiescent state the command inputs X0 to X7 are held HIGH by an internal pull-up transistor. When the system mode selection (SSM) input is LOW and the system is quiescent, the system inputs Z0 to Z3 are also held HIGH by an internal pull-up transistor. When SSM is HIGH the pull-up transistor for the Z-inputs is switched off, in order to prevent current flow, and a wired connection in the Z-DR matrix provides the system number.

Outputs

The output signal DATA transmits the generated information in accordance with the format illustrated by Fig.3. The code is transmitted using a biphase technique as illustrated by Fig.4. The code consists of four parts:

· Start part -1.5 bits (2 ´ logic 1)
· Control part -1 bit
· System part -5 bits
· Command part -6 bits

The output signal MDATA transmits the generated information modulated by 1/12 of the oscillator frequency with a 50%
duty factor.
In the quiescent state both DATA and MDATA are non-conducting (3-state outputs).
The scan driver outputs DR0 to DR7 are open drain n-channel transistors and conduct when the circuit is quiescent. After a legal key operation the scanning cycle is started and the outputs switched to the conductive state one by one. The DR-outputs were switched off at the end of the preceding debounce cycle.

Command matrix (X-DR)

Code	X-lines								DR-lines								Command bits					
no.	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
0	x								x								0	0	0	0	0	0
1	x									x							0	0	0	0	0	1
2	x										x						0	0	0	0	1	0
3	x											x					0	0	0	0	1	1
4	x												x				0	0	0	1	0	0
5	x													x			0	0	0	1	0	1
6	x														x		0	0	0	1	1	0
7	x															x	0	0	0	1	1	1
8		x							x								0	0	1	0	0	0
9		x								x							0	0	1	0	0	1
10		x									x						0	0	1	0	1	0
11		x										x					0	0	1	0	1	1

Code	X-lines								DR-lines								Command bits					
no.	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	5	4	3	2	1	0
12		x											x				0	0	1	1	0	0
13		x												x			0	0	1	1	0	1
14		x													x		0	0	1	1	1	0
15		x														x	0	0	1	1	1	1
16			x						x								0	1	0	0	0	0
17			x							x							0	1	0	0	0	1
18			x								x						0	1	0	0	1	0
19			x									x					0	1	0	0	1	1
20			x										x				0	1	0	1	0	0
21			x											x			0	1	0	1	0	1
22			x												x		0	1	0	1	1	0
23			x													x	0	1	0	1	1	1
24				x					x								0	1	1	0	0	0
25				x						x							0	1	1	0	0	1
26				x							x						0	1	1	0	1	0
27				x								x					0	1	1	0	1	1
28				x									x				0	1	1	1	0	0
29				x										x			0	1	1	1	0	1
30				x											x		0	1	1	1	1	0
31				x												x	0	1	1	1	1	1
32					x				x								1	0	0	0	0	0
33					x					x							1	0	0	0	0	1
34					x						x						1	0	0	0	1	0
35					x							x					1	0	0	0	1	1
36					x								x				1	0	0	1	0	0
37					x									x			1	0	0	1	0	1
38					x										x		1	0	0	1	1	0
39					x											x	1	0	0	1	1	1
40						x			x								1	0	1	0	0	0
41						x				x							1	0	1	0	0	1
42						x					x						1	0	1	0	1	0
43						x						x					1	0	1	0	1	1
44						x							x				1	0	1	1	0	0
45						x								x			1	0	1	1	0	1
46						x									x		1	0	1	1	1	0
47						x										x	1	0	1	1	1	1
48							x		x								1	1	0	0	0	0
49							x			x							1	1	0	0	0	1
50							x				x						1	1	0	0	1	0
51							x					x					1	1	0	0	1	1
52							x						x				1	1	0	1	0	0
53							x							x			1	1	0	1	0	1
54							x								x		1	1	0	1	1	0
55							x									x	1	1	0	1	1	1
56								x	x								1	1	1	0	0	0
57								x		x							1	1	1	0	0	1
58								x			x						1	1	1	0	1	0
59								x				x					1	1	1	0	1	1
60								x					x				1	1	1	1	0	0
61								x						x			1	1	1	1	0	1
62								x							x		1	1	1	1	1	0
63								x								x	1	1	1	1	1	1

System matrix (Z-DR)

Code	X-lines								DR-lines								System bits				
no.	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	4	3	2	1	0
0	x								x								0	0	0	0	0
1	x									x							0	0	0	0	1
2	x										x						0	0	0	1	0
3	x											x					0	0	0	1	1
4	x												x				0	0	1	0	0
5	x													x			0	0	1	0	1
6	x														x		0	0	1	1	0
7	x															x	0	0	1	1	1
8		x							x								0	1	0	0	0
9		x								x							0	1	0	0	1
10		x									x						0	1	0	1	0
11		x										x					0	1	0	1	1
12		x											x				0	1	1	0	0
13		x												x			0	1	1	0	1
14		x													x		0	1	1	1	0
15		x														x	0	1	1	1	1
16			x						x								1	0	0	0	0
17			x							x							1	0	0	0	1
18			x								x						1	0	0	1	0
19			x									x					1	0	0	1	1
20			x										x				1	0	1	0	0
21			x											x			1	0	1	0	1
22			x												x		1	0	1	1	0
23			x													x	1	0	1	1	1
24				x					x								1	1	0	0	0
25				x						x							1	1	0	0	1
26				x							x						1	1	0	1	0
27				x								x					1	1	0	1	1
28				x									x				1	1	1	0	0
29				x										x			1	1	1	0	1
30				x											x		1	1	1	1	0
31				x												x	1	1	1	1	1

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +8.5	V
V_{IN}	DC Input Voltage (Referenced to GND)*	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)*	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current	±10	mA
I_{OUT}	DC Output Current	±10	mA
P_{DO} P_{DO}	Maximum Power Dissipation OSC output other outputs	 50 100	 mW mW
P_D	Power Dissipation in Still Air	200	mW
Tstg	Storage Temperature	-65 to +150	°C

*V_{CC} + 0.5 must not exceeed 9.0V..

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 85°C
SOIC Package: : - 7 mW/°C from 65° to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply voltage (Reference to GND)	2.0	7.0	V
V_{IH}	DC Input voltage (HIGH)	0.7V_{CC}	V_{CC}	V
V_{IL}	DC Input voltage (LOW)	0	0.3V_{CC}	V
V_{OUT}	DC Output Voltage (MDATA, DATA)	-	7.0	V
I_{IN}	DC Input Current	-	±10	mA
I_{OL}	DC Output Current (LOW) pins 7,8 pins 9-13; 15-17	-	 0.6 0.3	mA
I_{OH}	DC Output Current (MDATA, DATA)	-	-0.4	mA
T_A	Operating Temperature, All Package Types	-25	85	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltage Reference to GND)
(V_{CC}= 2.0 to 7.0V unless otherwise specified, T_A=-25 to +70°C)

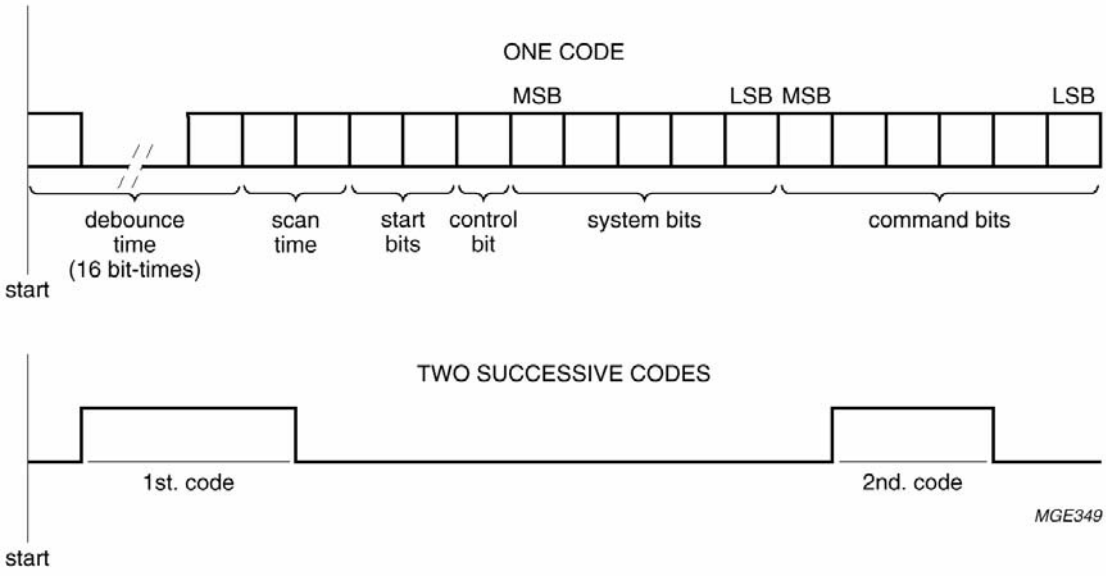
Symbol	Parameter	Test Conditions	Guaranteed Limits		Unit
			Min	Max	
I_{CC}	Quiscent supply current	U_{IL}=0B; V_{IH}=V_{CC} I_{OUT}=0 mA at all outputs		40	μA
INPUTS					
I_{IN}	Input current Pins 01, 03-06; 21-27	V_{IL}=0V	-10	-600	μA
	Pin 18	V_{IL}=0V; V_{IH}=V_{CC}	3.0	33	
I_{LI}	Input leakage current Pins 01-06;19-27	V_{IL}=0V; V_{IH}=V_{CC}	-	±10	μA
	Pin 18		-	-20	
OUTPUTS					
V_{OH}	Output voltage HIGH, pins 07-08	I_{OH}=-0.4mA V_{IL}=0.3 V_{CC}	V_{CC}-0.3	-	V
V_{OL}	Output voltage LOW Pins 07-08	I_{OL}=0.6mA V_{IL}=0V, V_{HI}=0.7V_{CC}	-	0.3	V
	Pins 9-13; 15-17	I_{OL}=0.3mA, V_{IL}=0V, V_{IH}=0.7V_{CC}	-	0.3	V
I_{LO}	Output leakage current Pins 07-13; 15-17	V_O=V_{CC}, V_{IH}=V_{CC}, V_{OH}=V_{CC}	- -	10	μA
I_{LO}	Output leakage current Pins 07-08	V_O=0V, V_{IH}=V_{CC}, V_{OL}=0V	- -	-20	μA
I_{OH}	DC Output Current Pins 9-13; 15-17	V_{IL}=0V; V_{IH}=V_{CC}; V_{OH}=V_{CC}		10	μA

AC ELECTRICAL CHARACTERISTICS

T_A=-25 to +85°C; V_{CC}=2.0 to 7.0 V unless otherwise specified

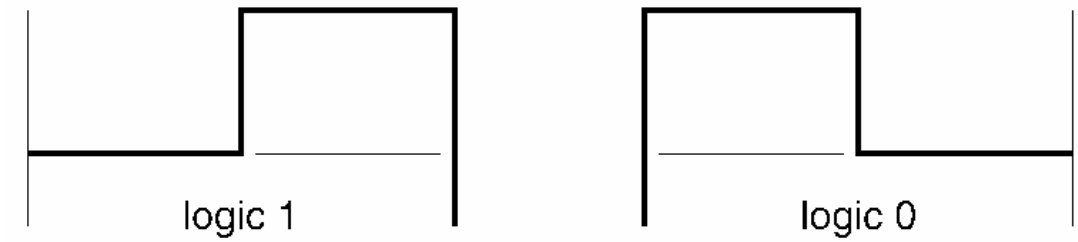
Symbol	Parameter	Test Condition	Guaranteed Limits		Unit
			Typ	Max	
f_{OSC}	Oscillator frequency operational	C_L=160pF	432	450	KHz

DATA OUTPUT FORMAT.



Where:
debounce time + scan time = 18 bit-times
repetition time = 4 ´ 16 bit-times

BIPHASE TRANSMISSION TECHNIQUE.



Where: 1 bit-time = 3.2 8 ´ TOSC = 1.778 ms (typ.)

Combined system mode (SSM is LOW)

The X and Z sense inputs have p-channel pull-up transistors, so that they are HIGH, until pulled LOW by connecting them to an output as the result of a key operation. Legal operation of a key in the X-DR or Z-DR matrix will start the debounce cycle, once key contact has been established for 18 bit-times without interruption, the oscillator enable signal is latched and the key may be released. An interruption within the 18 bit-time period resets the device.

At the end of the debounce cycle the DR-outputs are switched off and two scan cycles are started, that switch on the DR-lines one by one. When a Z- or X-input senses a low level, a latch enable signal is fed to the system (Z-input) or command (X-input) latches.

After latching a system number the device will generate the last command (i.e. all command bits logic 1) in the chosen system for as long as the key is operated. Latching of a command number causes the chip to generate this command together with the system number memorized in the system latch. Releasing the key will reset the device if no data is to be transmitted at the time. Once transmission has started the code will complete to the end.

Single system mode (SSM is HIGH)

In the single system mode, the X-inputs will be HIGH as in the combined system mode. The Z-inputs will be disabled by having their pull-up transistors switched off; a wired connection in the Z-DR matrix provides the system code. Only legal key operation in the X-DR matrix will start the debounce cycle, once key contact has been established for 18 bit-times without interruption the oscillator enable signal is latched and the key may be released. An interruption within the 18 bit-time period resets the internal action.

At the end of the debounce cycle the pull-up transistors in the X-lines are switched off and those in the Z-lines are

switched on for the first scan cycle. The wired connection in the Z-matrix is then translated into a system number and memorized in the system latch. At the end of the first scan cycle the pull-up transistors in the Z-lines are switched off and the inputs are disabled again; the pull-up transistors in the X-lines are switched on. The second scan cycle produces the command number which, after being latched, is transmitted together with the system number.

Key release detection

An extra control bit is added which will be complemented after key release; this indicates to the decoder that the next code is a new command. This is important in the case where more digits need to be entered (channel numbers of Teletext or Viewdata pages). The control bit will only be complemented after the completion of at least one code transmission. The scan cycles are repeated before every code transmission, so that even with “take over” of key operation during code transmission the right system and command numbers are generated.

Reset action

The device will be reset immediately a key is released during:

· debounce time

· between two codes.

When a key is released during matrix scanning, a reset will occur if:

· a key is released while one of the driver outputs is in the low ohmic stage (logic 0)

· a key is released before that key has been detected

· there is no wired connection in the Z-DR matrix when SSM is HIGH.