INA300 Overcurrent-Protection, Current-Sense Comparator

1 Features

- Wide Common-Mode Range: 0 V to 36 V
- Selectable Response Times:
  - 10 µs, 50 µs, 100 µs
- Programmable Threshold:
  - Adjust Using Single Resistor
  - Programmable From 0 mV to 250 mV
- Accuracy:
  - Offset Voltage: ±500 µV (Max)
  - Offset Voltage Drift: 0.5 µV/°C (Max)
- Selectable Hysteresis:
  - 2 mV, 4 mV, 8 mV
- Active Quiescent Current: 135 µA (Max)
- Selectable Disable Mode
  - Disabled Quiescent Current: 3.5 µA (Max)
  - Disabled Input Bias Current: 500 nA (Max)
- Open-Drain Output with Latch Mode Available

2 Applications

- Overcurrent Protection
- Computers
- Servers
- Telecom Equipment
- Power Supplies
- Battery Chargers

3 Description

Designed for overcurrent protection applications, the INA300 is a current-sensing comparator that detects overcurrent by measuring the voltage developed across a shunt resistor, and comparing that voltage to the threshold voltage input level. The device measures this differential voltage signal on common-mode voltages that can vary from 0 V up to 36 V, independent of the supply voltage. The device features an adjustable threshold range that is set using a single external limit-setting resistor. A selectable hysteresis feature enables adjustable operation of the comparator to accommodate the wide input signal range of 0 mV to 250 mV.

An open-drain alert output on the device can be configured to operate in either a transparent mode where the output status follows the input state, or in a latched mode where the alert output is cleared when the latch is cleared. The device response time setting is selectable, which enables overcurrent alerts to be issued in as fast as 10 µs.

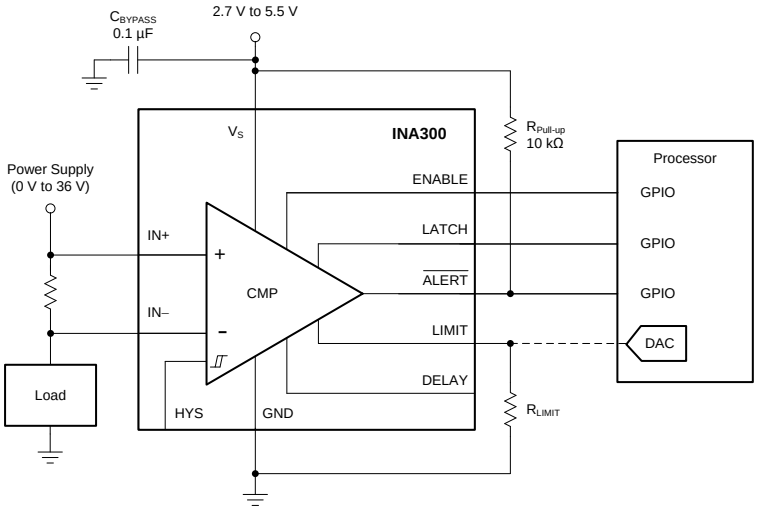
This device operates from a single 2.7-V to 5.5-V supply, drawing a maximum supply current of 135 µA. The device is specified over the extended operating temperature range of –40°C to +125°C, and is available in WSON-10 and VSSOP-10 packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA300	WSON (10)	2.00 mm × 2.00 mm
	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2014) to Revision B — **Page**

- Changed data sheet title ... 1
- Added VSSOP (DGS) package to data sheet ... 1
- Changed text in Description section for clarity ... 1
- Moved storage temperature from Handling Ratings table to Absolute Maximum Ratings table ... 4
- Changed Handling Ratings to ESD Ratings ... 4
- Added DGS data to *Thermal Information* table ... 4

Changes from Original (February 2014) to Revision A — **Page**

- Made changes to product preview data sheet ... 1

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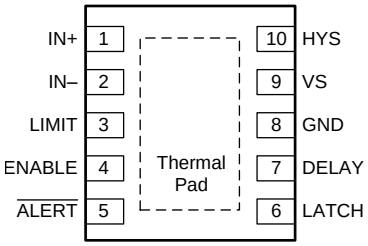
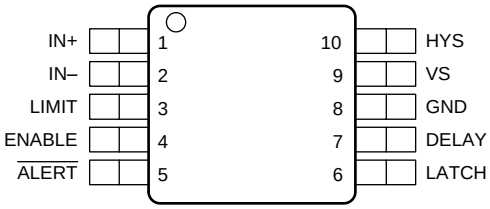
5 Pin Configuration and Functions

DSQ Package
10-Pin WSON
Top View



DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	1	Analog input	Connect to supply side of shunt resistor
IN–	2	Analog input	Connect to load side of shunt resistor
LIMIT	3	Analog input	Alert threshold limit input. See the *Setting The Current-Limit Threshold* section for details on setting limit threshold.
ENABLE	4	Digital input	Enable or disable selection input
ALERT	5	Digital output	Overlimit alert, active-low, open-drain output
LATCH	6	Digital input	Transparent or latch mode selection input
DELAY	7	Digital input	Response time selection input
GND	8	Analog	Ground
VS	9	Analog	Power supply, 2.7 V to 5.5 V
HYS	10	Digital input	Hysteresis setting input. See the *Selectable Hysteresis* section for hysteresis settings.
Thermal pad	DSQ (WSON) package only	—	This pad can be connected to ground or left floating.

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6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_S			6	V
Analog inputs (IN+, IN–)	Differential (V_{IN+}) – ($V_{IN–}$)(2)	–40	40	V
	Common-mode (3)	GND – 0.3	40	
Analog input	LIMIT	GND – 0.3	(V_S) + 0.3	V
Digital inputs	LATCH, DELAY, ENABLE, HYS	GND – 0.3	(V_S) + 0.3	V
Alert output		GND – 0.3	6	V
Operating temperature		–40	125	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and $V_{IN–}$ are the voltages at the IN+ and IN– terminals, respectively.
(3) Input voltage may exceed the voltage shown if the current at that terminal is limited to 5 mA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage		12		V
V_S	Operating supply voltage	2.7	3.3	5.5	V
	Delay setting		100		µs
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA300		UNIT
		DSQ (WSON)	DGS (VSSOP)	
		10 PINS	10 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	63.5	169.4	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	79.5	59.1	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	33.9	89.6	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	7.8	8.5	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	34.3	88.3	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	7.5	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

at T_A = 25°C, V_{SENSE} = V_{IN+} – $V_{IN–}$ = 0 mV, V_S = 3.3 V, V_{IN+} = 12 V, V_{LIMIT} = 10 mV, and DELAY = 100 µs (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{CM}	Common-mode input voltage		0		36	V
V_{IN}	Differential input voltage	V_{IN} = V_{IN+} – $V_{IN–}$	0		250	mV
CMR	Common-mode rejection	V_{IN+} = 0 V to 36 V, T_A= –40ºC to +125ºC	100	120		dB
V_{OS}	Offset voltage, RTI(1)	V_S = 3.3 V, DELAY = 100 µs		–75	–500	µV
		V_S = +3.3 V, DELAY = 50 µs		–125	–500	
		V_S = +3.3 V, DELAY = 10 µs(2)		–350	–650	
dV_{OS}/dT	Offset voltage drift, RTI(1)	T_A= –40ºC to +125ºC		0.1	0.5	µV/°C
PSR	Power-supply rejection ratio	V_S = 2.7 V to 5.5 V, V_{IN+} = 12 V, T_A= –40ºC to +125ºC		75	150	µV/V
I_B	Input bias current			5	10	µA
		Disable mode		0.05	0.5	
I_{OS}	Input offset current			±0.1		µA
I_{LIMIT}	Limit threshold output current	T_A= 25ºC	19.9	20	20.1	µA
		T_A= –40ºC to +125ºC	19.85		20.15	
DIGITAL INPUT/OUTPUT						
t_p	Alert propagation delay	Delay = open, overdrive = 1 mV		10		µs
		Delay = GND, overdrive = 1 mV		50		
		Delay = V_S, overdrive = 1 mV		100		
HYS	Hysteresis	HYS = open		2		mV
		HYS = GND		4		
		HYS = V_S		8		
V_{IH}	High-level input voltage	Latch, enable	1.4		6	V
		Delay, hysteresis	V_S – 0.5		6	
V_{IL}	Low-level input voltage	Latch, enable	0		0.4	V
		Delay, hysteresis	0		0.5	
V_{OL}	Alert low-level output voltage	I_{OL} = 3 mA		50	400	mV
	$\overline{ALERT}$ terminal leakage input current	V_{OH} = 3.3 V		0.1	1	µA
	Digital leakage input current	0 ≤ V_{IN} ≤ V_S		1	2	µA
POWER SUPPLY						
I_Q	Quiescent current	V_{SENSE} = 0 mV, T_A = 25ºC		115	135	µA
		T_A = –40ºC to +125ºC			150	
		V_{SENSE} = 0 mV, disable mode, HYS = 2 mV		2	3.5	

(1) RTI = referred-to-input.
(2) Absolute-maximum values are tested with the threshold limit set using the corresponding noise adjustment factor (NAF) value. See the *Noise Adjustment Factor (NAF)* section for additional information on applying the NAF value.

6.6 Timing Requirements

		MIN	TYP	MAX	UNIT
	Start-up time		1		ms
t_{en}	Enable time		300		µs
t_{dis}	Disable time		20		µs

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6.7 Typical Characteristics

at T_A = 25°C, V_S = 3.3 V, V_{IN+} = 12 V, alert pull-up resistor = 10 kΩ, and Delay = 100 µs (unless otherwise noted)

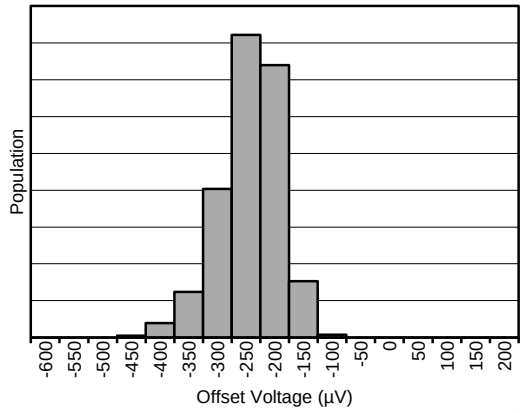

Figure 1. Input Offset Voltage (Delay = 10 µs)

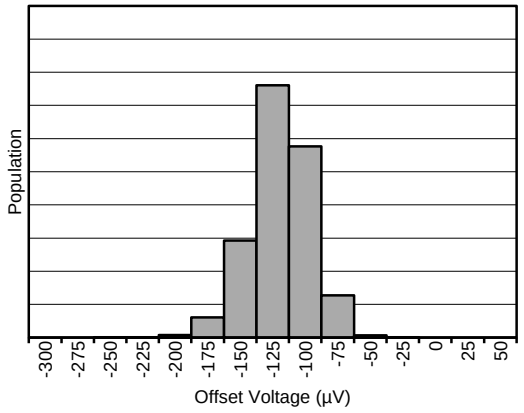

Figure 2. Input Offset Voltage (Delay = 50 µs)

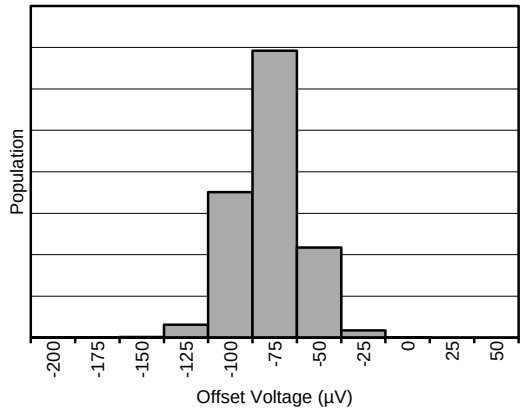

Figure 3. Input Offset Voltage (Delay = 100 µs)

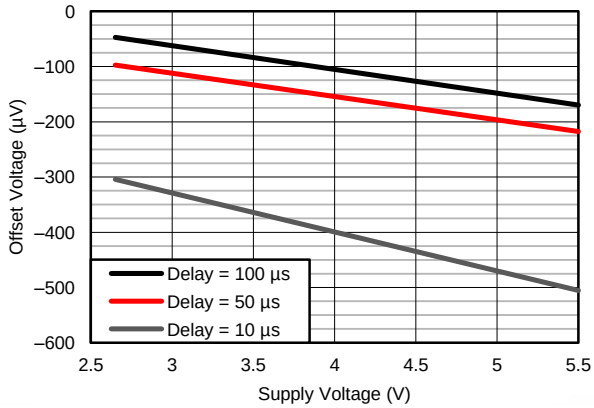

Figure 4. Input Offset Voltage vs Supply Voltage

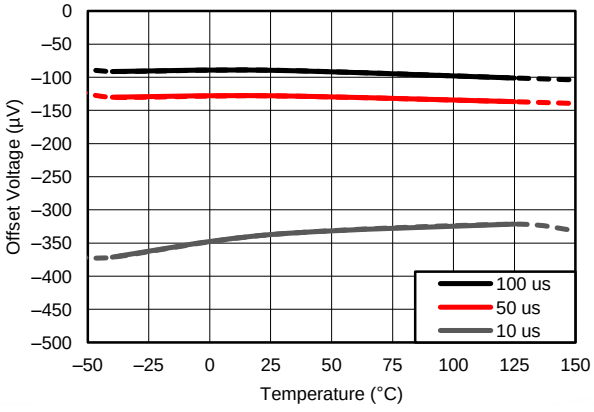

Figure 5. Input Offset Voltage vs Temperature

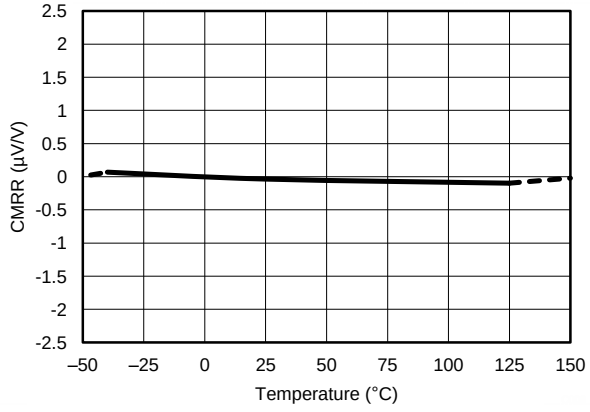

Figure 6. Common-Mode Rejection Ratio vs Temperature

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 3.3 V, V_{IN+} = 12 V, alert pull-up resistor = 10 kΩ, and Delay = 100 µs (unless otherwise noted)

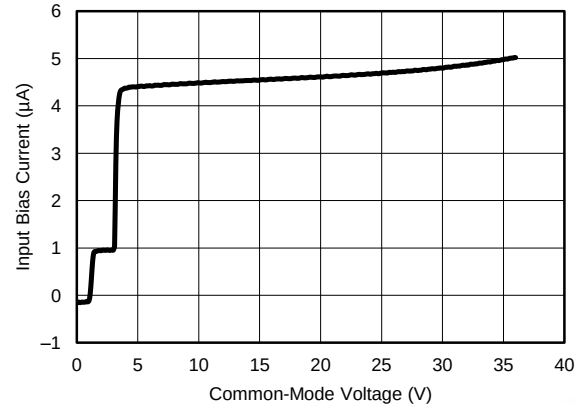

Figure 7. Input Bias Current vs Common-Mode Voltage (Enabled)

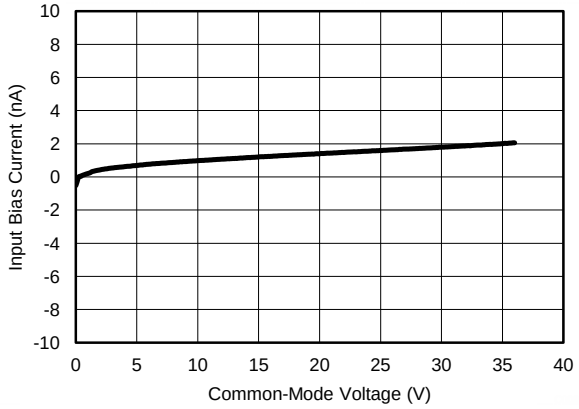

Figure 8. Input Bias Current vs Common-Mode Voltage (Disabled)

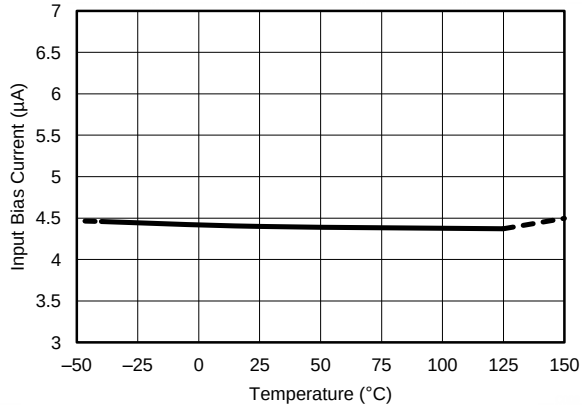

Figure 9. Input Bias Current vs Temperature (Enabled)

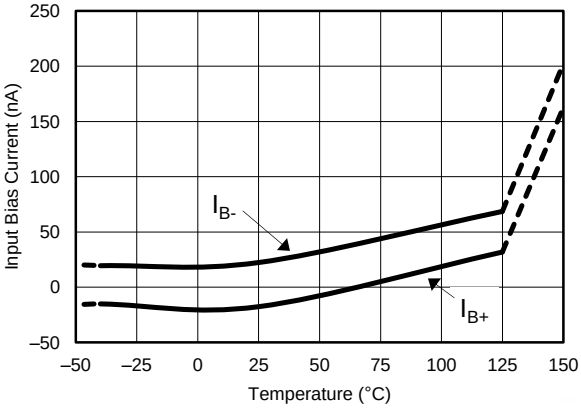

Figure 10. Input Bias Current vs Temperature (Disabled)

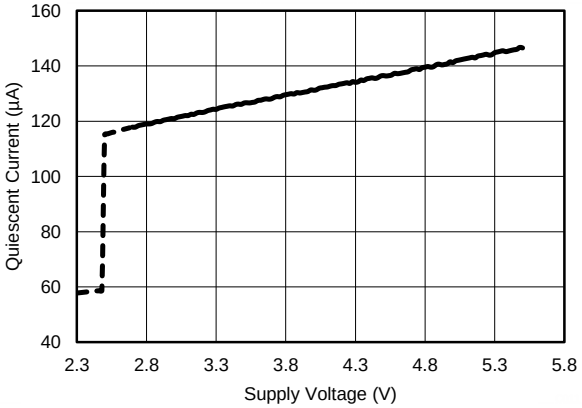

Figure 11. Quiescent Current vs Supply Voltage (Enabled)

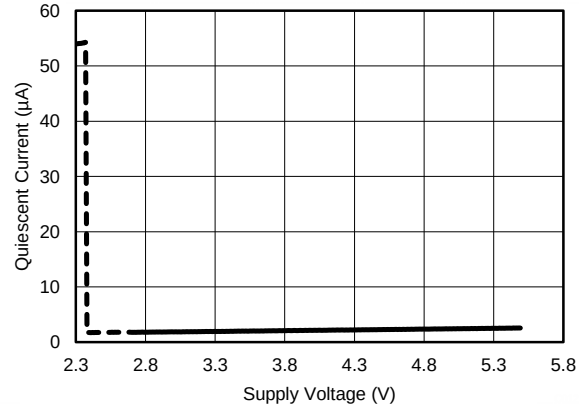

Figure 12. Quiescent Current vs Supply Voltage (Disabled)

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 3.3 V, V_{IN+} = 12 V, alert pull-up resistor = 10 kΩ, and Delay = 100 µs (unless otherwise noted)

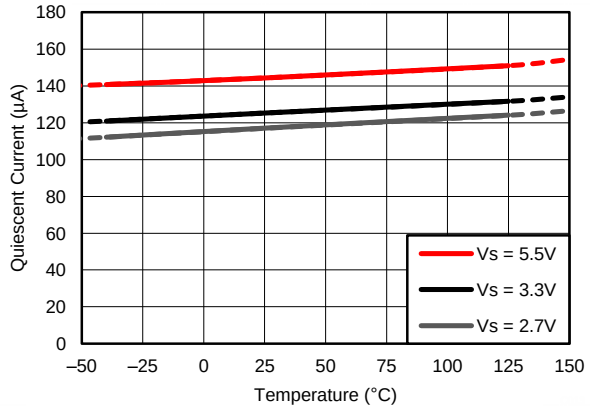

Figure 13. Quiescent Current vs Temperature (Enabled)

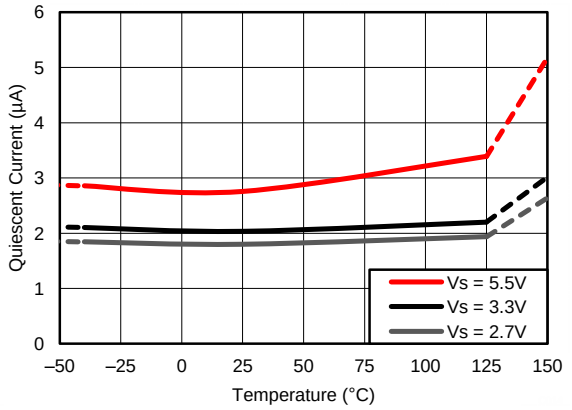

Figure 14. Quiescent Current vs Temperature (Disabled)

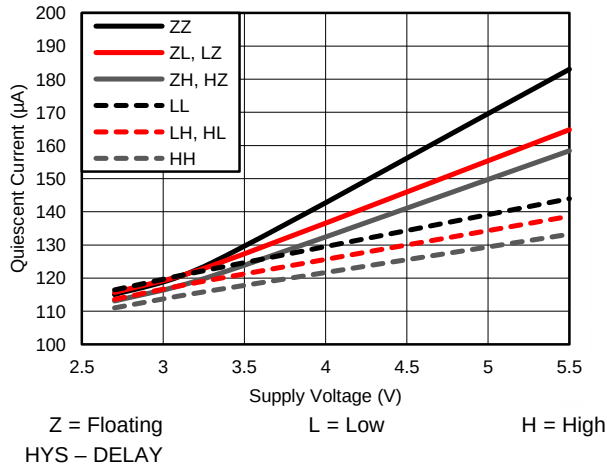

Figure 15. Quiescent Current vs HYS and DELAY Settings (Enabled)

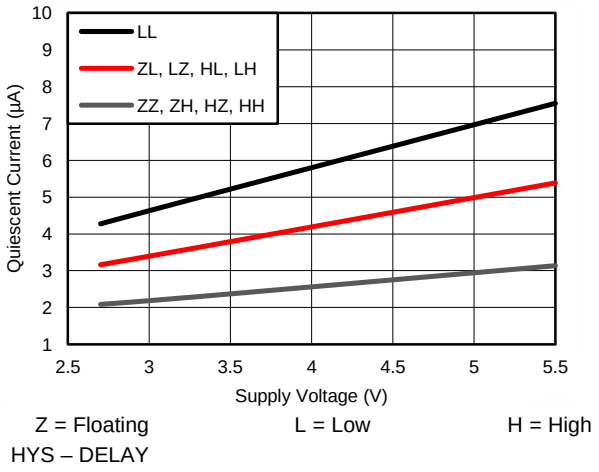

Figure 16. Quiescent Current vs HYS and DELAY Settings (Disabled)

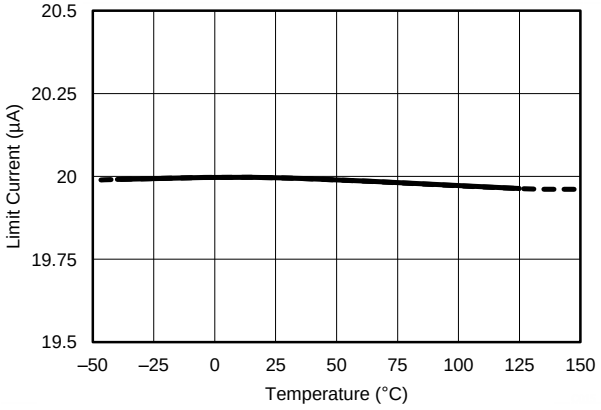

Figure 17. Limit Current Source vs Temperature

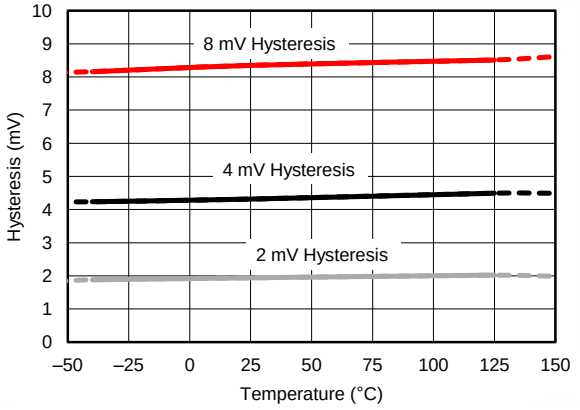

Figure 18. Hysteresis vs Temperature

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 3.3 V, V_{IN+} = 12 V, alert pull-up resistor = 10 kΩ, and Delay = 100 µs (unless otherwise noted)

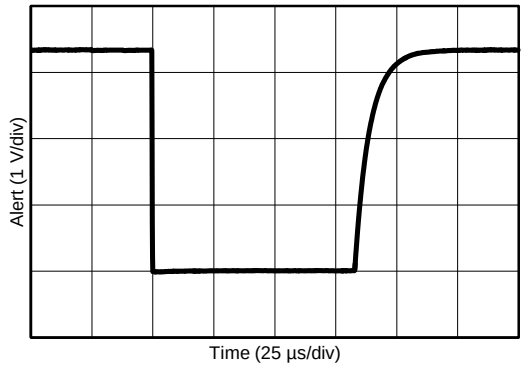


Figure 19. Alert Step Response

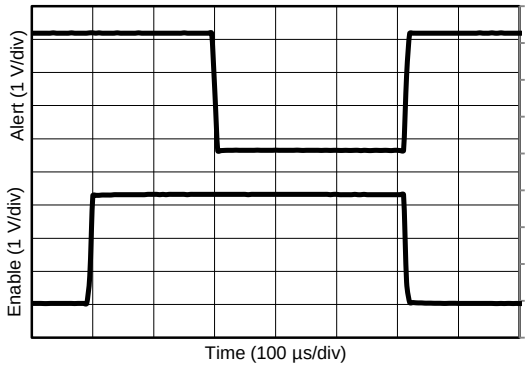


Figure 20. Alert Response (Disable to Enable)

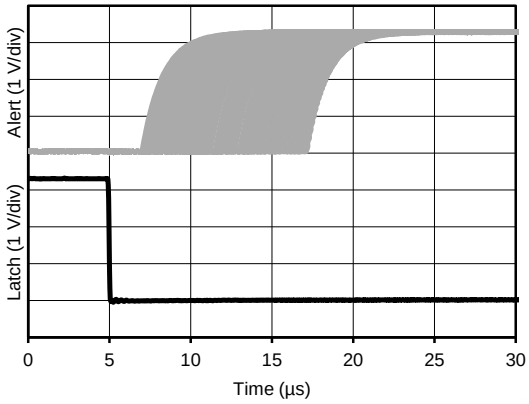


Figure 21. Alert Response (Latch Mode to Transparent Mode)

7 Detailed Description

7.1 Overview

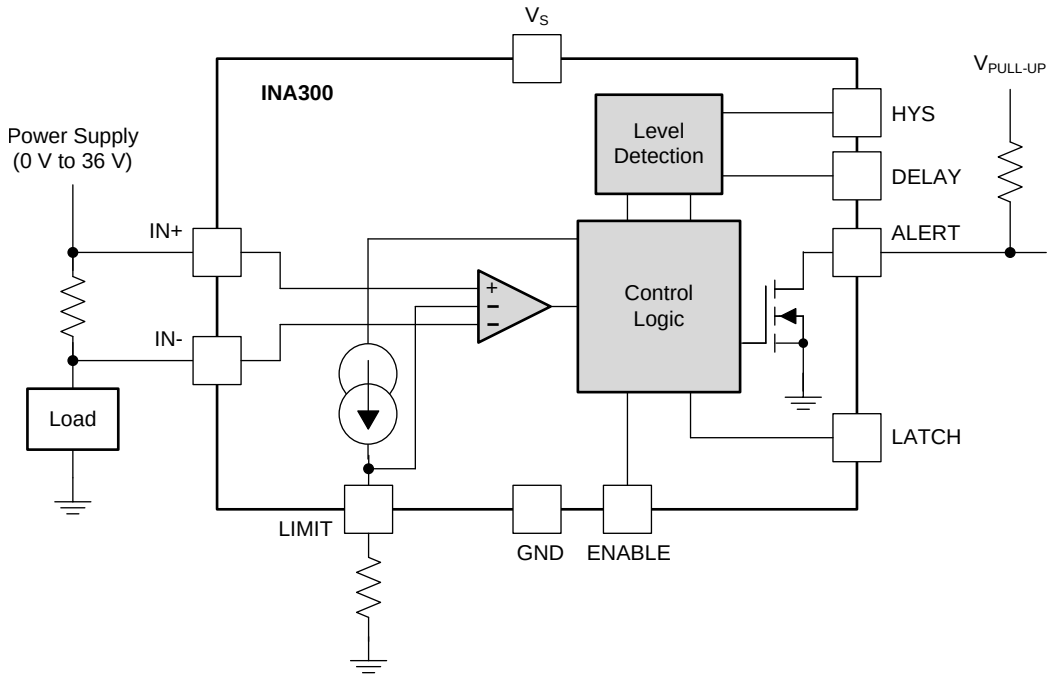
The INA300 is a 36-V, common-mode comparator designed specifically for overcurrent protection applications. To reduce system component count, this device combines both the current sense amplifier and threshold comparison into a single product for the overcurrent detection function. Programming this comparison threshold is configured through a single external resistor, thus simplifying the circuit design while allowing for easy adjustments to the threshold when needed. The value of the threshold setting resistor is selected based on an internal 20-µA current source to achieve a corresponding signal to the voltage developed across the current-sensing or current-shunt resistor in series with the load current being monitored.

The device is designed to accommodate a wide range of application requirements, including common-mode voltage, noise thresholds, and signal ranges. A wide signal threshold range reaching up to 250 mV is available to accommodate both power-sensitive applications requiring small dissipations across a current sense resistor and larger current-sensing resistors used in lower current applications.

Additional features available with the INA300 include a disable mode for reducing the current consumption of the device to below 10 µA, an output mode selector to enable either a latched or transparent alert output, and a selectable hysteresis value and alert response delay.

The wide signal range of the device is further enhanced with an adjustable hysteresis value to adjust the characteristics of the comparator, thus allowing for better accommodation of the full input range. The selectable alert response delays present in the INA300 assist in optimizing device operation to account for the system noise levels and operating characteristics required from this device. Longer delay settings allow for added rejection of system noise commonly present, thus reducing the potential for false alerts resulting from noise spikes that can easily occur in high-speed comparators.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Selecting a Current-Sensing Resistor

The device measures the differential voltage developed across a resistor when current flows through it to determine if the current being monitored exceeds a defined limit. This resistor is commonly referred to as a *current-sensing resistor* or a *current-shunt resistor*, with each term commonly used interchangeably. The flexible design of the device allows for measuring a wide differential input signal range across this current-sensing resistor, extending up to 250 mV.

Selecting the value of this current-sensing resistor is based primarily on two factors: the required accuracy of the current measurement and the allowable power dissipation across the current-sensing resistor. Larger voltages developed across this resistor allow more accurate measurements to be made. This large signal accuracy improvement results from the fixed internal amplifier errors that are dominated by the inherent input offset voltage of the device. When the input signal decreases, these fixed internal amplifier errors become a larger portion of the measurement and increase the uncertainty in the measurement accuracy. When the input signal increases, the measurement uncertainty is reduced because the fixed errors are a smaller percentage of the signal being measured.

A system design trade-off for improving the measurement accuracy through the use of larger input signals is the increase in power across the current-sensing resistor. Increasing the value of the current-shunt resistor increases the differential voltage developed across the resistor when current passes through the component. This increase in voltage across the resistor increases the power that the resistor must be able to dissipate. Decreasing the value of the current-shunt resistor value reduces the power dissipation requirements of the resistor, but increases the measurement errors resulting from the decreased input signal. Selecting the optimal value for the shunt resistor requires factoring both the accuracy requirement for the specific application and the allowable power dissipation of this component.

An increasing number of very low ohmic-value resistors are becoming available with values reaching down to 200 μΩ with power dissipations of up to 5 W that enable very large currents to be accurately monitored with sensing resistors.

7.3.1.1 Selecting a Current-Sensing Resistor: Example

In this example, the trade-offs involved in selecting a current-sensing resistor are discussed. This example requires a 5% measurement accuracy for detecting a 10-A overcurrent event at a 50-μs delay setting where only 250 mW is allowable for the dissipation across the current-sensing resistor at the full-scale current level. Although the maximum power dissipation is defined as 250 mW, a lower dissipation is preferred to improve system efficiency. Some initial assumptions are made that are used in this example: the limit setting resistor, R_{LIMIT}, is a 1% component and the maximum tolerance specification for the internal threshold setting current source, 0.5%, is used. Given the total error budget of 5%, up to 3.5% of error is available to be attributed to the internal offset of the device.

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Feature Description (continued)

As shown in Table 1, the maximum value calculated for the current-sensing resistor with these requirements is 2.5 mΩ. Although this value satisfies the maximum power dissipation requirement of 250 mW, headroom is available from the 5% maximum total error to reduce the value of the current-sensing resistor and reduce the power dissipation further. Selecting a 1.5-mΩ, current-sensing resistor value offers a good tradeoff for reducing the power dissipation in this scenario by approximately 40% while still remaining within the defined accuracy region.

Table 1. Calculating the Current-Sensing Resistor, R_{SENSE}

PARAMETER		EQUATION	VALUE	UNIT
	Maximum measurement error		5%	
I_{MAX}	Maximum current		10	A
P_{RSENSE}	Maximum allowable R_{SENSE} power dissipation	$R_{SENSE} \times I_{MAX}^2$	250	mW
	Initial error	R_{LIMIT} + I_{LIMIT} tolerances	1.5%	
R_{SENSE_MAX}	Maximum sensing resistor value	P_{RSENSE} / I_{MAX}^2	2.5	mΩ
V_{SENSE_MAX}	Input sense voltage	$R_{SENSE_MAX} \times I_{MAX}$	25	mV
V_{OS} Error	Offset voltage error	$(V_{OS} / V_{SENSE_MAX}) \times 100$	2%	
Error_Available	Maximum allowable offset error	Maximum Error – Initial Error	3.5%	
V_{SENSE_MIN}	Minimum input sense voltage	V_{OS} / (Error_Available / 100)	14.3	mV
R_{SENSE_MIN}	Minimum sensing resistor value	V_{SENSE_MIN} / I_{MAX}	1.43	mΩ
P_{RSENSE_MIN}	Minimum power dissipation	$R_{SENSE_MIN} \times I_{MAX}^2$	143	mW

7.3.2 Setting The Current-Limit Threshold

The device determines if an overcurrent event is present by comparing the measured differential voltage developed across the current-sensing resistor to the corresponding signal programmed at the LIMIT terminal. The threshold voltage for the LIMIT terminal can be set using a resistor or an external voltage source.

7.3.2.1 Resistor-Controlled Current Limit

The typical approach for setting the limit threshold voltage is to connect a resistor from the LIMIT terminal to ground. The value of this resistor, R_{LIMIT}, is chosen in order to create a corresponding voltage at the LIMIT terminal equivalent to the voltage, V_{TRIP}, developed by the load current flowing through the current-sensing resistor. An internal 20-µA current source is present at the LIMIT terminal that creates the corresponding voltage depending on the value of R_{LIMIT}. In the equations from Table 2, V_{TRIP} represents the overcurrent threshold the device is programmed to monitor for and V_{LIMIT} is the programmed signal set to detect the V_{TRIP} level. The term *noise adjustment factor* (NAF) is included in the V_{LIMIT} equation for the 10-µs delay setting. This value is equal to 500 µV and is used to adjust the operating point for the internal noise in this delay setting. The 50-µs and 100-µs delay settings do not use the NAF term in calculating the V_{LIMIT} threshold. See the *Noise Adjustment Factor (NAF)* section for more details on the noise adjustment factor.

In Table 2, the process for calculating the required value for R_{LIMIT} in order to set the appropriate threshold voltage, V_{LIMIT}, is shown. This calculation is based on the 10-µs delay setting so the NAF term is included in the calculation. For a delay setting of 50 µs or 100 µs, the NAF term is omitted.

Table 2. Calculating the Limit Threshold Setting Resistor, R_{LIMIT}

PARAMETER		EQUATION
V_{TRIP}	Desired current trip value	$I_{LOAD} \times R_{SENSE}$
V_{LIMIT}	Programmed threshold limit voltage	$V_{LIMIT} = V_{TRIP}$
V_{LIMIT} (1)	Threshold voltage	$(I_{LIMIT} \times R_{LIMIT}) – NAF$
R_{LIMIT} (1)	Threshold limit setting resistor	$(V_{LIMIT} + NAF) / I_{LIMIT}$
R_{LIMIT} (1)	Limit setting resistor	$(V_{LIMIT}$ + 500 µV) / 20 µA

(1) NAF is used with the 10-µs delay setting. NAF can be omitted in the R_{LIMIT} calculation for the 50-µs and 100-µs delay settings.

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TI recommends using NAF in calculating the value for V_{LIMIT} and R_{LIMIT} at the 10-µs delay setting. Removing NAF from the V_{LIMIT} and R_{LIMIT} calculation at the 10-µs delay setting lowers the trigger point of the alert output. Lowering the trigger point results in the device issuing an overcurrent alert prior to reaching the corresponding V_{TRIP} threshold. The averaging effect included with the 50-µs and 100-µs delay settings inherently eliminates the effect internal noise has on the threshold voltage.

7.3.2.2 Voltage Source Controlled Current Limit

The second method for setting the limit voltage is to connect the LIMIT terminal to a programmable DAC (digital-to-analog converter) or other external voltage source. The benefit of this method is the ability to adjust the current limit to account for different threshold voltages that are used for different system operating conditions. For example, this method can be used in a system that has one current-limit threshold level that must be monitored during the power-up sequence but different thresholds must be monitored during other system operating modes.

In Table 3, V_{TRIP} represents the overcurrent threshold the device is programmed to monitor for and V_{SOURCE} is the programmed signal set to detect the V_{TRIP} level. NAF is included in the V_{SOURCE} equation for the 10-µs delay setting. This value is equal to 500 µV and is used to adjust the operating point for the noise in the delay setting. The 50-µs and 100-µs delay settings do not use the NAF term in calculating the V_{SOURCE} threshold. For these delay settings, the NAF term is omitted. See the *Noise Adjustment Factor (NAF)* section for more details on the noise adjustment factor.

Table 3. Calculating the Limit Threshold Voltage Source, V_{SOURCE}

PARAMETER		EQUATION
V_{TRIP}	Desired current trip value	$I_{LOAD} \times R_{SENSE}$
V_{SOURCE} (1)	Programmed threshold limit voltage	V_{TRIP} + NAF
V_{SOURCE} (1)	Programmed signal set to detect the V_{TRIP} level	V_{TRIP} + 500 µV

(1) NAF is used with the 10-µs delay setting. NAF can be omitted in the V_{SOURCE} calculation for the 50-µs and 100-µs delay settings.

TI recommends using NAF in calculating the value for V_{SOURCE} at the 10-µs delay setting. Removing NAF from the V_{SOURCE} calculation at the 10-µs delay setting lowers the trigger point of the alert output. Lowering the trigger point results in the device issuing an overcurrent alert prior to reaching the corresponding V_{TRIP} threshold. The averaging effect included with the 50-µs and 100-µs delay settings inherently eliminates the effect internal noise has on the threshold voltage.

7.3.3 Delay Setting

The device response time for overcurrent events is adjustable based on the DELAY terminal setting. Three response time settings are available, ranging from 10 µs to 100 µs. The primary purpose for the three different delay settings is to offer a trade-off between a faster alert response and a more precise overcurrent threshold level detection.

The device has a 10-µs internal comparison window. This single comparison window is the fundamental time unit used for all three delay settings. For the 10-µs delay setting, the device compares the average of the input signal during the 10-µs comparison window to the threshold limit programmed at the LIMIT terminal. If the averaged input signal exceeds the threshold at the end of the 10-µs comparison window, the output alert triggers and pulls the $\overline{\text{ALERT}}$ terminal low. However, if the averaged input does not exceed the threshold at the end of the 10-µs comparison window, there is no change in the output alert status, which remains high to indicate that no overcurrent event is detected.

For the 50-µs delay setting, there must be five consecutive 10-µs comparison windows that result in an average input signal exceeding the threshold limit in order for the output alert to trigger and pull the $\overline{\text{ALERT}}$ terminal low. If any single 10-µs comparison window fails to detect an overcurrent condition before reaching five consecutive overcurrent comparisons, the internal counter is reset and no output alert is issued. With the internal counter reset, a new group of five consecutive 10-µs comparison windows of overcurrent conditions are required in order to trigger the alert and pull the $\overline{\text{ALERT}}$ terminal low.

The 100-µs delay setting operates in the same manner as the 50-µs method, but instead requires ten consecutive 10-µs comparison windows with an input signal exceeding the threshold limit in order to issue an output alert and pull the $\overline{\text{ALERT}}$ terminal low.

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Requiring multiple consecutive overcurrent detections aides significantly in reducing the likelihood of system noise causing false alerts, which can be extremely detrimental to critical system operations. However, by enabling an alert window equal to the comparison window of 10 µs, the device still has the flexibility to be used in fast overcurrent detection applications that require quick responses to rapidly changing system operating characteristics.

In Figure 22, the device alert output response is shown for both a 10-µs delay setting and a 50-µs delay setting based on the same input signal condition. The initial increase of the input signal, V_{IN}, above the V_{LIMIT} level remains above the limit for approximately 30 µs. With the device set to the 10-µs delay setting, the overcurrent condition is detected and the alert output terminal is pulled low approximately 10 µs later. With the device set to the 50-µs delay setting, an alert is not issued because five consecutive 10-µs overcurrent measurements are not detected. With the input signal only being over the limit for 30 µs rather than the corresponding 50 µs needed for this delay setting, the device does not issue an alert under this condition. For the second instance where V_{IN} rises above the V_{LIMIT} threshold, the input remains above the limit for more than five consecutive 10-µs measurements, indicating an overcurrent condition and the alert output terminal is pulled low.

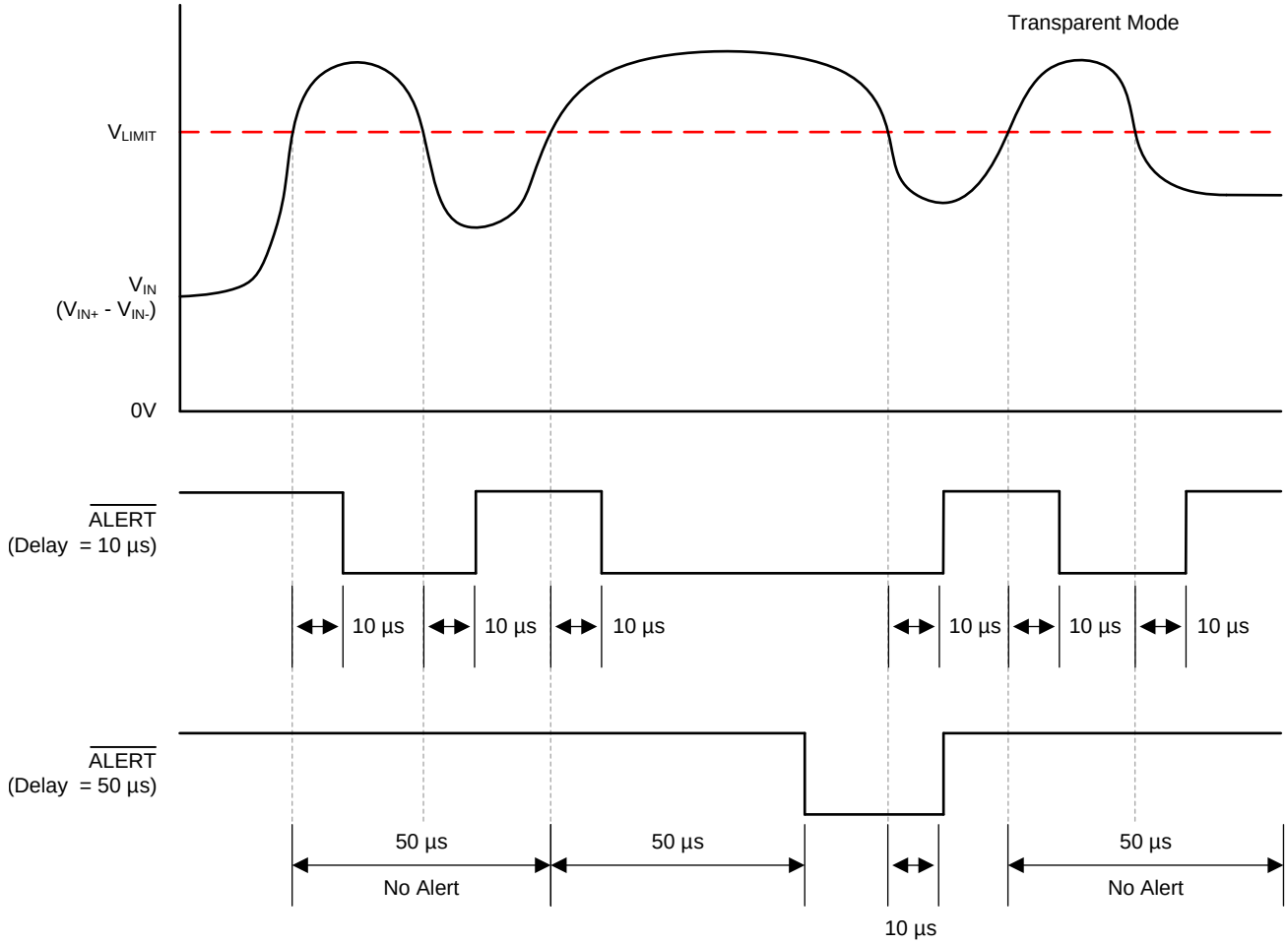

Figure 22. DELAY Terminal Settings

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As discussed previously, there are three different available delay settings that are configured based on the signal connected to the DELAY terminal, as shown in Figure 23 and Table 4. The DELAY terminal must be either connected directly to ground, directly to supply, or left completely floating. Additional external resistors should not be connected to this terminal. If a resistance is required by the application to be placed in series with either the supply or ground connection to the DELAY terminal, this resistance must be limited to 1 kΩ so as to not conflict with the internal level-detection circuitry.

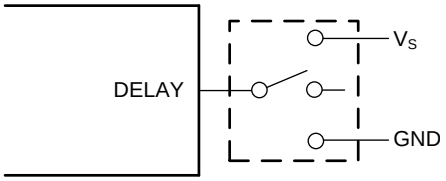

Figure 23. Delay Response

Table 4. Delay Settings

DELAY	ALERT DELAY (µs)
Open or floating	10
GND	50
V_S	100

7.3.4 Alert Timing Response

The device has a 10-µs internal comparison window where the input signal is measured to compare to the limit threshold voltage. This window continuously runs internal to the device without any external indicator or control. A comparison is made at the completion of each 10-µs comparison window to determine if the averaged input over the comparison window exceeds the limit threshold, thus indicating if an overcurrent event has occurred.

This comparison window is not synchronized with the input signal so there is an unknown timing component present. With this free-running internal timing window, an overcurrent event can occur anywhere within the 10-µs comparison window. This condition causes a variation in the amount of time before the alert appears at the output because the comparison is always made at the end of the 10-µs comparison window. Figure 24 shows the variation in time between when the input signal rises above the threshold voltage and when a change at the alert output terminal occurs.

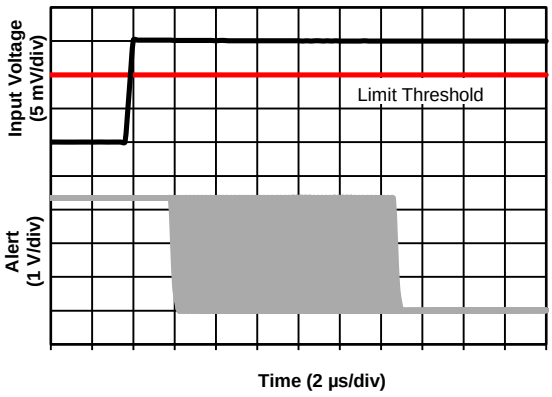

Figure 24. 10-µs Alert Response Window

The delay shown in Figure 24 represents the response time of the device with a 10-µs delay setting. With a 50-µs delay setting, an additional 40 µs is added to the timing response, as shown in Figure 25. A 100-µs delay setting adds 90 µs to the response time, as shown in Figure 26.

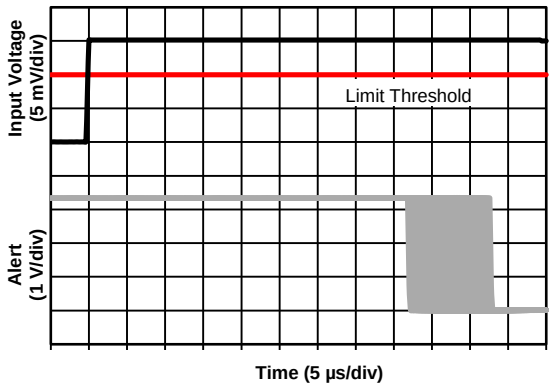

Figure 25. 50-µs Alert Response Window

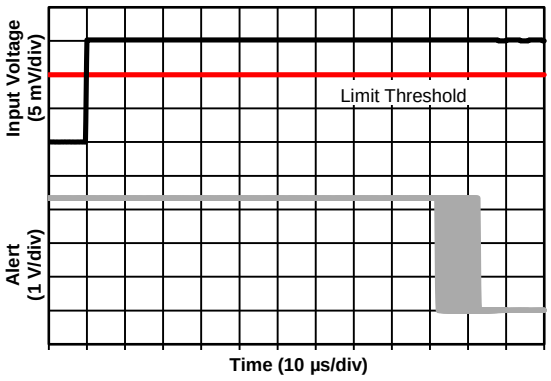

Figure 26. 100-µs Alert Response Window

7.3.5 Selectable Hysteresis

Device hysteresis is adjustable based on the setting at the hysteresis (HYS) terminal. The smallest setting for hysteresis on the device, 2 mV, is enabled by leaving the HYS terminal open and floating. A 4-mV hysteresis is set by connecting the HYS terminal to ground; connecting this terminal to the supply voltage sets the hysteresis to 8 mV, as shown in Figure 27. The HYS terminal must be either connected directly to ground, directly to supply, or left completely floating. Additional external resistors should not be connected to this terminal. If a resistance is required by the application to be placed in series with either the supply or ground connections to the HYS terminal, this resistance must be limited to 1 kΩ so as to not conflict with the internal level-detection circuitry.

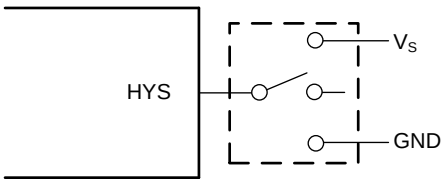

Figure 27. Delay Response

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The very wide dynamic input range of the INA300 necessitates an adjustable hysteresis to ensure that the device can be more appropriately configured based on the specific operating conditions and requirements of the application. Figure 28 illustrates the transition locations for the $\overline{\text{ALERT}}$ terminal based on where the input signal, V_{IN}, is measured relative the limit threshold, V_{LIMIT}. The corresponding hysteresis levels and physical terminal settings for the device are shown in Table 5.

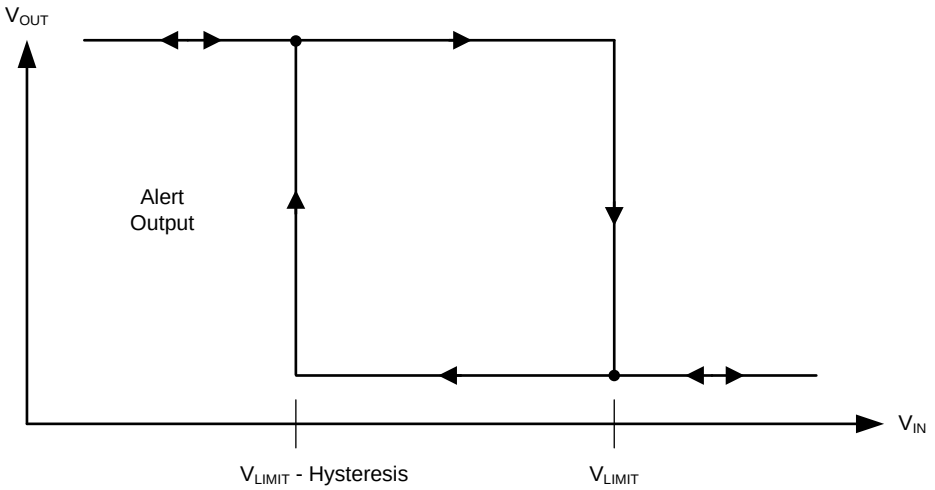

Figure 28. Typical Comparator Hysteresis

Table 5. Hysteresis Settings

HYSTERESIS	HYSTERESIS SETTING
Float	2 mV
GND	4 mV
V_S	8 mV

7.3.6 Alert Output

The device $\overline{\text{ALERT}}$ terminal is an active-low, open-drain output. This output is designed to be pulled low when the input conditions are detected to be out-of-range. This open-drain output pin is recommended to include a 10-kΩ, pull-up resistor to the supply voltage. This open-drain terminal can be pulled up to a voltage beyond the supply voltage, V_S, but should not exceed 5.5 V.

7.3.7 Noise Adjustment Factor (NAF)

The device is a high-speed, low-noise comparator that is designed to alert when the measured input signal exceeds the programmed limit level. Internal noise in the device couples into the measurement and can result in alerts being issued prior to the input signal exceeding the voltage level present at the LIMIT terminal. This known internal noise component effects the input signal measurement by causing a consistent shift in the device internal offset, resulting in a shifted trip threshold for the device. NAF serves to adjust the V_{LIMIT} setting to account for this internal shift, thus allowing for a more precise level detection of the measured current.

The NAF value is based on the noise contribution on the measurement at the 10-µs delay setting. This value is equal to 500 µV and is applied in the calculation to adjust the V_{LIMIT} threshold level to allow for a more accurate alert trip point. The NAF term is only applied in the V_{LIMIT} calculation at the 10-µs delay setting. The averaging effect included with the 50-µs and 100-µs delay settings inherently eliminates the effect internal noise has on the threshold voltage. The NAF term can be omitted from the R_{LIMIT} calculation at the 10-µs delay setting with the effect of a lower trigger point of the alert output. Lowering the trigger point results in the device issuing an overcurrent alert prior to reaching the corresponding V_{TRIP} threshold.

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7.4 Device Functional Modes

7.4.1 Alert Mode

The device has two output operating modes that are selected based on the LATCH terminal setting. The two operating modes are transparent mode and latch mode. These modes change how the ALERT terminal responds to the changing input signal conditions.

7.4.1.1 Transparent Output Mode

The device is set to transparent mode when the LATCH terminal is pulled low, thus allowing the output alert state to change and follow the input signal with respect to the programmed alert threshold. For example, when the differential input signal rises above the alert threshold, the alert output terminal is pulled low. As soon as the differential input signal drops below the alert threshold for 10 µs, the output returns to the default high output state. A common implementation using the device in transparent mode is to connect the ALERT terminal to a hardware interrupt input on a controller. As soon as an overcurrent condition is detected in the device and the ALERT terminal is pulled low, the controller interrupt terminal detects the output state change and can begin making changes to the system operation needed to address the overcurrent condition.

7.4.1.2 Latch Output Mode

Some applications do not have the functionality available to continuously monitor the state of the output ALERT terminal to detect an overcurrent condition. A typical example of this application is a system that is only able to poll the ALERT terminal state periodically to determine if the system is functioning correctly. If the device is set to transparent mode in this type of application, missing the change in state of the ALERT terminal is possible when ALERT is pulled low to indicate an out-of-range event if the out-of-range condition does not appear during one of these periodic polling events.

Latch mode is specifically intended to accommodate these applications. As shown in Table 6, the device is placed in latch mode by setting the voltage on the LATCH terminal to a logic high level. The difference between latch mode and transparent mode is how the alert output responds when an overcurrent event ends. In transparent mode, when the differential input signal drops below the limit threshold level for 10 µs, the output state returns to the default high setting to indicate that the overcurrent event had ended.

In latch mode, when an overlimit condition is detected and the ALERT terminal is pulled low, the ALERT terminal does not return to the default high level when the differential input signal drops below the alert threshold level for 10 µs. In order to clear the alert the LATCH terminal must be pulled low for at least 20 µs. Pulling the LATCH terminal low allows the ALERT terminal to return to the default high level provided that the differential input signal has dropped below the alert threshold. If the input signal is still above the threshold limit when the LATCH terminal is pulled low, the ALERT terminal remains low. When the alert condition is detected by the system controller, the LATCH terminal can be set back to high in order to place the device back in latch mode.

Table 6. Output Mode Settings

OUTPUT MODE	LATCH TERMINAL SETTING
Transparent mode	LATCH = low
Latch mode	LATCH = high

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The latch and transparent modes are represented in Figure 29. In this figure, when V_{IN} drops back below the V_{LIMIT} threshold for the first time, the LATCH terminal is pulled high. With the LATCH terminal pulled high, the device is set to latch mode so that the alert output state does not return high when the input signal drops below the V_{LIMIT} threshold. Only when the LATCH terminal is pulled low does the $\overline{\text{ALERT}}$ terminal return to the default high level, thus indicating the input signal is below the limit threshold. When the input signal drops below the limit threshold for the second time, the LATCH terminal is already pulled low. The device is set to transparent mode at this point and the $\overline{\text{ALERT}}$ terminal is pulled back high as soon as the input signal drops below the alert threshold.

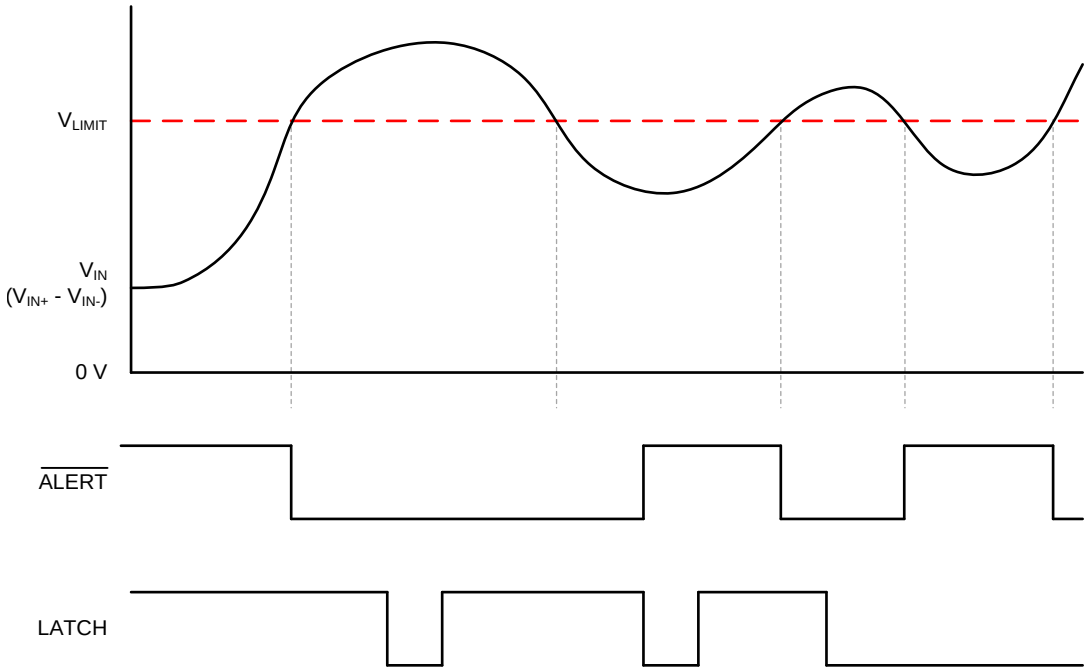

Figure 29. Transparent versus Latch Mode

7.4.2 Disable Mode

The INA300 has an ENABLE terminal that allows the device to be placed into an active enabled state or a low-power disabled state where a total of less than 10 µA is consumed from all terminals. This disable state allows the device to be used in applications where very low current consumption is required to extend battery life where constant monitoring is not required. The device requires approximately 20 µs to enter the low-power state when the ENABLE terminal transitions from high to low, as shown in Table 7. To return to the enabled active state, the device requires approximately 300 µs to return to normal operation when the ENABLE terminal transitions from low to high, thus taking the device out of the low-power state.

Table 7. Enable and Disable Mode Settings

ENABLE MODE	ENABLE TERMINAL SETTING
Disable mode	ENABLE = low
Enable mode	ENABLE = high

The internal counter that determines if the necessary consecutive 10-µs window comparison alert conditions are reached for the 50-µs and 100-µs delay setting is reset when the device is put into a disabled state. When the device is re-enabled the counter restarts.

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7.4.3 Input Filtering

External system noise can have a significant effect in the ability of a comparator to accurately measure and detect whether input signals exceed the reference threshold levels, thus indicating an overrange condition. The device is susceptible to external noise as well, although the 50-µs and 100-µs delay settings are designed to mitigate the impact of noise based on the effective averaging achieved in these modes. The most obvious effect that external noise can have on the operation of a comparator is to cause a false alert condition. If a comparator detects a large noise transient coupled into the signal, the device can easily interpret this transient as an overrange condition.

External filtering can help reduce the amount of noise that reaches the comparator inputs and reduce the likelihood of a false alert from occurring. The tradeoff to adding this noise filter is that the comparator response time is increased because of the input signal being filtered as well as the noise. Figure 30 shows the implementation of an input filter for the device.

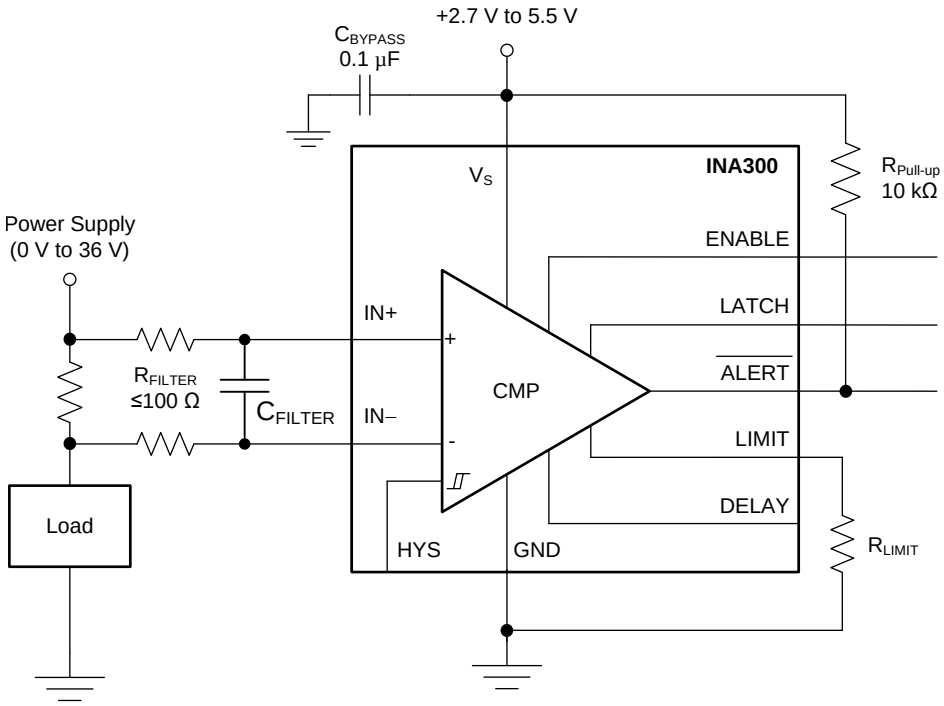

Figure 30. Input Filter

Limiting the amount of input resistance used in this filter is important because this resistance can have a significant effect on the input signal that reaches the device input pins resulting from the device input bias currents. A typical system implementation involves placing the current-sensing resistor very near the device so the traces are very short and the trace impedance is very small. This layout helps reduce the ability of coupling additional noise into the measurement. Under these conditions, the characteristics of the input bias currents have minimal effect on device performance.

As shown in Figure 31, the input bias currents increase in opposite directions when the differential input voltage increases. This increase results from the design of the device, which allows common-mode input voltages to far exceed the device supply voltage range. With input filter resistors now placed in series with these unequal input bias currents, there are unequal voltage drops developed across these input resistors. The difference between these two drops appears as an added signal that (in this case) subtracts from the voltage developed across the current-sensing resistor, thus reducing the signal that reaches the device input terminals. Smaller value input resistors reduce this effect of signal attenuation to allow for a more accurate measurement.

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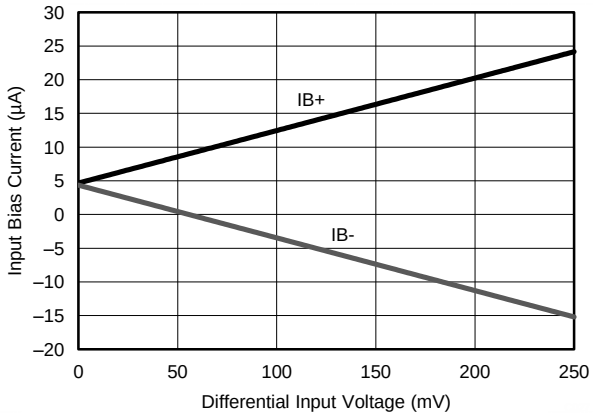

Figure 31. Input Bias Current vs Differential Input Voltage

For example, with a differential voltage of 10 mV developed across a current-sensing resistor and using 100-Ω resistors, the differential signal that actually reaches the device is 9.8 mV. A measurement error of 2% is created as a result of these external input filter resistors. Using 10-Ω input filter resistors instead of the 100-Ω resistors reduces this added error from 2% down to 0.2%.

7.4.4 Using the INA300 With Common-Mode Transients Above 36 V

With a small amount of additional circuitry, the device can be used in circuits subject to transients higher than 36 V. Use only zener diodes or zener-type transient absorbers (sometimes referred to as *Transzorbs*). Any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors, as shown in Figure 32, as a working impedance for the zener diode. Keeping these resistors as small as possible is best, preferably 100 Ω or less. Larger values can be used with an additional error induced resulting from a reduced signal that actually reaches the device input terminals. Because this circuit limits only short-term transients, many applications are satisfied with a 100-Ω resistor along with conventional zener diodes of the lowest power rating available. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

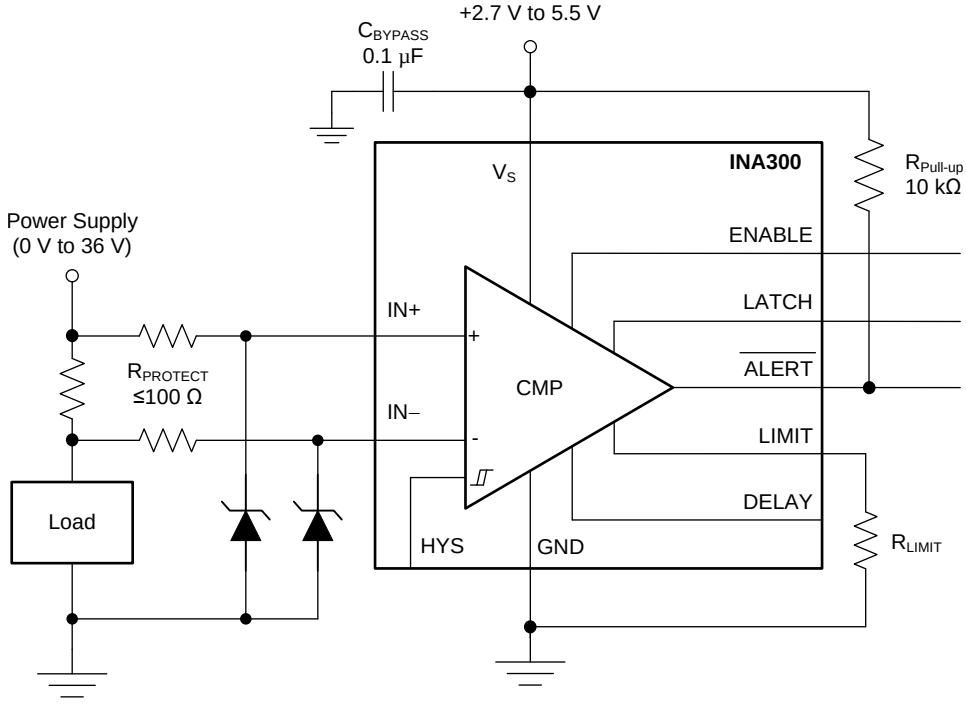

Figure 32. Transient Protection

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The INA300 is designed to enable easy configuration for detecting overcurrent conditions in an application. This device is individually targeted towards overcurrent detection of a single threshold. However, this device can also be paired with additional devices and circuitry to create more complex monitoring functional blocks.

8.2 Typical Applications

8.2.1 Unidirectional Operation

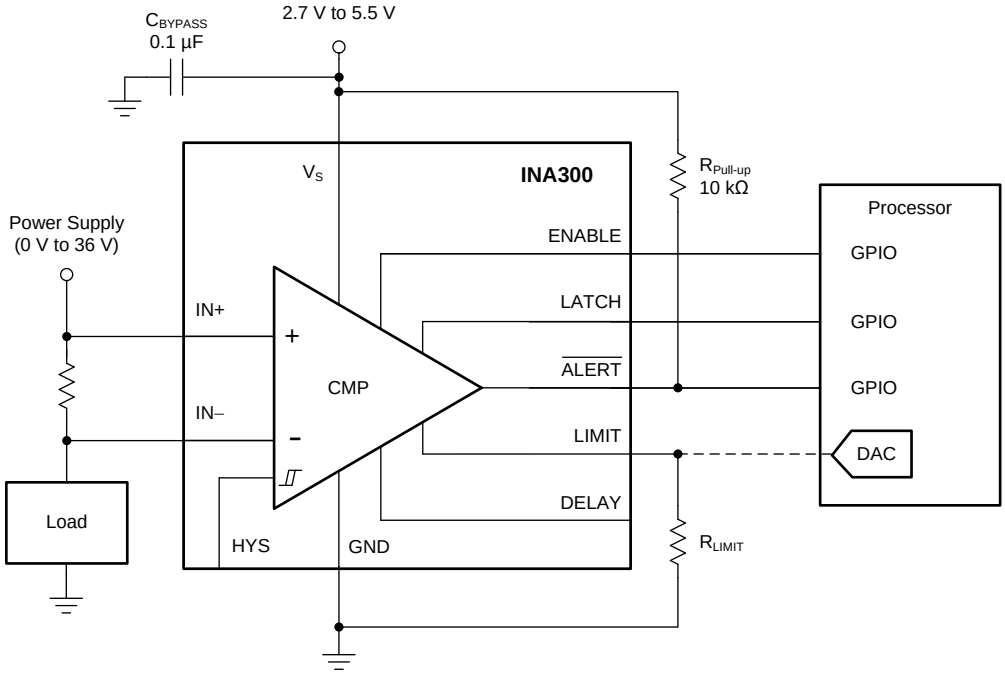

Figure 33. Unidirectional Application Schematic

8.2.1.1 Design Requirements

The device measures current through a resistive shunt with current flowing in one direction, thus enabling detection of an overcurrent event only when the differential input voltage exceeds the threshold limit.

8.2.1.2 Detailed Design Procedure

Figure 33 shows the basic connections of the device. The input terminals, IN+ and IN–, should be connected as closely as possible to the current-sensing resistor to minimize any resistance in series with the shunt resistance. Additional resistance between the current-sensing resistor and input terminals can result in errors in the measurement. When input current flows through this external input resistance, the voltage developed across the shunt resistor can differ from the voltage reaching the input terminals.

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Typical Applications (continued)

8.2.1.3 Application Curve

Figure 34 shows the alert response transitioning from a high to a low state following the input signal exceeding the limit threshold voltage. The time required for the output to respond varies as a result of when the input signal crosses the threshold limit voltage relative to where in the continuous running internal 10-µs comparison window the overrange condition occurs. In Figure 34, the output response varies from roughly 2 µs to approximately 12 µs when the input exceeds the threshold level. This variance is a result of where in the 10-µs comparison window the overrange event occurs. If the overrange event occurs late in the 10-µs comparison window and is large enough to average the entire window measurement up above the threshold level, the alert appears to respond very quickly. If the alert occurs late in the 10-µs comparison window and is not large enough to average the entire window measurement up above the threshold level, the alert does not appear until the next 10-µs comparison window completes, assuming the input signal remains above the threshold for the entire duration.

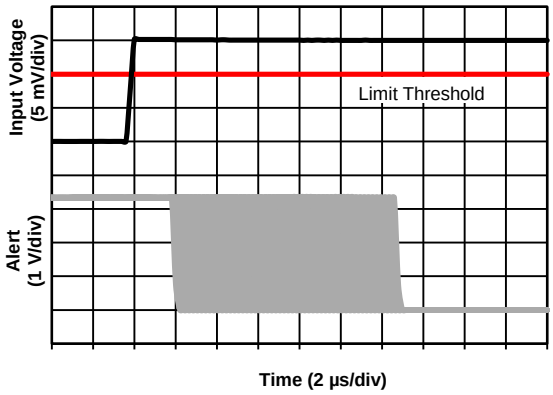

Figure 34. Alert Response

Typical Applications (continued)

8.2.2 Bidirectional Operation

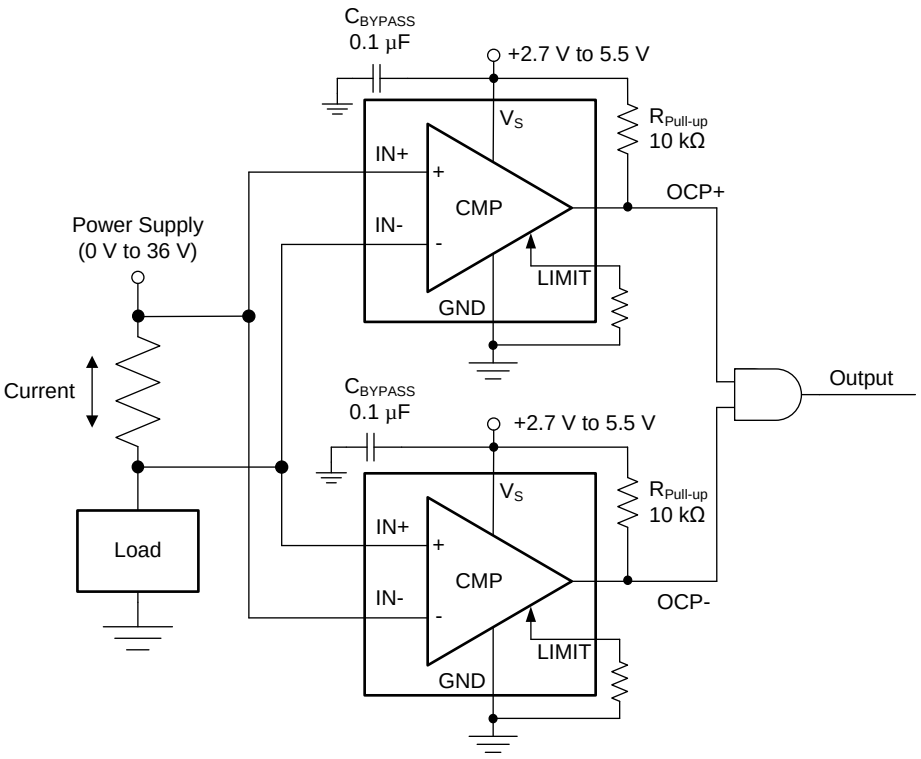

Figure 35. Bidirectional Application

8.2.2.1 Design Requirements

Although the device is only able to measure current through a current-sensing resistor flowing in one direction, a second INA300 can be used to create a bidirectional monitor.

8.2.2.2 Detailed Design Procedure

With the input terminals of a second device reversed across the same current-sensing resistor, the second device is now able to detect current flowing in the other direction relative to the first device, as shown in Figure 35. The outputs of each device connect to an AND gate to detect if either of the limit threshold levels are exceeded. The output of the AND gate is high if neither overcurrent limit thresholds are exceeded. A low output state of the AND gate indicates that either the positive overcurrent limit or the negative overcurrent limit are surpassed.

Table 8. Bidirectional Overcurrent Output Status

OCP STATUS	OUTPUT
OCP+	0
OCP–	0
No OCP	1

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8.2.2.3 Application Curve

Figure 36 illustrates two INA300 devices being used in a bidirectional configuration and an output control circuit to detect if one of the two alerts is exceeded.

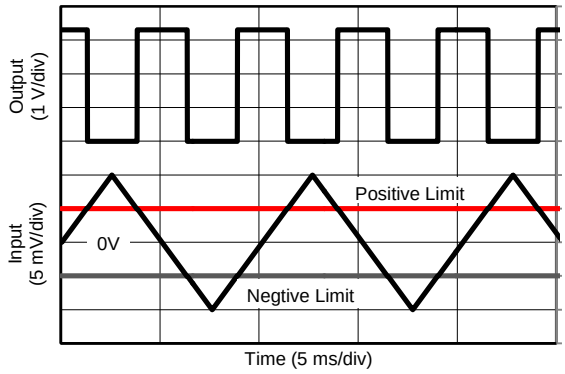

Figure 36. Bidirectional Application Curve

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8.2.3 Window Comparator

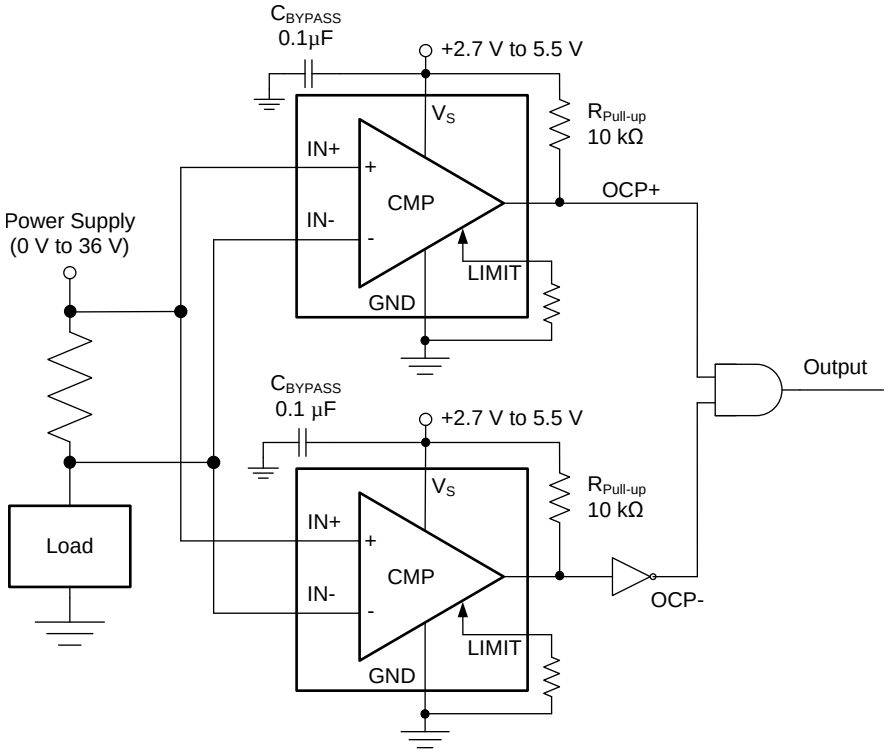

Figure 37. Window Comparator Application

8.2.3.1 Design Requirements

The device can also be used to create a window comparator function, detecting whether the current being monitored is within a programmed range or has fallen outside of the expected operating region.

8.2.3.2 Detailed Design Procedure

Figure 37 shows how the window comparator function is setup using two devices. The input terminals of each device are connected to the same current-sensing resistor. The limit threshold for the top device is set to the upper limit of the window range. The bottom device limit threshold is set to the desired lower limit of the range. With a logic inverter placed at the output of the device monitoring the lower limit, the OCP– signal is high when the input signal is above the lower limit threshold. The OCP+ signal is high when the input signal is below the upper limit threshold. A high value at the output (output of the AND gate) indicates that the monitored current is operating within the desired window range.

Table 9. Window Comparator Output Status

INPUT CONDITION	OUTPUT STATUS
Above range	0
Below range	0
In range	1

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8.2.3.3 Application Curve

Figure 38 shows the output waveform from the device window comparator application. In Figure 38, the output signal is high when OCP– is low (the input signal is above the lower limit) and when OCP+ is high (the input signal is below the upper limit). If the signal rises above the upper limit or drops below the lower limit, the corresponding OCP output changes state, causing the state of the output (following the AND gate) to change to zero to indicate an out-of-range condition.

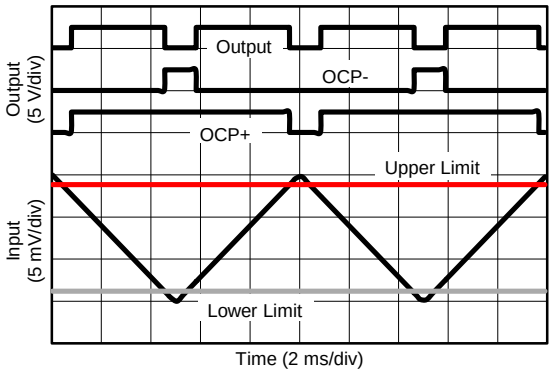

Figure 38. Output Waveform

9 Power Supply Recommendations

The device input circuitry can accurately measure signals on common-mode voltages beyond the power-supply voltage, V_S. For example, the voltage applied to the V_S power-supply terminal can be 5 V, whereas the load power-supply voltage being monitored (V_{CM}) can be as high as +36 V. Note also that the device can withstand the full –0.3 V to +36 V range at the input terminals, regardless of whether the device has power applied or not.

Power-supply bypass capacitors are required for stability and should be placed as closely as possible to the supply and ground terminals of the device. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

10 Layout

10.1 Layout Guidelines

- The power-supply bypass capacitor should be placed as closely as possible to the supply and ground terminals. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- The connection of R_{LIMIT} to the ground terminal should be made as direct as possible to limit additional capacitance on this node. Routing this connection should be limited to the same plane if possible avoiding vias to internal planes. If the routing can not be made on the same plane and must pass through vias, ensure that a path is routed from the R_{LIMIT} back to the ground terminal and that the R_{LIMIT} is not just connected directly to a ground plane.
- The DELAY terminal must be either connected directly to ground, directly to supply, or left completely floating. Additional external resistors should not be connected to this terminal. If a resistance is required by the application to be placed in series with either the supply or ground connection to the DELAY terminal, this resistance must be limited to 1 kΩ so as to not conflict with the internal level detection circuitry.
- The HYS terminal must be either connected directly to ground, directly to supply, or left completely floating. Additional external resistors should not be connected to this terminal. If a resistance is required by the application to be placed in series with either the supply or ground connections to the HYS terminal, this resistance must be limited to 1 kΩ so as to not conflict with the internal level detection circuitry.
- The open-drain output pin is recommended to be pulled up to the supply voltage rail through a 10-kΩ pull-up resistor.

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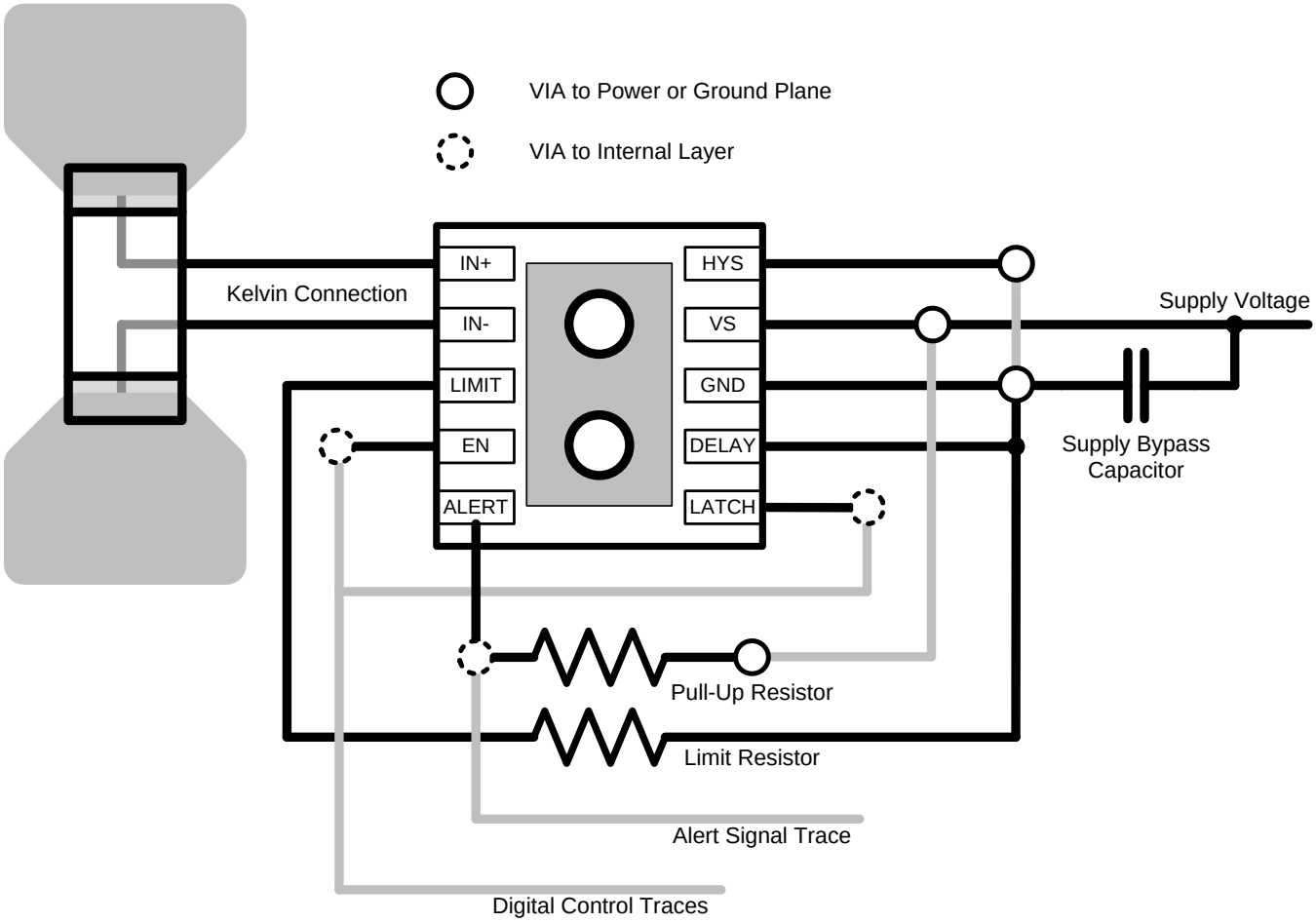
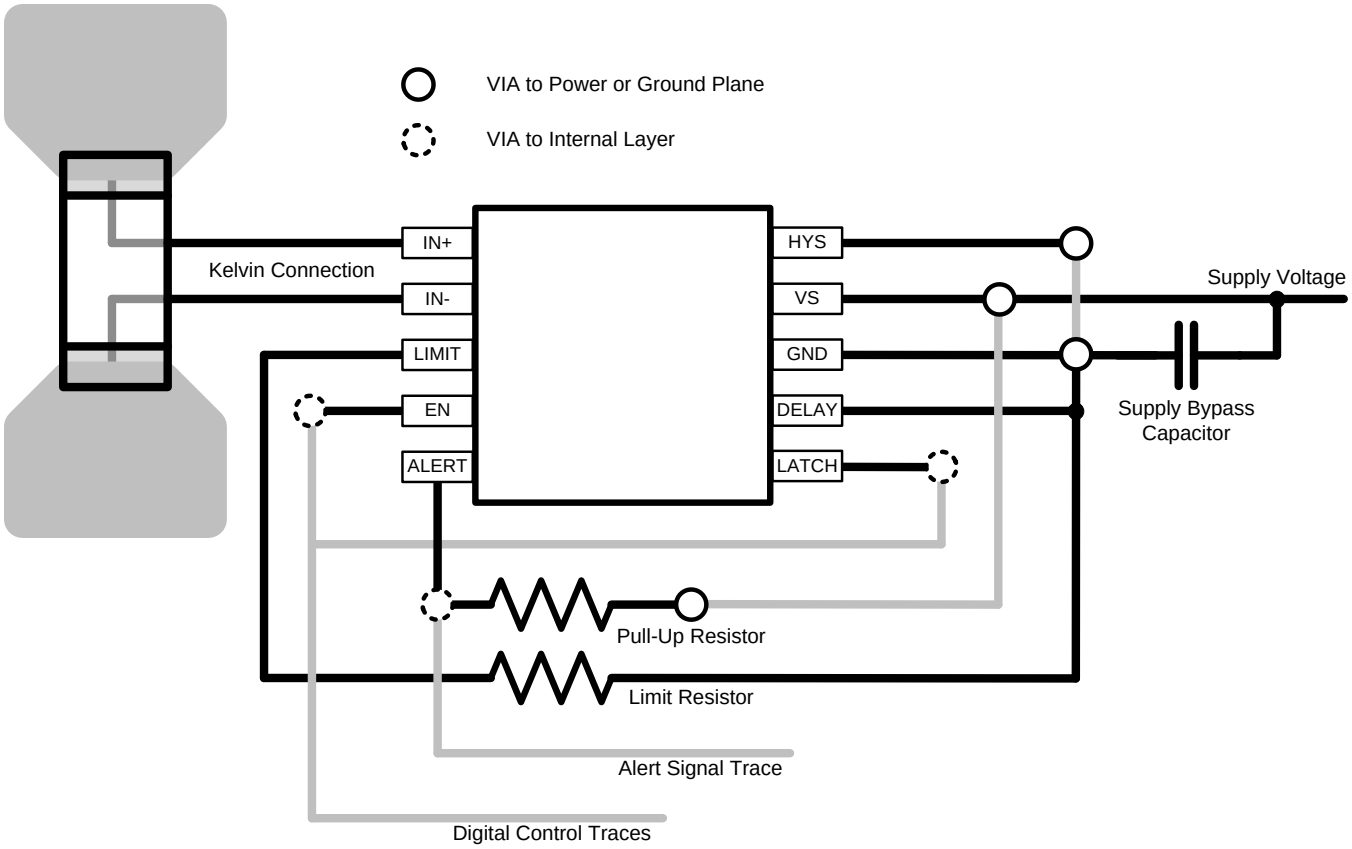
10.2 Layout Example



NOTE: Connect the limit resistor directly to the GND terminal.

Figure 39. Recommended Layout for WSON Package

Layout Example (continued)



NOTE: Connect the limit resistor directly to the GND terminal.

Figure 40. Recommended Layout for VSSOP Package

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- INA300EVM User's Guide, SBAU220

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

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11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA300AIDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	12T6	Samples
INA300AIDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	12T6	Samples
INA300AIDSQR	ACTIVE	WSON	DSQ	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKD	Samples
INA300AIDSQT	ACTIVE	WSON	DSQ	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF INA300 :

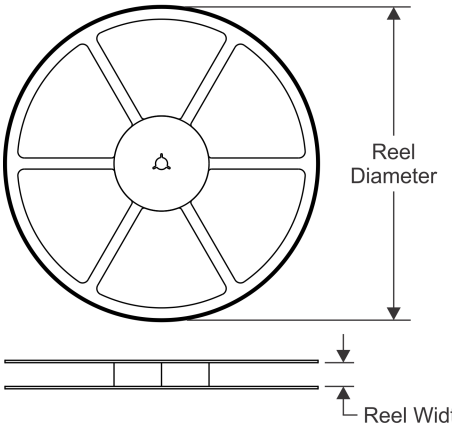
- Automotive: INA300-Q1

NOTE: Qualified Version Definitions:

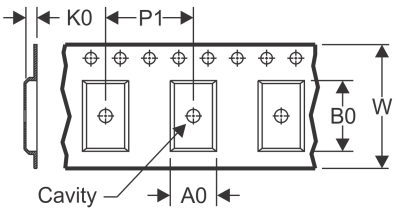
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

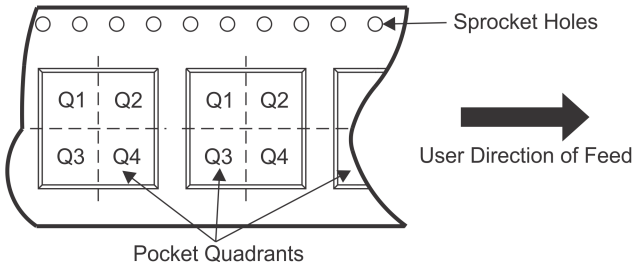


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

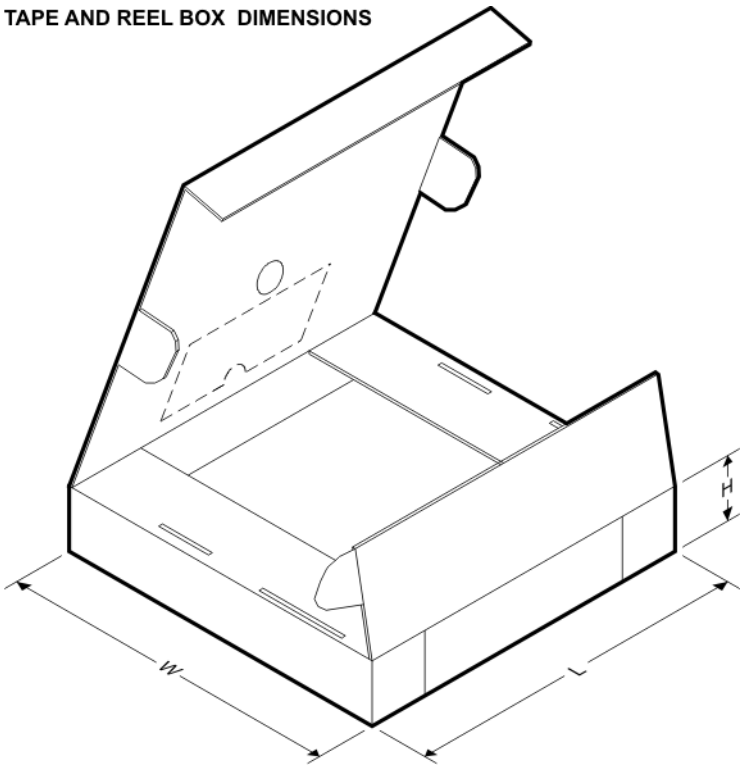
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA300AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA300AIDGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA300AIDSQR	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA300AIDSQT	WSON	DSQ	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

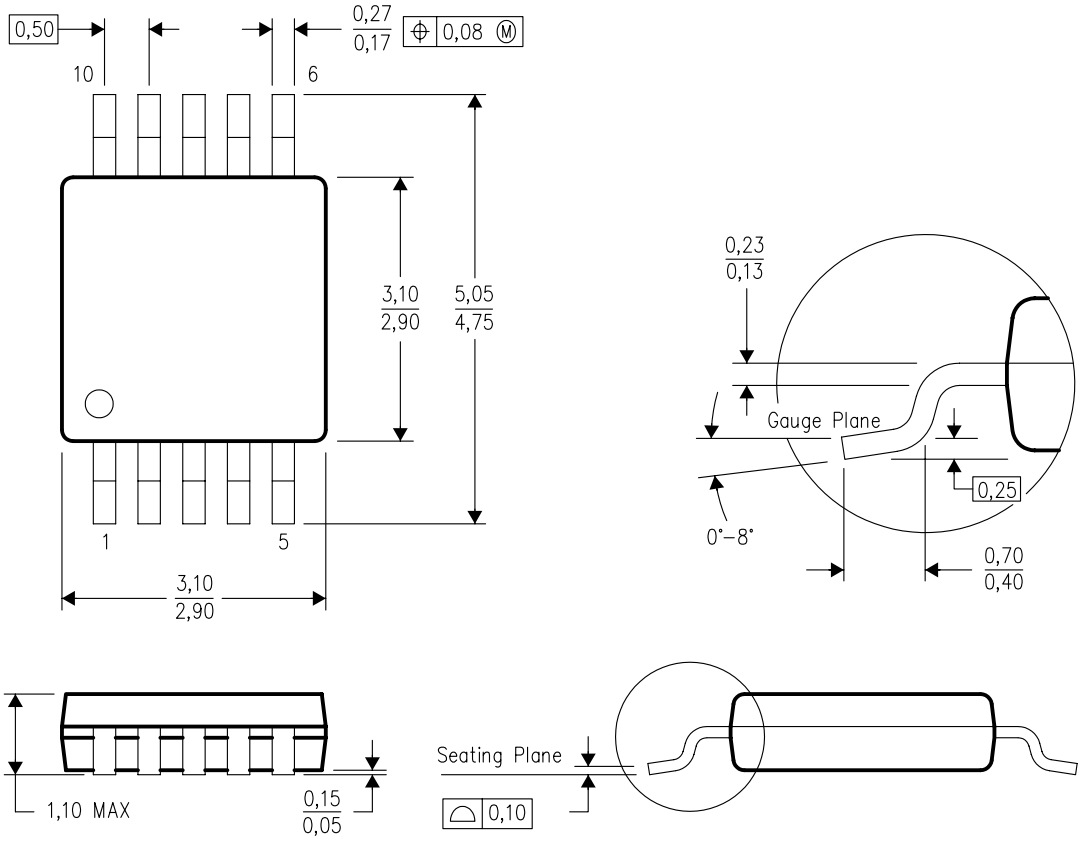
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA300AIDGSR	VSSOP	DGS	10	2500	364.0	364.0	27.0
INA300AIDGST	VSSOP	DGS	10	250	364.0	364.0	27.0
INA300AIDSQR	WSON	DSQ	10	3000	210.0	185.0	35.0
INA300AIDSQT	WSON	DSQ	10	250	210.0	185.0	35.0

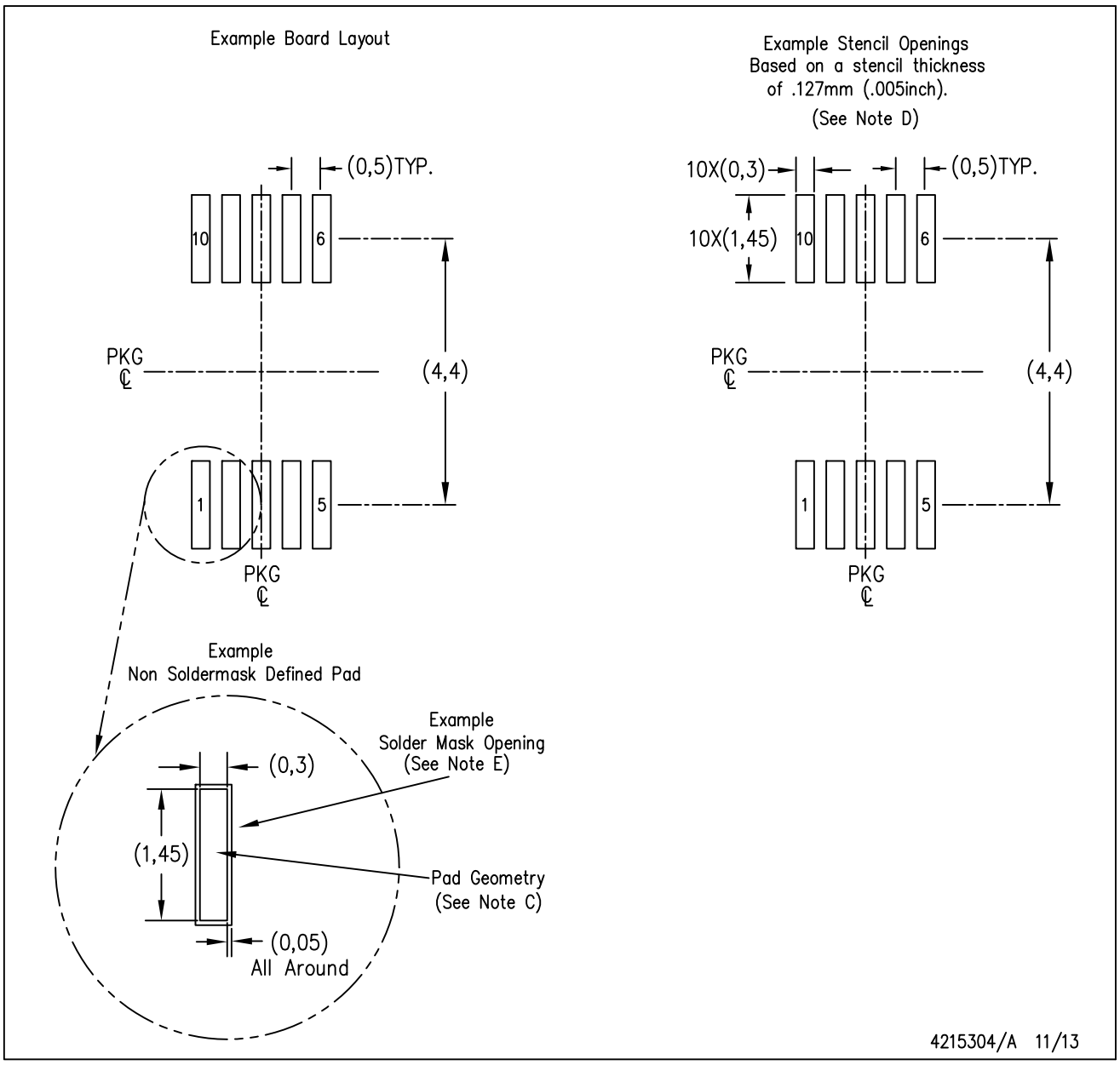
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

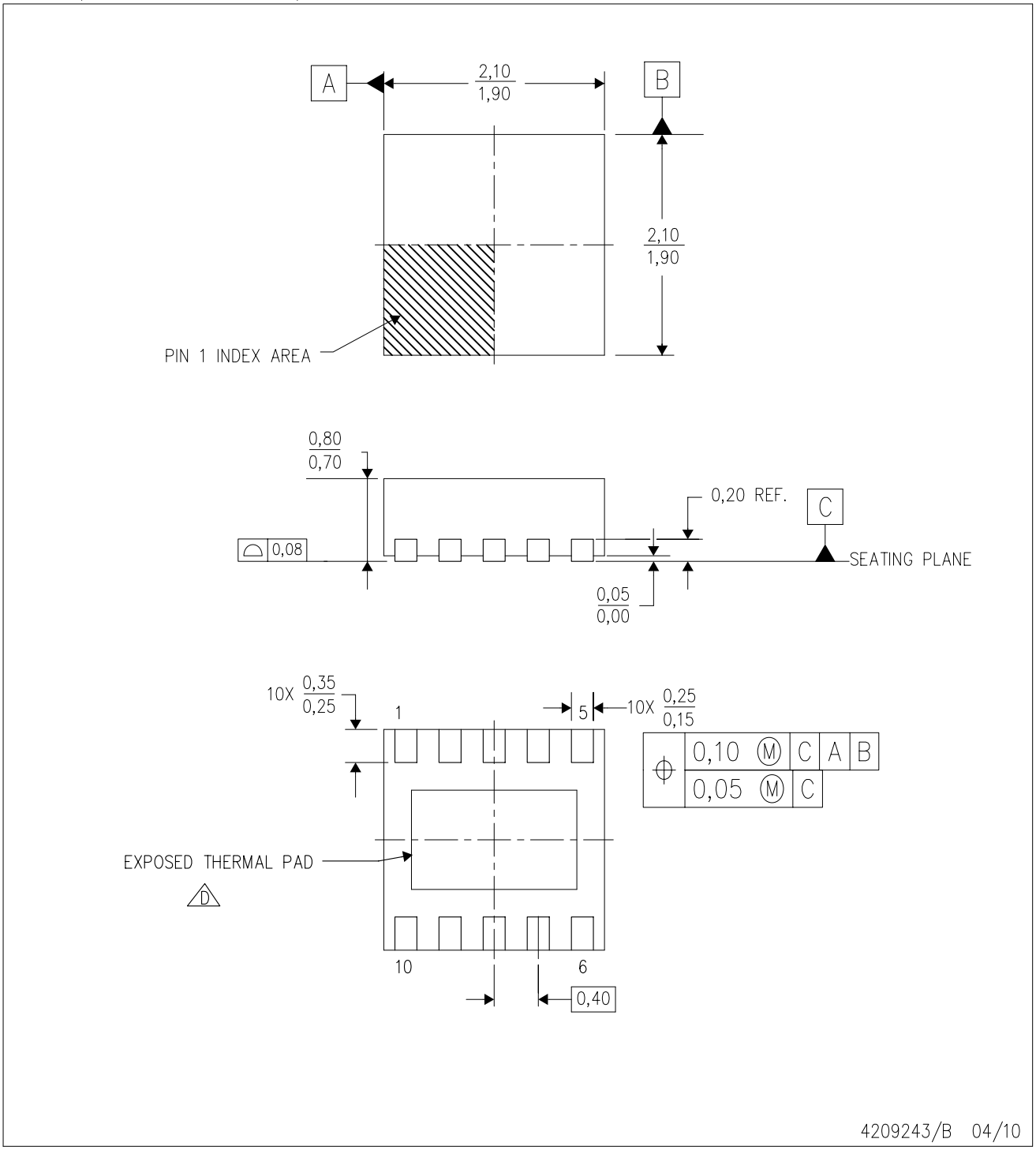
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

DGS (S–PDSO–G10) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DSQ (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

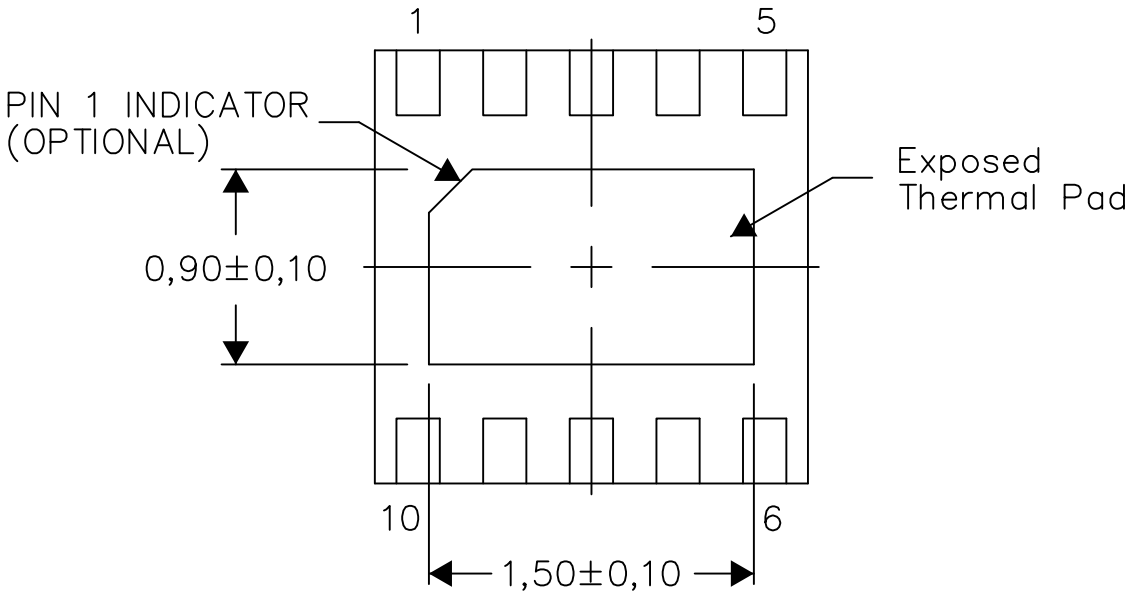
DSQ (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



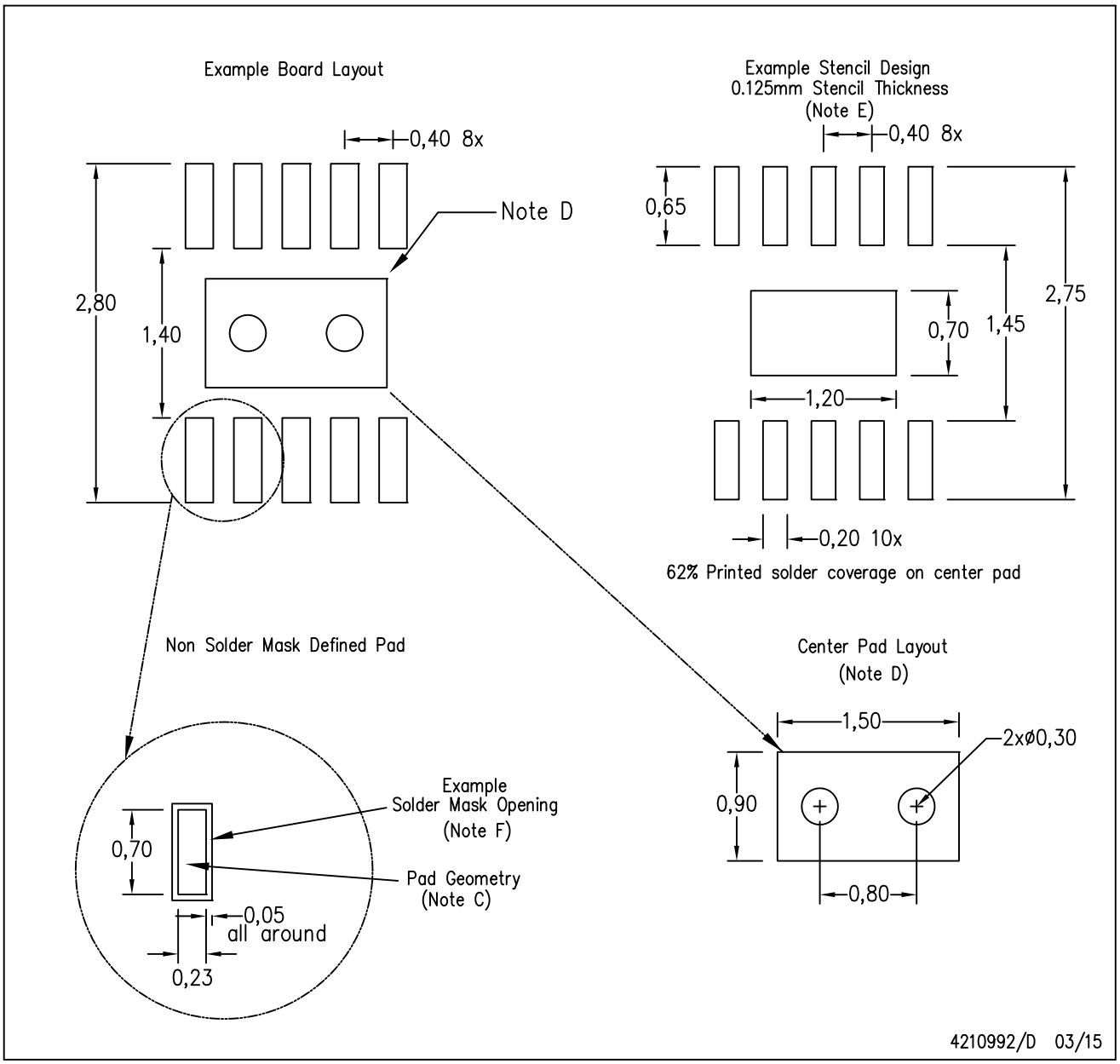
Bottom View

Exposed Thermal Pad Dimensions

4210993/E 06/15

NOTES: A. All linear dimensions are in millimeters

DSQ (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
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