PRECISION, LOW POWER INSTRUMENTATION AMPLIFIERS

Check for Samples: INA129-EP

FEATURES

- **Low Offset Voltage**
- **Low Input Bias Current**
- **High CMR**
- **Inputs Protected to ±40 V**
- **Wide Supply Range: ±2.25 V to ±18 V**
- **Low Quiescent Current**

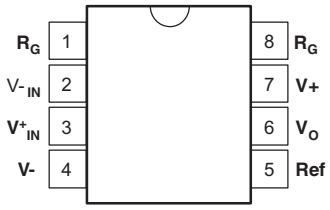
APPLICATIONS

- **Bridge Amplifier**
- **Thermocouple Amplifier**
- **RTD Sensor Amplifier**
- **Medical Instrumentation**
- **Data Acquisition**

SUPPORTS DEFENSE, AEROSPACE AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

D PACKAGE
(TOP VIEW)



(1) Custom temperature ranges available

DESCRIPTION

The INA129 is a low power, general purpose instrumentation amplifier offering excellent accuracy. The versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200 kHz at G = 100).

A single external resistor sets any gain from 1 to 10,000. The INA129 provides an industry-standard gain equation; the INA129 gain equation is compatible with the AD620.

The INA129 is laser trimmed for very low offset voltage, drift and high common-mode rejection (113 dB at G ≥ 100). It operates with power supplies as low as ±2.25 V, and quiescent current is only 750 µA - ideal for battery operated systems. Internal input protection can withstand up to ±40 V without damage.

The INA129 is available in an SO-8 surface-mount package specified for the –55°C to 125°C temperature range.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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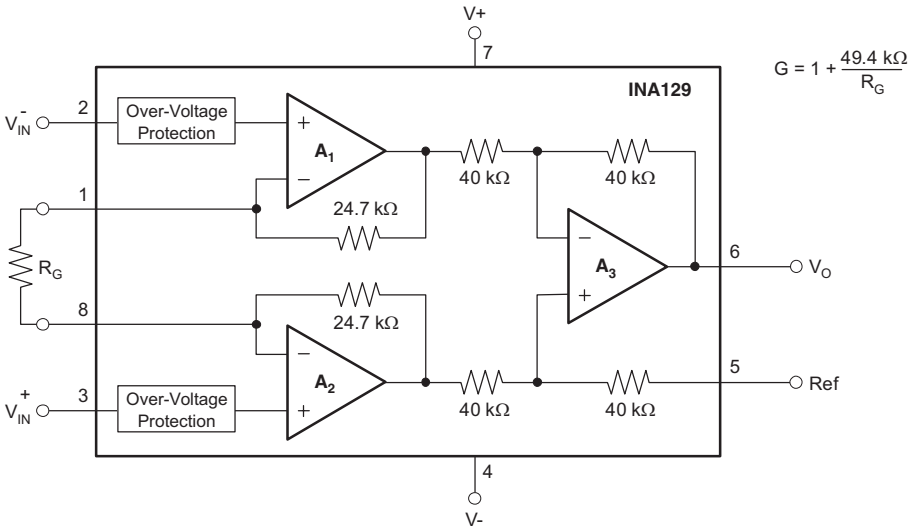
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC-D	INA129MDREP	129EP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_S	Supply voltage	±18	V
	Analog input voltage range	±40	V
	Output short-circuit (to ground)	Continuous	
T_A	Operating temperature	–55 to 125	°C
T_{STG}	Storage temperature range	–55 to 125	°C
T_J	Junction temperature	150	°C
	Lead temperature (soldering, 10s)	300	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

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ELECTRICAL CHARACTERISTICS

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ (unless otherwise noted)
Boldface limits apply over the specified temperature range, T_A = –55°C to 125°C.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT						
Offset Voltage, RTI						
Initial	T_A = 25°C				±100 ±800/G	µV
	Over temperature				**±150 ±2050/G**	
vs power supply	T_A = 25°C, V_S = ±2.25 V to ±18 V				±1.6 ±175/G	µV/V
	Over temperature				**±1.8 ±175/G**	
Long-term stability				±1 ±3/G		µV/mo
Impedance, differential				10^{10} || 2		Ω || pF
Common mode				10^{11}||9		Ω || pF
Common mode voltage range(1)	V_O = 0 V		(V+) − 2	(V+) − 1.4		V
			(V−) + 2	(V−) + 1.7		V
Safe input voltage					±40	V
Common-mode rejection	V_{CM} = ±13 V, ΔR_S = 1 kΩ	G = 1	75	86		dB
		Over temperature	**67**			
		G = 10	93	106		
		Over temperature	**84**			
		G = 100	113	125		
		Over temperature	**98**			
		G = 1000	113	130		
		Over temperature	**98**			
CURRENT						
Bias current				±2	±8	nA
	Over temperature				**±16**	
Offset Current				±1	±8	nA
	Over temperature				**±16**	
NOISE						
Noise voltage, RTI	G = 1000, R_S = 0 Ω	f = 10 Hz		10		nV/√Hz
		f = 100 Hz		8		
		f = 1 kHz		8		
		f_B = 0.1 Hz to 10 Hz		0.2		µVpp
Noise current	G = 1000, R_S = 0 Ω	f = 10 Hz		0.9		pA/√Hz
		f = 1 kHz		0.3		
		f_B = 0.1 Hz to 10 Hz		30		pA_{PP}
GAIN						
Gain equation				1 + (49.4 kΩ/R_G)		V/V
Range of gain			1		10000	V/V
Gain error	G = 1			±0.05	±0.1	%
	Over temperature				**±0.15**	
	G = 10			±0.02	±0.5	
	Over temperature				**±0.65**	
	G = 100			±0.05	±0.65	
	Over temperature				**±1.1**	
	G = 1000			±0.5	±2	

(1) Input common-mode range varies with output voltage — see typical curves.

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ELECTRICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ (unless otherwise noted)
Boldface limits apply over the specified temperature range, T_A = –55°C to 125°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain vs temperature (2)		G = 1		±1	±10	ppm/°C
49.4-kΩ resistance (2) (3)				±25	±100	ppm/°C
Nonlinearity		V_O = ±13.6 V, G = 1		±0.0001	±0.0018	% of FSR
		Over temperature			**±0.0035**	
		G = 10		±0.0003	±0.0035	
		Over temperature			**±0.0055**	
		G = 100		±0.0005	±0.0035	
		Over temperature			**±0.0055**	
		G = 1000		±0.001	See (4)	
OUTPUT						
Voltage	Positive	R_L = 10 kΩ	(V+) − 1.4	(V+) − 0.9		V
	Negative	R_L = 10 kΩ	(V−) + 1.4	(V−) + 0.8		
Load capacitance stability				1000		pF
Short-circuit current				+6/−15		mA
FREQUENCY RESPONSE						
Bandwidth, −3 dB		G = 1		1300		kHz
		G = 10		700		
		G = 100		200		
		G = 1000		20		
Slew rate		V_O = ±10 V, G = 10		4		V/µs
Settling time, 0.01%		G = 1		7		µs
		G = 10		7		
		G = 100		9		
		G = 1000		80		
Overload recovery		50% overdrive		4		µs
POWER SUPPLY						
Voltage range			±2.25	±15	±18	V
Current, total		V_{IN} = 0 V		±700	±750	µA
		Over temperature			**±1200**	
TEMPERATURE RANGE						
Specification			−55		125	°C
Operating			−55		125	°C
θ_{JA}	8-pin DIP			80		°C/W
	SO-8 SOIC			150		

(2) Specified by wafer test.
(3) Temperature coefficient of the 49.4-kΩ term in the gain equation.
(4) Nonlinearity measurements in G = 1000 are dominated by noise. Typical nonlinearity is ±0.001%.

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TYPICAL CHARACTERISTICS

At T_A = 25°C, V_S = ±15 V, unless otherwise noted.

GAIN vs FREQUENCY

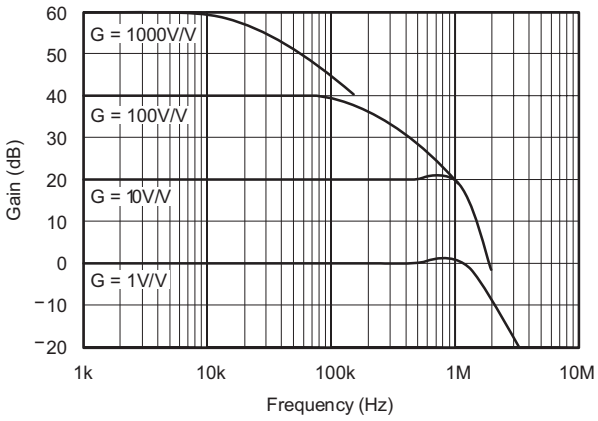

Figure 1.

COMMON-MODE REJECTION vs FREQUENCY

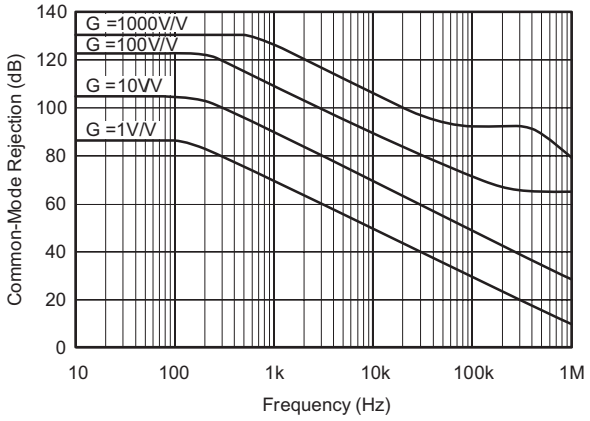

Figure 2.

POSITIVE POWER SUPPLY REJECTION vs FREQUENCY

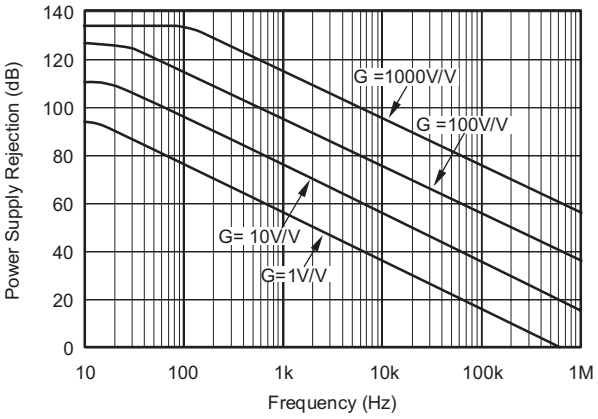

Figure 3.

NEGATIVE POWER SUPPLY REJECTION vs FREQUENCY

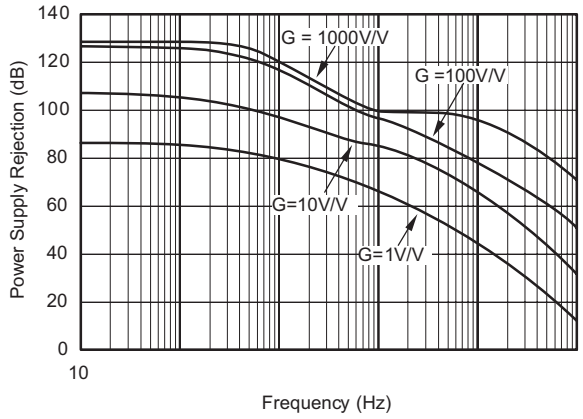

Figure 4.

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TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = ±15 V, unless otherwise noted.

INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE (V_S = ±15 V)

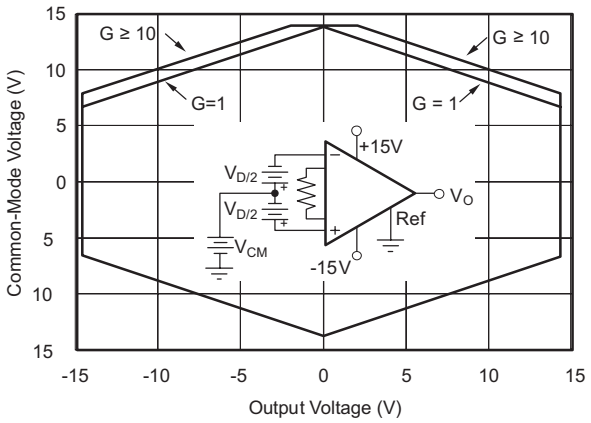

Figure 5.

INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE (V_S = ±5 V, ±2.5 V)

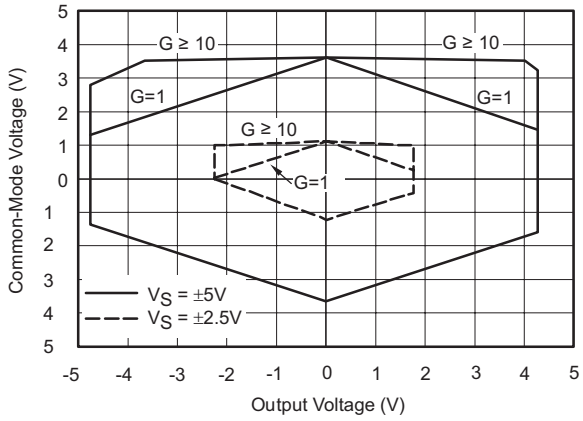

Figure 6.

INPUT-REFERRED NOISE vs FREQUENCY

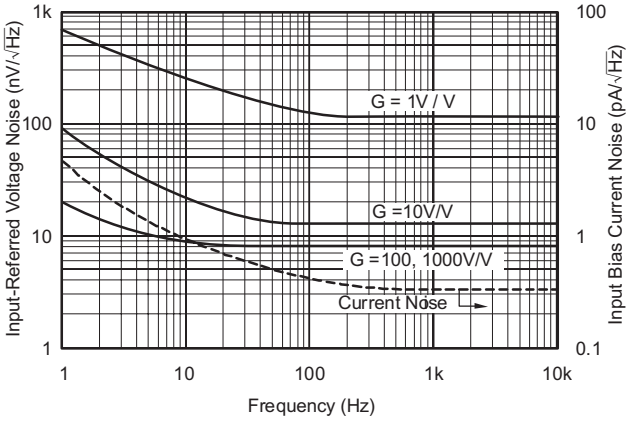

Figure 7.

SETTLING TIME vs GAIN

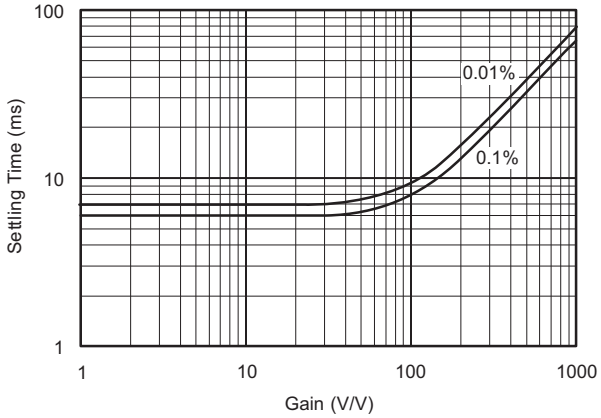

Figure 8.

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TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = ±15 V, unless otherwise noted.

QUIESCENT CURRENT AND SLEW RATE vs TEMPERATURE

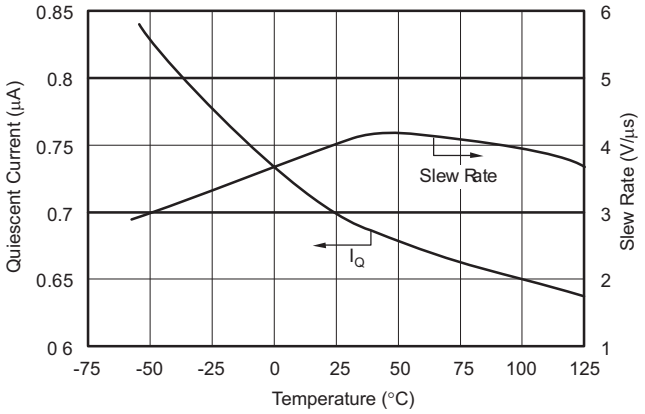

Figure 9.

INPUT OVER-VOLTAGE V/I CHARACTERISTICS

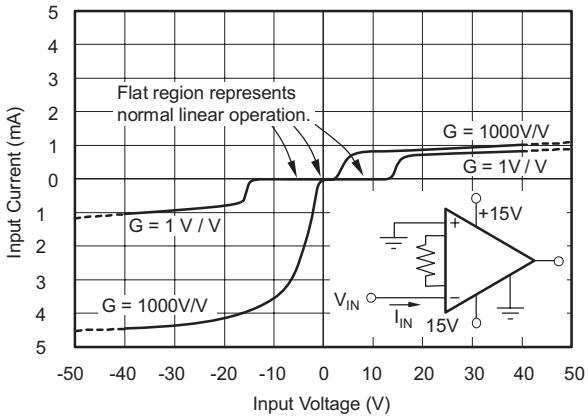

Figure 10.

INPUT OFFSET VOLTAGE WARM-UP

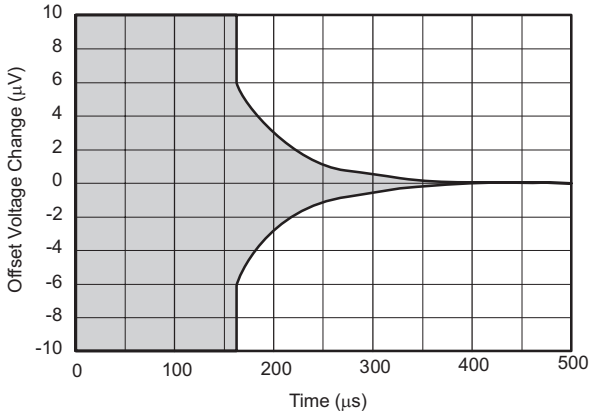

Figure 11.

INPUT BIAS CURRENT vs TEMPERATURE

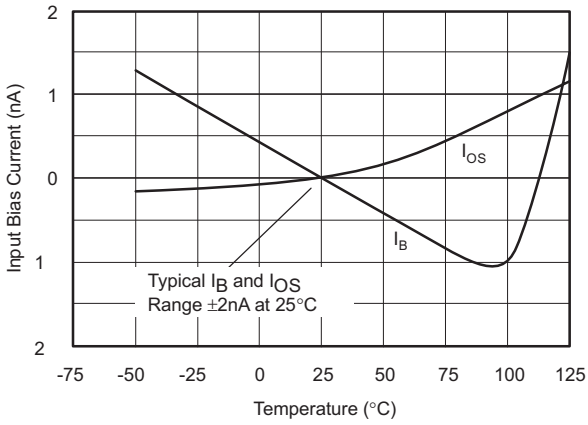

Figure 12.

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TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = ±15 V, unless otherwise noted.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

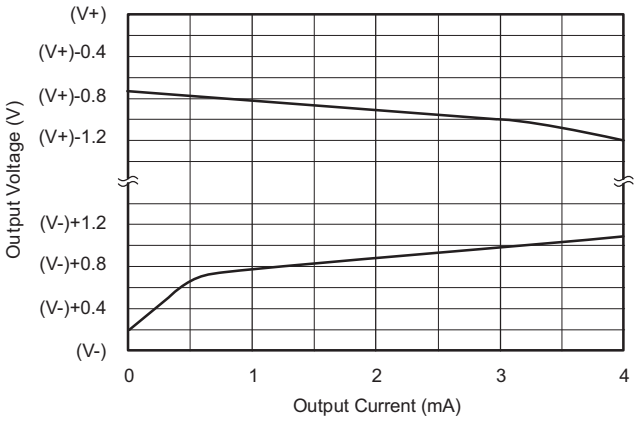

Figure 13.

OUTPUT VOLTAGE SWING vs POWER SUPPLY VOLTAGE

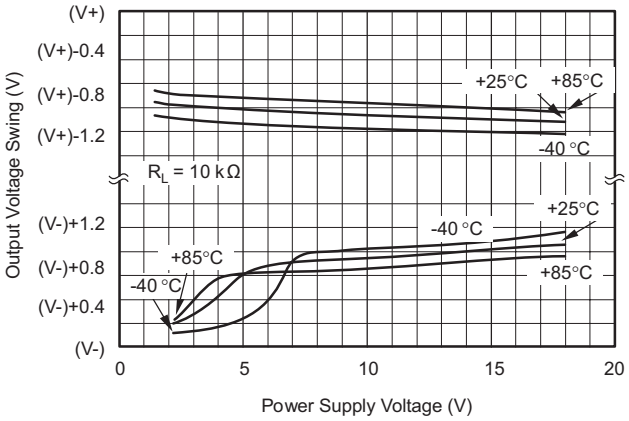

Figure 14.

SHORT-CIRCUIT OUTPUT CURRENT vs TEMPERATURE

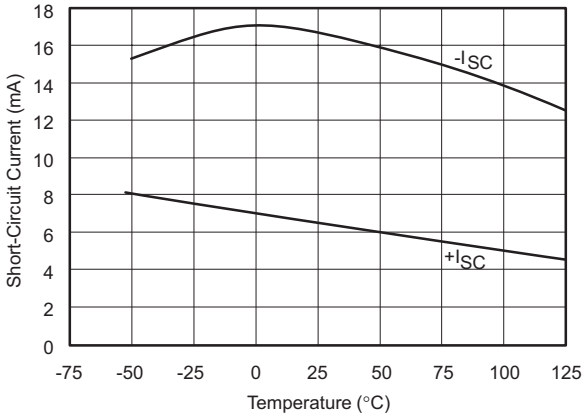

Figure 15.

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

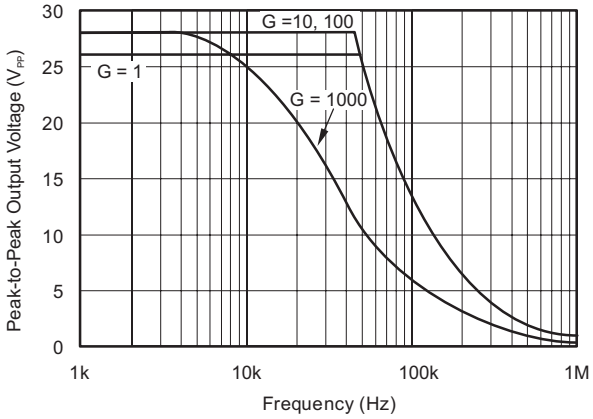

Figure 16.

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TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = ±15 V, unless otherwise noted.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

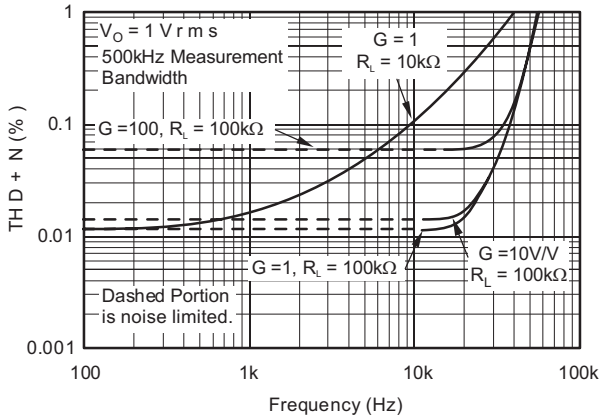

Figure 17.

SMALL SIGNAL (G = 1, 10)

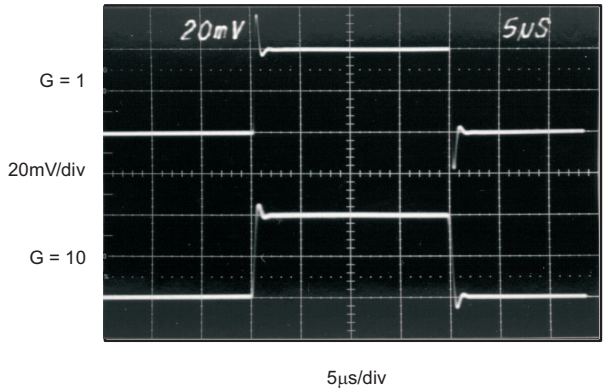

Figure 18.

SMALL SIGNAL (G = 100, 1000)

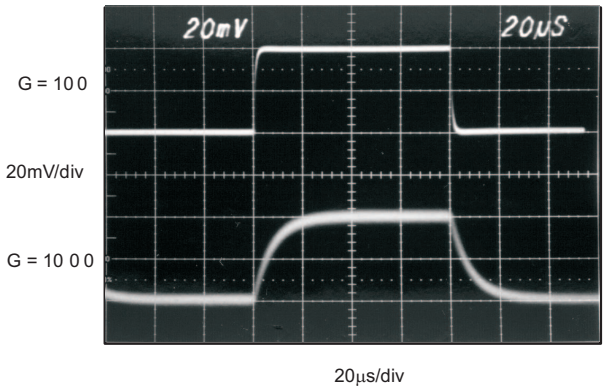

Figure 19.

LARGE SIGNAL (G = 1, 10)

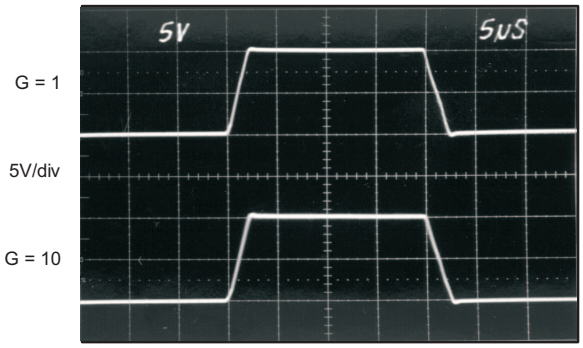

Figure 20.

LARGE SIGNAL (G = 100, 1000)

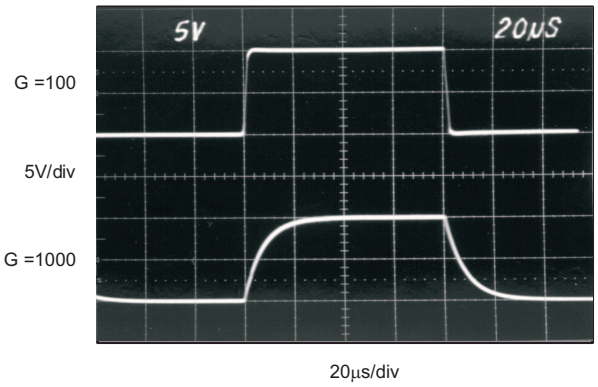

Figure 21.

VOLTAGE NOISE 0.1 Hz TO 10 Hz INPUT-REFERRED, G ≥ 100

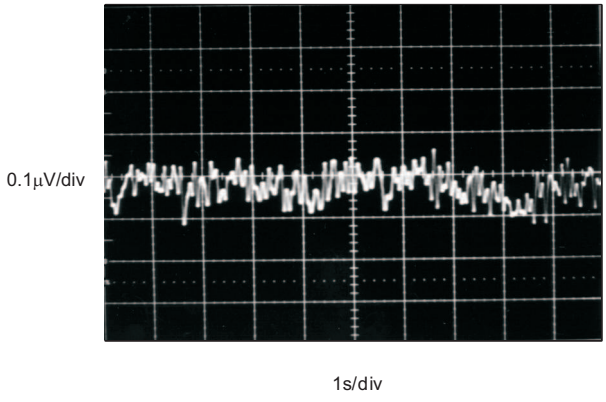

Figure 22.

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APPLICATION INFORMATION

Figure 23 shows the basic connections required for operation of the INA129. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 8 Ω in series with the Ref pin will cause a typical device to degrade to approximately 80 dB CMR (G = 1).

Setting the Gain

Gain is set by connecting a single external resistor, R_G, between pins 1 and 8.

$$G = 1 + \frac{49.4\ \text{k}\Omega}{R_G} \tag{1}$$

Commonly used gains and resistor values are shown in Figure 23.

The 49.9-kΩ term in Equation 1 comes from the sum of the two internal feedback resistors of A1 and A2. These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these internal resistors are included in the gain accuracy and drift specifications of the INA129.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from Equation 1. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

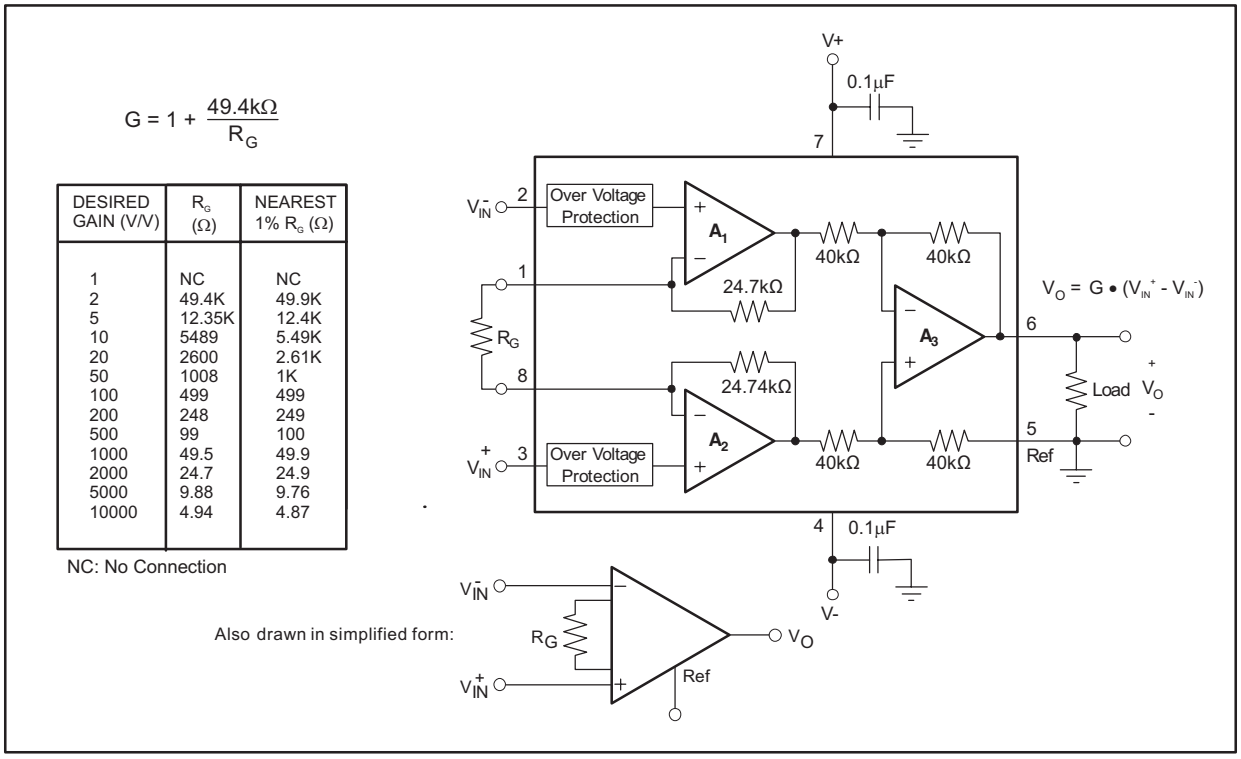

Figure 23. Basic Connections

Dynamic Performance

Figure 1 shows that, despite its low quiescent current, the INA129 achieves wide bandwidth, even at high gain. This is due to the current-feedback topology of the input stage circuitry. Settling time also remains excellent at high gain.

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Noise Performance

The INA129 provides very low noise in most applications. Low frequency noise is approximately 0.2 μVPP measured from 0.1 Hz to 10 Hz (G ≥ 100). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

Offset Trimming

The INA129 is laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 24 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed with the output. The operational amplifier buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

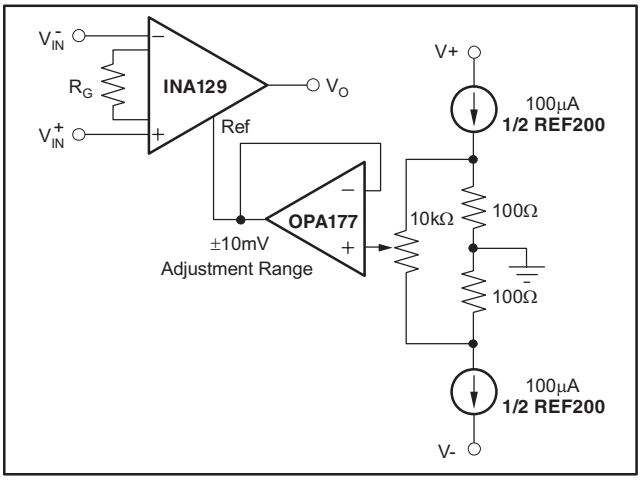

Figure 24. Optional Trimming of Output Offset Voltage

Input Bias Current Return Path

The input impedance of the INA129 is extremely high (approximately 10^{10} Ω). However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±2 nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 25 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range, and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 25). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

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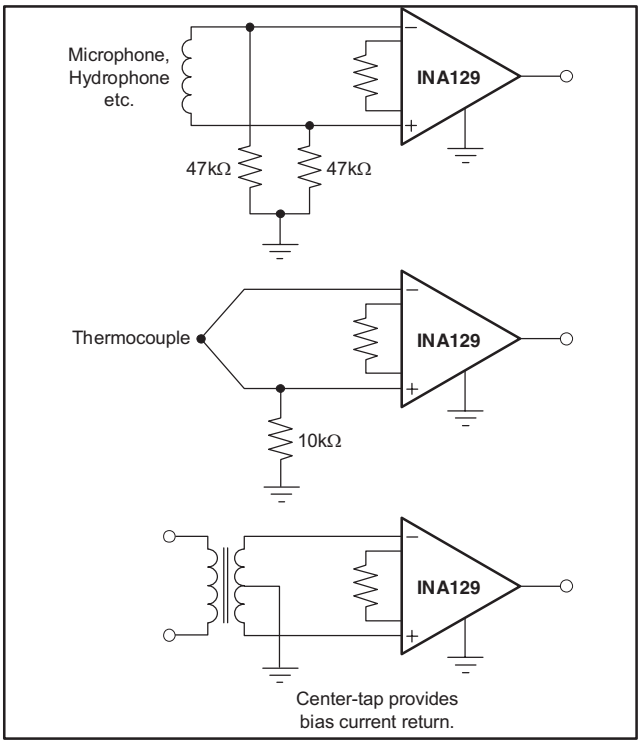

Figure 25. Providing an Input Common-Mode Current Path

Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA129 is from approximately 1.4 V below the positive supply voltage to 1.7 V above the negative supply. As a differential input voltage causes the output voltage increase, however, the linear input range will be limited by the output voltage swing of amplifiers A1 and A2. So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage (see Figure 5 and Figure 6).

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of A3 will be near 0 V even though both inputs are overloaded.

Low Voltage Operation

The INA129 can be operated on power supplies as low as ±2.25 V. Performance remains excellent with power supplies ranging from ±2.25 V to ±18 V. Most parameters vary only slightly throughout this supply voltage range.

Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Figure 5 and Figure 6 show the range of linear operation for ±15 V, ±5 V, and ±2.5 V supplies.

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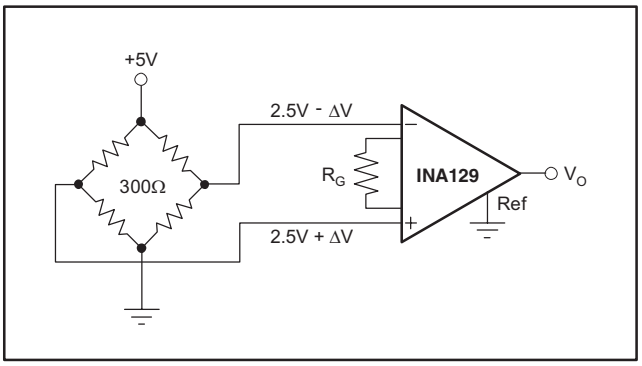


Figure 26. Bridge Amplifier

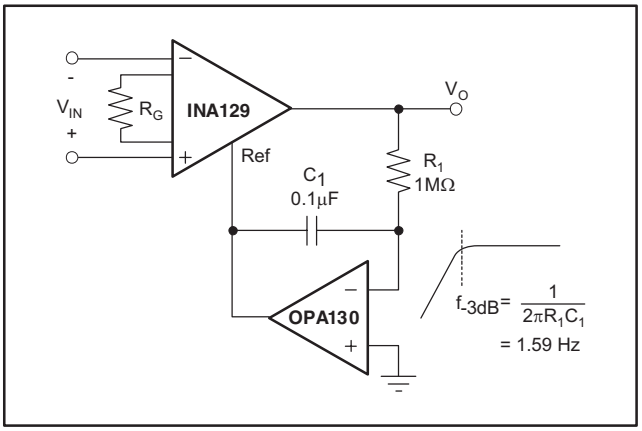
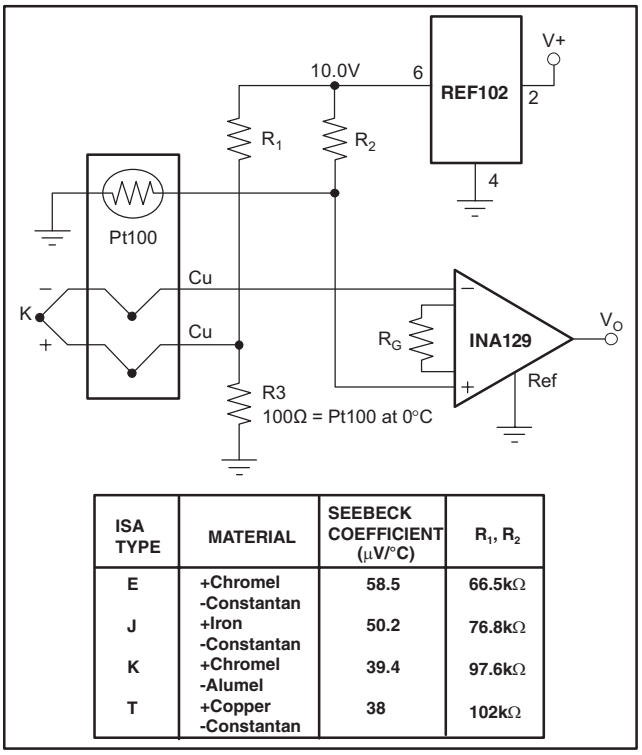
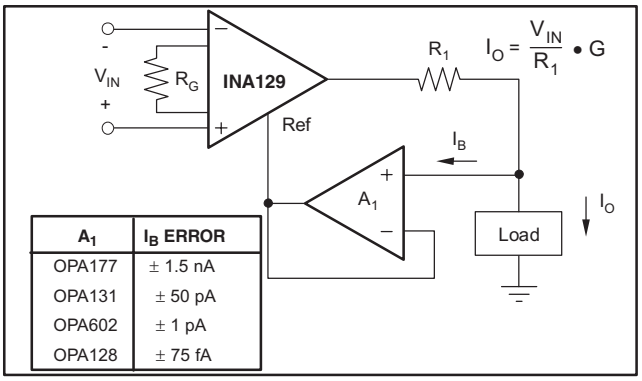


Figure 27. AC-Coupled Instrumentation Amplifier



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (μV/°C)	R1, R2
E	+Chromel -Constantan	58.5	66.5kΩ
J	+Iron -Constantan	50.2	76.8kΩ
K	+Chromel -Alumel	39.4	97.6kΩ
T	+Copper -Constantan	38	102kΩ

Figure 28. Thermocouple Amplifier With RTD Cold-Junction Compensation



A1	IB ERROR
OPA177	± 1.5 nA
OPA131	± 50 pA
OPA602	± 1 pA
OPA128	± 75 fA

Figure 29. Differential Voltage to Current Converter

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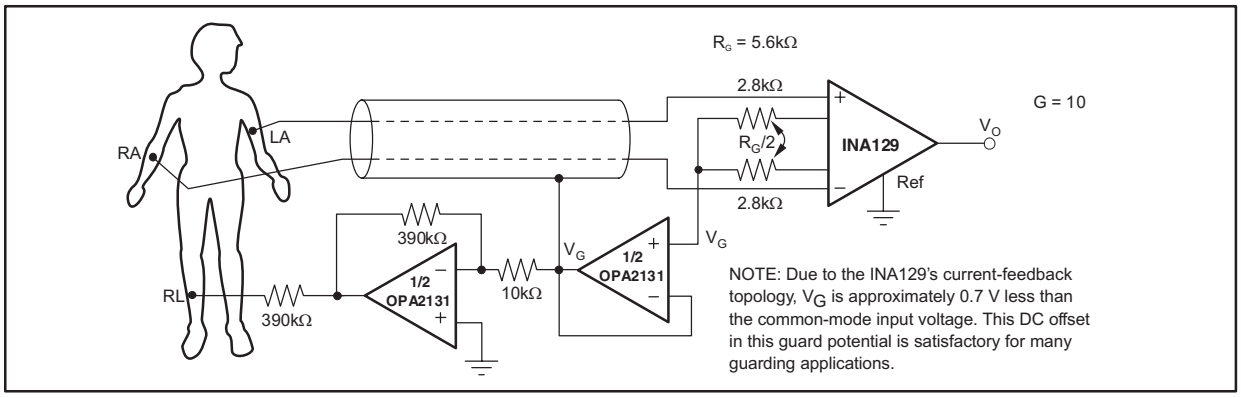

Figure 30. ECG Amplifier With Right-Leg Drive

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
INA129MDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
V62/10605-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF INA129-EP :

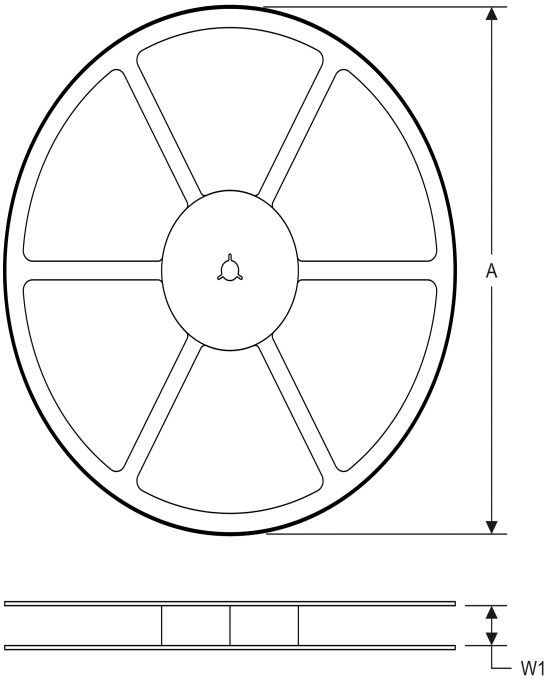
- Catalog: INA129

NOTE: Qualified Version Definitions:

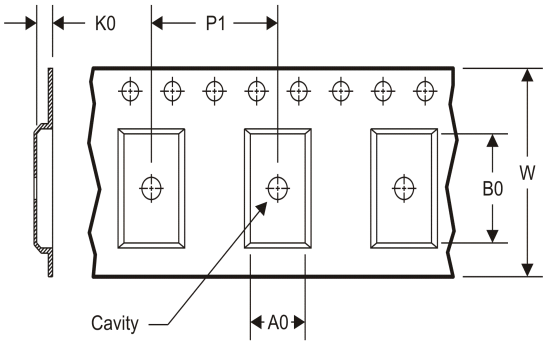
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



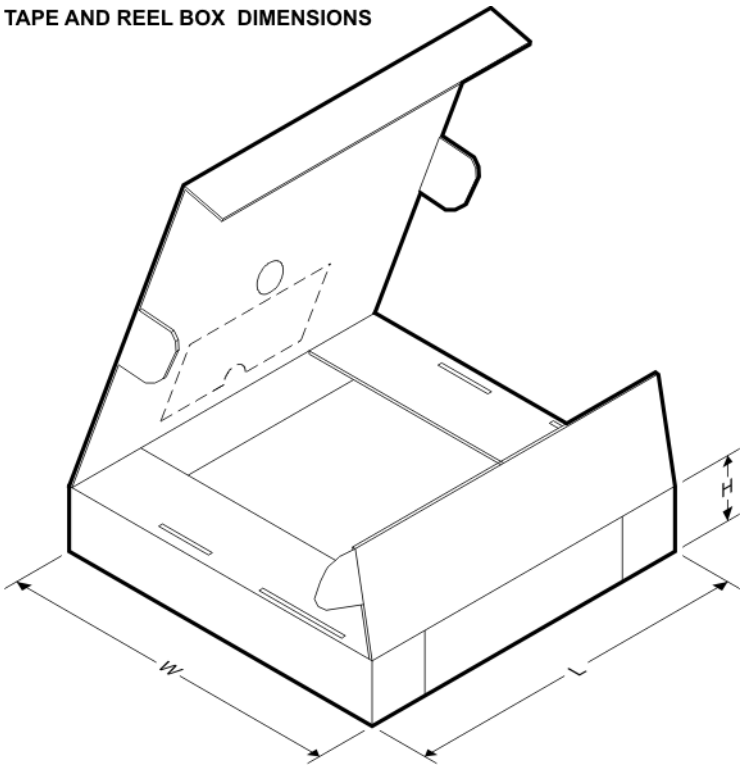
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA129MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

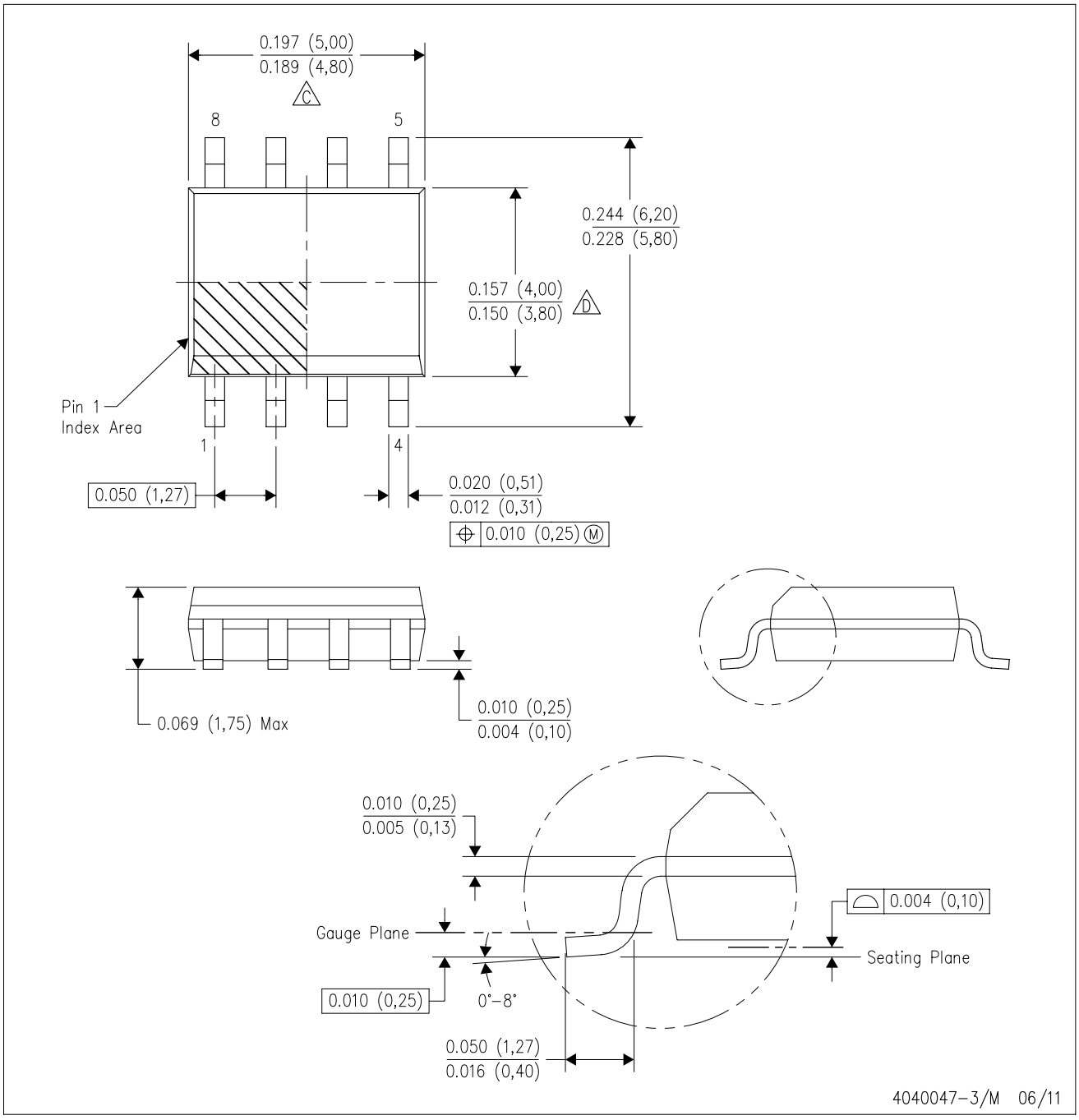
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

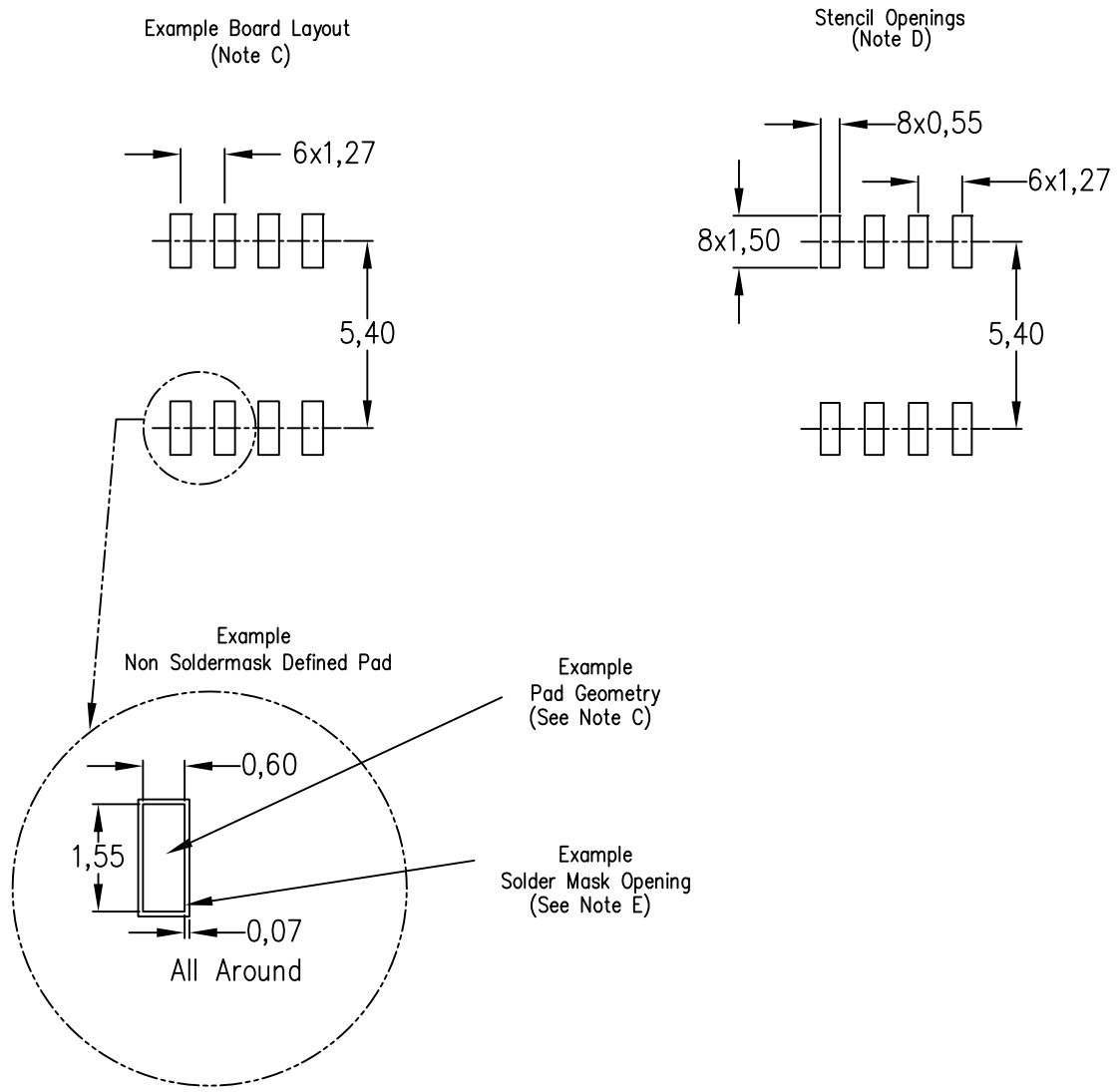
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA129MDREP	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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