Low Noise, Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

INA-01100

Features

- **Cascadable 50 Ω Gain Block**
- **Low Noise Figure:** 1.7 dB Typical at 100 MHz
- **High Gain:** 32.5 dB Typical at 100 MHz
- **3 dB Bandwidth:** DC to 500 MHz
- **Unconditionally Stable (k>1)**

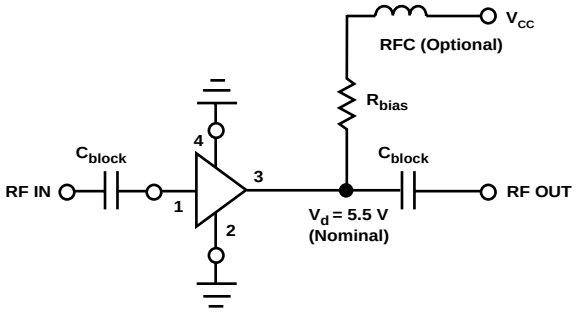
Description

The INA-01100 is a low-noise silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) feedback amplifier chip. It is designed for narrow or wide bandwidth industrial and military applications that require high gain and low noise IF or RF amplification.

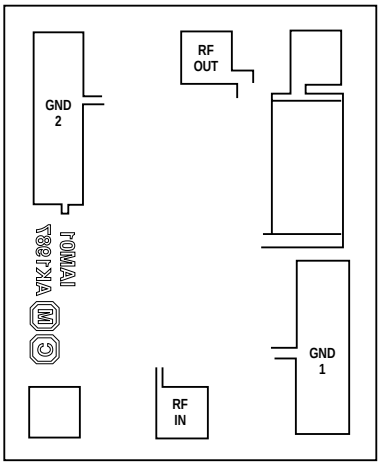
The INA series of MMICs is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX}, ISOSAT™-I silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide intermetal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.[1]

Typical Biasing Configuration



Chip Outline[1]



Note:

1. See Application Note, "A005: Transistor Chip Use" for additional information.

INA-01100 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	50 mA
Power Dissipation[2,3]	400 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance:
$\theta_{jc} = 60°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{Mounting\ Surface}$ (T_{MS}) = 25°C.
3. Derate at 16.7 mW/°C for T_{MS} > 176°C.

INA-01100 Electrical Specifications[1,3], T_A = 25°C

Symbol	Parameters and Test Conditions[2]: I_d = 35 mA, Z_O = 50 Ω		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 100 MHz	dB		32.5	
ΔG_P	Gain Flatness	f = 10 to 250 MHz	dB		±0.5	
$f_{3\ dB}$	3 dB Bandwidth		MHz		500	
ISO	Reverse Isolation ($\|S_{12}\|^2$)	f = 10 to 250 MHz	dB		39	
VSWR	Input VSWR	f = 10 to 250 MHz			1.6:1	
	Output VSWR	f = 10 to 250 MHz			1.5:1	
NF	50 Ω Noise Figure	f = 100 MHz	dB		1.7	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 100 MHz	dBm		11	
IP_3	Third Order Intercept Point	f = 100 MHz	dBm		23	
t_D	Group Delay	f = 100 MHz	psec		200	
V_d	Device Voltage		V	4.0	5.5	7.0
dV/dT	Device Voltage Temperature Coefficient		mV/°C		+10	

Notes:
1. The recommended operating current range for this device is 30 to 40 mA. Typical performance as a function of current is on the following page.
2. RF performance of the chip is determined by packaging and testing 10 devices per wafer.
3. The values are the achievable performance for the INA-01100 mounted in a 70 mil stripline package.

INA-01100 Typical Scattering Parameters[1] (Z_O = 50 Ω, T_A = 25°C, V_{CC} = 35 mA)

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		
GHz	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	k
0.01	0.09	–16	32.7	43.4	–1	–38.5	.012	–1	.18	1	1.17
0.05	0.10	–27	32.7	43.1	–10	–38.6	.012	15	.19	5	1.18
0.10	0.11	–5	32.4	41.9	–20	–38.4	.012	–8	.20	10	1.17
0.20	0.14	–80	31.6	38.0	–37	–38.6	.012	4	.24	14	1.22
0.30	0.18	–98	30.5	33.7	–52	–38.8	.011	–10	.27	15	1.31
0.40	0.20	–110	29.4	29.6	–65	–39.6	.011	2	.30	10	1.51
0.50	0.22	–115	28.4	26.2	–75	–38.6	.012	–12	.32	6	1.48
0.60	0.24	–120	27.4	23.4	–84	–39.1	.011	–7	.34	1	1.67
0.80	0.27	–124	25.7	19.3	–100	–38.3	.012	–6	.36	–11	1.76
1.00	0.30	–127	24.3	16.3	–115	–36.1	.016	–5	.36	–22	1.58
1.5	0.44	165	21.8	12.37	–179	–33.6	.020	42	.19	–69	1.75
2.0	0.44	154	17.9	7.88	146	–33.0	.022	42	.13	–106	2.42
2.5	0.46	148	14.6	5.36	121	–30.6	.029	36	.12	–151	2.63
3.0	0.48	139	11.4	3.71	96	–30.0	.032	45	.10	159	3.31

Note:
1. S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section of the *Communications Components Designer's* Catalog.

INA-01100 Typical Performance, T_A = 25°C

(unless otherwise noted: The values are the achievable performance for the INA-01100 mounted in a 70 mil stripline package.)

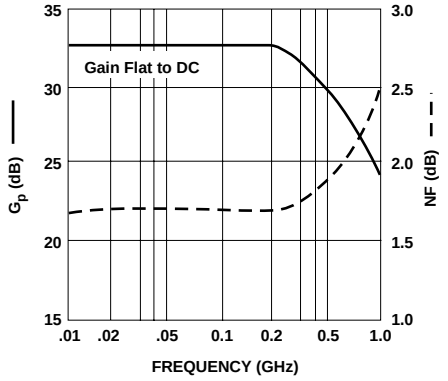


Figure 1. Typical Gain and Noise Figure vs. Frequency, T_A = 25°C, I_d = 35 mA

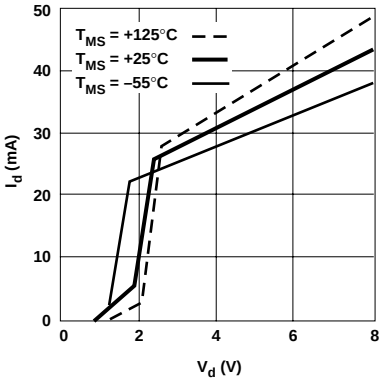


Figure 2. Device Current vs. Voltage.

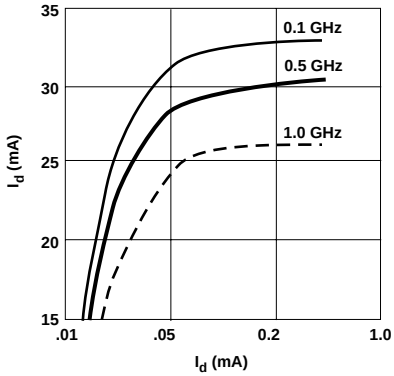


Figure 3. Power Gain vs. Current.

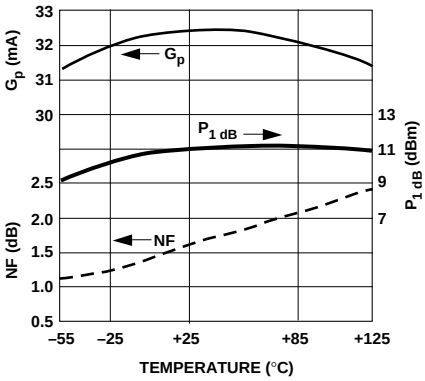


Figure 4. Output Power and 1 dB Gain Compression, NF and Power Gain vs. CaseTemperature. f = 0.1 GHz, I_d = 35 mA.

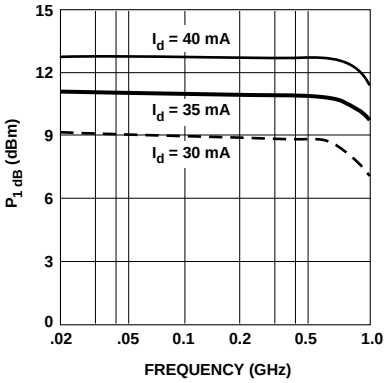


Figure 5. Output Power at 1 dB Gain Compression vs. Frequency.

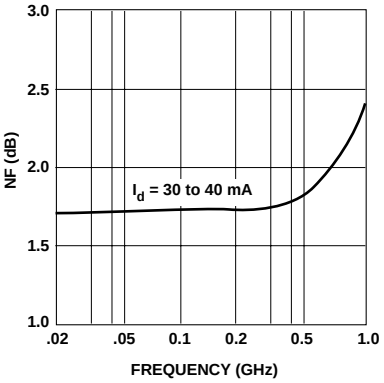
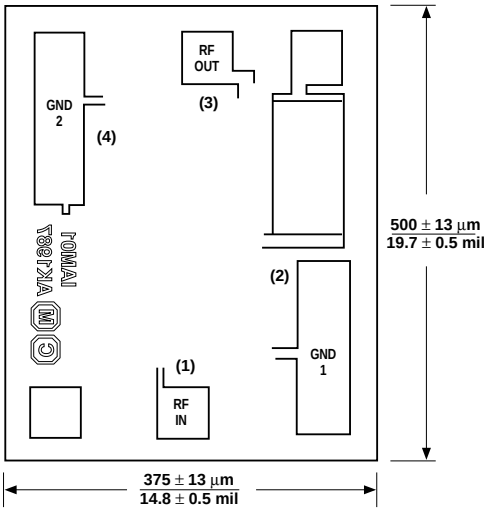


Figure 6. Noise Figure vs. Frequency.

INA-01100 Chip Dimensions



Chip thickness is 140 µm/5.5 mil. Bond Pads are 41 µm/1.6 mil typical on each side. Note: Ground Bonding is Critical. Refer to Application Bulletin, "AB-0007: INA Bonding Configuration".