9-Line SCSI Terminator
– 35MHz Channel Bandwidth

The IMP5115 SCSI terminator is part of IMP's family of high-performance, adaptive, non-linear mode SCSI products, which are designed to deliver true UltraSCSI performance in SCSI applications. The low voltage BiCMOS architecture employed in its design offers performance superior to older linear passive and active techniques. IMP's SCSI termination architecture employs high-speed adaptive elements for each channel, thereby providing the fastest response possible — typically 35MHz, which is 100 times faster than the older linear regulator/terminator approach used by other manufacturers. Products using this older linear regulator approach have bandwidths which are dominated by the output capacitor and which are limited to 500KHz (see further discussion in the Functional Description section). This new architecture also eliminates the output compensation capacitor required in earlier terminator designs. Each is approved for use with SCSI-1, -2, -3, UltraSCSI and beyond — providing the highest performance alternative available today.

Another key improvement offered by the IMP5115 lies in its ability to insure reliable, error-free communications even in systems which do not adhere to recommended SCSI hardware design guidelines, such as the use of improper cable lengths and impedances. Frequently, this situation is not controlled by the peripheral or host designer and, when problems occur, they are the first to be made aware of the problem. The IMP5115 architecture is much more tolerant of marginal system integrations.

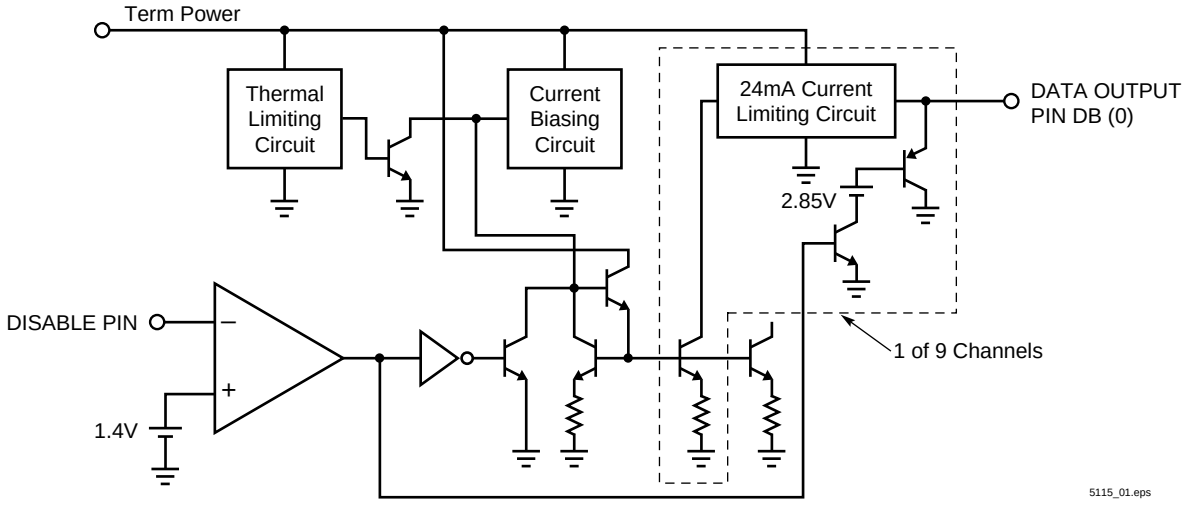
Recognizing the needs of portable and configurable peripherals, the IMP5115 has a TTL compatible sleep/disable mode. Quiescent current is typically 375µA in this mode, while the output capacitance is also less than 3pF. The obvious advantage of extended battery life for portable systems is inherent in the product's sleep-mode feature. Additionally, the disable function permits factory-floor or production-line configurability, reducing inventory and product-line diversity costs. Field configurability can also be accomplished without physically removing components which, often times results in field returns due to mishandling.

Reduced component count is also inherent in the IMP5115 architecture. Traditional termination techniques require large stabilization and transient protection capacitors of up to 20µF in value and size. The IMP5115 architecture does not require these components, allowing all the cost savings associated with inventory, board space, assembly, reliability, and component costs.

Key Features

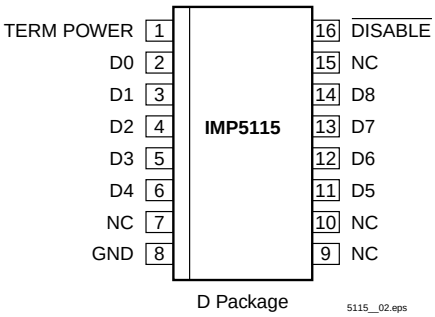
- Ultra-Fast response for Fast-20 SCSI applications
- 35MHz channel bandwidth
- 3.3V operation
- Less than 3pF output capacitance
- 375µA Sleep-mode current
- Thermally self limiting
- No external compensation capacitors
- Implements 8-bit or 16-bit (wide) applications
- Compatible with active negation drivers (60mA/channel)
- Compatible with passive and Active terminations
- Approved for use with SCSI 1, 2, 3 and UltraSCSI
- Hot swap compatible
- Pin-for-pin compatible with DS21S07A/2105

Block Diagrams



Pin Configuration

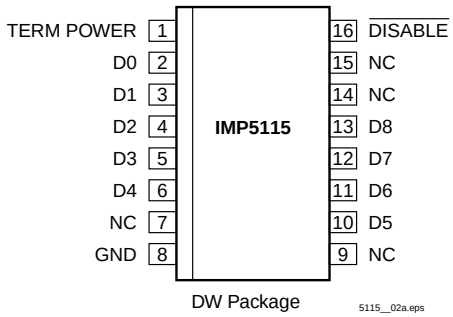
SO-16



D Package

5115__02.eps

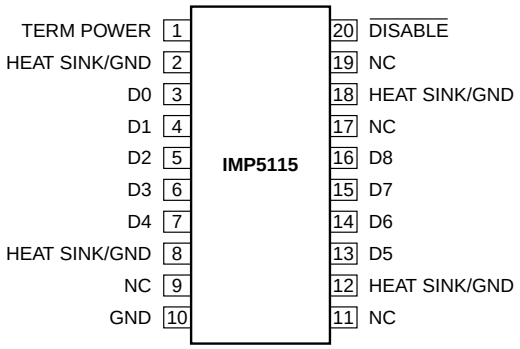
SOWB-16



DW Package

5115__02a.eps

TSSOP-20



PWP Package

5115_02b.eps

Ordering Information

Part Number	Temperature Range	Package
IMP5115CD	0°C to 125°C	16-pin Plastic SO
IMP5115CDT	0°C to 125°C	Tape and Reel, 16-pin Plastic SO
IMP5115CDW	0°C to 125°C	16-pin Plastic SOWB
IMP5115CDWT	0°C to 125°C	Tape and Reel, 16-pin Plastic SOWB
IMP5115CPWP	0°C to 125°C	20-pin Plastic TSSOP
IMP5115CPWPT	0°C to 125°C	Tape and Reel, 20-pin Plastic TSSOP

5115_t01.at3

Absolute Maximum Ratings[1]

Continuous Termination Voltage 10V
Continuous Output Voltage Range . . . . . 0V to 5.5V
Continuous Disable Voltage Range . . . . . 0V to 5.5V
Operating Junction Temperature . . . . . 0°C to 125°C
Storage Temperature Range . . . . . –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) . . . . . 300°C

Note: 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

Thermal Data

D Package:
Thermal Resistance Junction-to-Ambient, θ_{JA} . . . . . 120°C / W
DW Package:
Thermal Resistance Junction-to-Ambient, θ_{JA} . . . . . 95°C / W
PWP Package:
Thermal Resistance Junction-to-Ambient, θ_{JA} . . . . . 139°C / W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device / pc-board system. All of the ambient airflow is assumed.

Recommended Operating Conditions[2]

Parameter	Symbol	Min	Typ	Max	Units
TermPwr Voltage	V_{TERM}	4.0		5.5	V
High Level Enable Input Voltage	V_{IH}	2		V_{TERM}	V
Low Level Disable Input Voltage	V_{IL}	0		0.8	V
Operating Junction Temperature Range		0		125	°C

5115_t02.eps

Note: 2. Recommended operating conditions indicate the range over which the device is functional.

Electrical Characteristics

Unless otherwise specified, these specifications apply at an ambient operating temperature of T_A = 25°C. TermPwr = 4.75V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output High Voltage	V_{OUT}		2.65	2.85		V
TermPwr Supply Current	I_{CC}	All data lines = Open		6	9	mA
		All data lines = 0.5V		215	225	
		Disable Pin < 0.8V		375		µA
Output Current	I_{OUT}	V_{OUT} = 0.5V	–21	–23	–24	mA
Disable Input Current	I_{IN}	Disable Pin = 4.75V		10		nA
		Disable Pin = 0V		–90		µA
Output Leakage Current	I_{OL}	Disable Pin < 0.8V, V_O = 0.5V		10		nA
Capacitance in Disable Mode	C_{OUT}	V_{OUT} = 0V, Frequency = 1MHz		3		pF
Channel Bandwidth	BW			35		MHz
Termination Sink Current, per Channel	I_{SINK}	V_{OUT} = 4V		60		mA

5115_t03.eps

Application Information

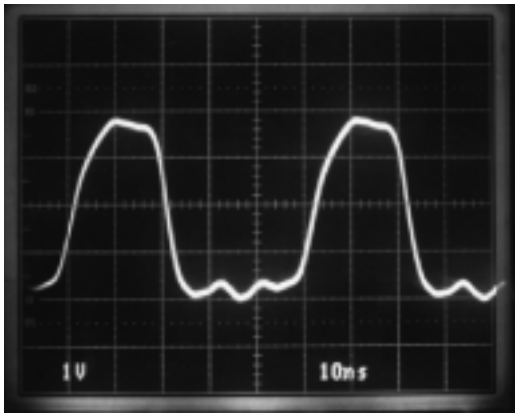


Figure 1. Receiving Waveform – 20MHz

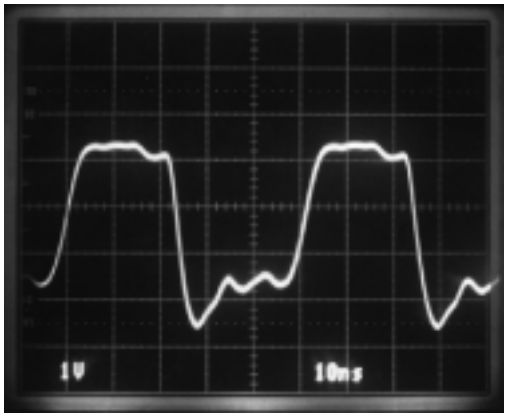


Figure 2. Driving Waveform – 20MHz

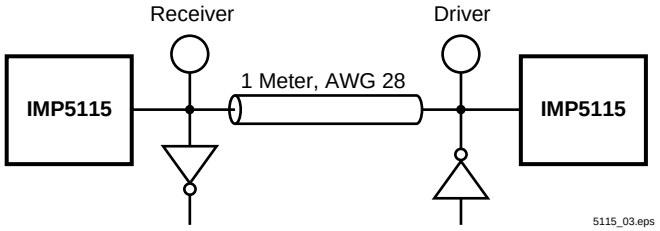


Figure 3.

IMP5115 Maximizes Line Current

Cable transmission theory suggests to optimize signal speed and quality, the termination should act both as an ideal voltage reference when the line is released (deasserted) and as an ideal current source when the line is active (asserted). Common active terminators which consist of linear regulators in series with resistors (typically 110Ω) are a compromise. With coventional linear terminators as the line voltage increases the amount of current decreases linearly by the equation;

$$\frac{(V_{REF} - V_{LINE})}{R} = I.$$

The IMP5115, with its unique new architecture, applies the maximum amount of current regardless of line voltage until the termination high threshold (2.85V) is reached.

Acting as a near ideal line terminator, the IMP5115 closely reproduces the optimum case when the device is enabled. To enable the device the Disable pin must be driven LOW. When enabled, quiescent current is 6mA and the device will respond to line demands by delivering 24mA on assertion and by imposing 2.85V on de-assertion.

Disable / Sleep Mode

Disable mode places the device in a sleep state, where quiescent current typically 375µA. When disabled, all outputs are in a high impedance state. Sleep mode can be used for power conservation or to remove the terminator from the SCSI chain.

An additional feature of the IMP5115 are their compatibility with active negation drivers.

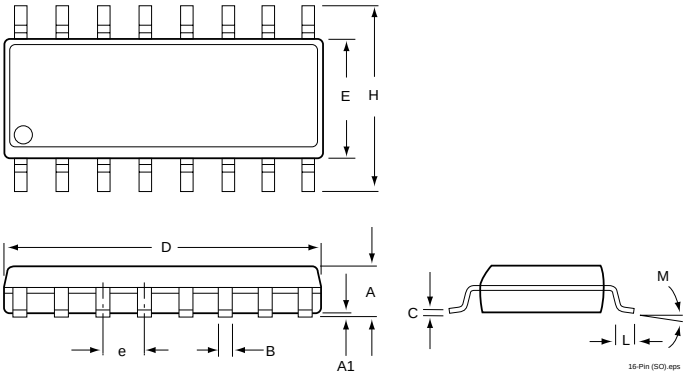
Table 1. Power Up/ Power Down Function Table

Disable	Outputs	Quiescent Current
H	Enabled	6mA
L	Disabled/High Impedance	375µA
Open	Enabled	6mA

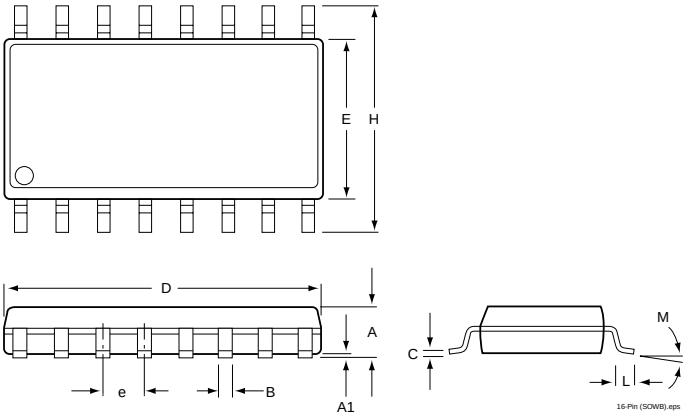
5115_t04.eps

Package Dimensions

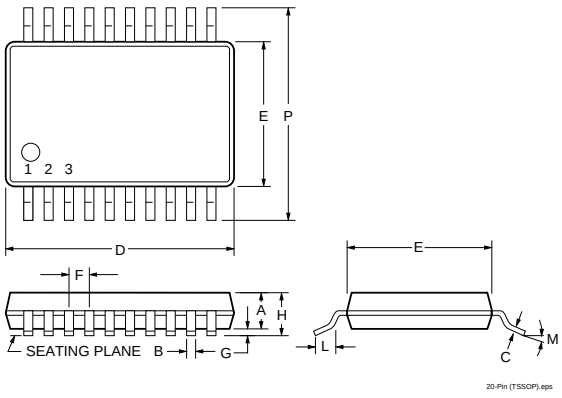
SO (16-Pin)



SOWB (16-Pin)



TSSOP (20-Pin)



	Inches		Millimeters	
	Min	Max	Min	Max
SO (16-Pin)*				
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.018	0.35	0.46
C	0.007	0.010	0.19	0.25
D	0.385	0.394	9.78	10.01
E	0.150	0.158	3.81	4.01
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.79	6.20
L	0.020	0.030	0.51	0.77
SOWB (16-Pin)				
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.010	0.018	0.25	0.46
C	0.009	0.013	0.23	0.32
D	—	0.420	—	10.67
E	0.295	0.305	7.49	7.75
e	0.050 BSC		1.27 BSC	
H	0.404	0.419	10.26	10.65
L	0.025	0.035	0.64	0.89
TSSOP (20-Pin)				
A	0.068	0.078	1.73	1.99
B	0.009	0.015	0.25	0.8
C	0.005	0.008	0.13	0.22
D	0.303	0.311	7.70	7.90
E	0.205	0.212	5.20	5.38
F	0.025 BSC		1.27 BSC	
G	0.002	0.008	0.05	0.21
H	0.064	0.072	1.63	1.83
L	0.025	0.037	0.65	0.95
M	0°	8°	0°	8°
P	0.301	0.311	7.65	7.90

** JEDEC Drawing MS-012AC*

5115_t05.at3

ISO 9001 Registered

IMP, Inc.
Corporate Headquarters
2830 N. First Street
San Jose, CA 95134-2071
Tel: 408-432-9100
Fax: 408-432-1085
e-mail: info@impinc.com
http://www.impweb.com

2002 © IMP, Inc.
Printed in USA
Publication #: 7006
Revision: C
Issue Date: 08/19/02
Type: Product