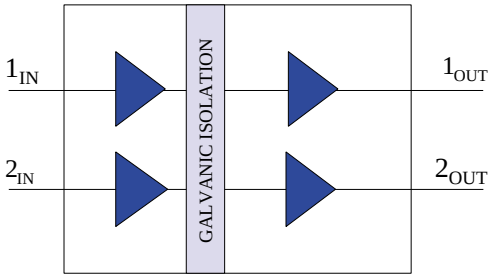
NVE CORPORATION

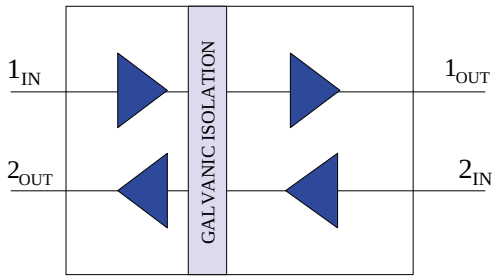
IL711/712 *IsoLoop®*

Dual Digital Isolator

Functional Diagram



IL711



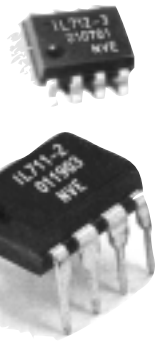
IL712

Ordering Information

Model	Package Type	
	8–PDIP	*8–SOIC*
IL711	-2	-3
IL712	-2	-3

IL711-2 is 8–PDIP package

IL712-3 is an 8–SOIC package



Features

- +5V and +3.3V CMOS Compatible
- 2 ns Typical Pulse Width Distortion
- 10 ns Typical Propagation Delay
- High Speed: 100 MBaud
- 2 ns Channel to Channel Skew
- 30 kV/µs Typical Transient Immunity
- 2500V_{RMS} Isolation (1 min)
- 8-pin PDIP and 8-pin SOIC Packages
- UL1577 Approved (File # E207481)
- IEC 61010-1 Approved (Report # 607057)

Applications

- Isolated Data Transmission
- Isolated ADCs and DACs
- Fieldbus Isolation
- High Speed Digital Systems
- Computer Peripheral Interfaces
- Logic Level Shifting

Description

The IL711 and IL712 offer the user a level of true logic integration in an isolation product not previously available. The high speed digital isolators are configured as dual unidirectional in the IL711, and as a bi-directional pair in the IL712. Both devices are integrated with patented* *IsoLoop®* technology giving them an excellent transient immunity specification. The symmetric magnetic coupling barrier gives these devices a propagation delay of only 10ns and a pulse width distortion of 2 ns.

Both the IL711 and the IL712 have 100Mbaud data rates which are independent of direction, i.e. the IL712 operates in full duplex mode making it ideal for many fieldbus bus applications. PROFIBUS / RS485 configurations are achieved by combinations of IL710 and the IL711 or IL712, either combination meeting the overall propagation delay requirements of the specification. Available in 8-pin PDIP and 8-pin SOIC packages, the IL711 and IL712 are specified over the temperature range of -40°C to +100°C without any derating in performance.

Isoloop® is a registered trademark of NVE Corporation

* US Patent number 5,831,426; 6,300,617 and others

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Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-55	175	°C
Ambient Operating Temperature(1)	T_A	-55	125	°C
Supply Voltage	V_{DD1},V_{DD2}	-0.5	7	Volts
Input Voltage	V_I	-0.5	V_{DD1}+0.5	Volts
Input Voltage	V_{OE}	-0.5	V_{DD2}+0.5	Volts
Output Voltage	V_O	-0.5	V_{DD2}+0.5	Volts
Drive Channel Output Current	I_O		10	mAmps
Lead Solder Temperature(10s)			260	°C
ESD	2kV Human Body Model			

Recommended Operating Conditions

Parameters	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	-40	100	°C
Supply Voltage	V_{DD1},V_{DD2}	3.0	5.5	Volts
Logic High Input Voltage	V_{IH}	2.4	V_{DD1}	Volts
Logic Low Input Voltage	V_{IL}	0	0.8	Volts
Input Signal Rise and Fall Times	t_{IR},t_{IF}		1	µsec

Insulation Specifications

Parameter	Condition	Min.	Typ.	Max.	Units
Barrier Impedance			$>10^{14}$ ||3		Ω ‖ pF
Creepage Distance (External)		7.036 (PDIP) 4.026 (SOIC)			mm
Leakage Current	240 V_{RMS} 60Hz		0.2		µAmps

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Capacitance (Input-Output)(5)	C_{I-O}		2		pF	f= 1MHz
Thermal Resistance (PDIP) Thermal Resistance (SOIC)	θ_{JCT} θ_{JCT}		150 240		°C/W °C/W	Thermocouple located at center underside of package
Package Power Dissipation	P_{PD}			150	mW	

IEC61010-1

TUV Certificate Numbers: B 01 07 44230 001 (PDIP)
B 01 07 44230 002 (SOIC)

Classification as Table 1.

Model	Pollution Degree	Material Group	Max Working Voltage	Package Type	
				8–PDIP	*8–SOIC*
IL710-2, IL711-2	II	III	300 VRMS	✓	
IL710-3, IL711-3	II	III	150 VRMS		✓

UL 1577

Component Recognition program. File # E207481
Rated 2500Vrms for 1min.

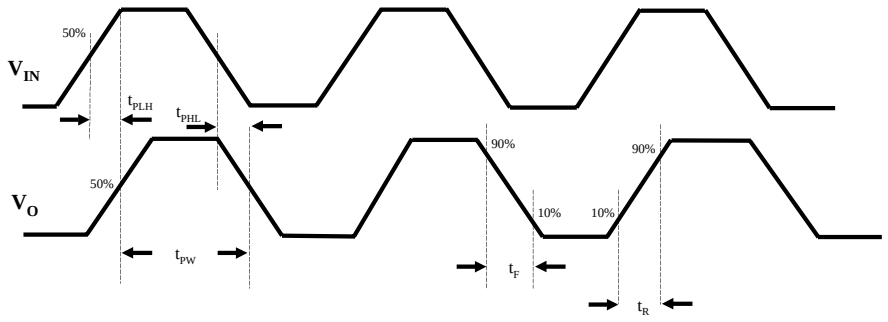
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Electrical Specifications

Electrical Specifications are T_{min} to T_{max} unless otherwise stated.

Parameter		Symbol	3.3 Volt Specifiations			5Volt Specifications			Units	Test Conditions
DC Specifications			**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**		
Input Quiescent Supply Current	IL711	I_{DD1}		9	14		12	20	µA	
	IL712			2.2	3.3		3	5	mA	
Output Quiescent Supply Current	IL711	I_{DD2}		2.2	3.3		4	5	mA	
	IL712			2.2	3.3		3	5	mA	
Logic Input Current		I_I	-10		10	-10		10	µA	
Logic High Output Voltage		V_{OH}	V_{DD}-0.1 0.8*V_{DD}	V_{DD} V_{DD}-0.5		V_{DD}-0.1 0.8*V_{DD}	V_{DD} V_{DD}-0.5		V	I_O =-20 µA, V_I =V_{IH} I_O = -4 mA, V_I =V_{IH}
Logic Low Output Voltage		V_{OL}		0 0.5	0.1 0.8		0 0.5	0.1 0.8	V	I_O = 20 µA, V_I =V_{IL} I_O = 4 mA, V_I =V_{IL}
Switching Specifications										
Maximum Data Rate			100	110		100	110		MBd	C_L = 15 pF
Pulse Width		PW	10			10			ns	
Propagation Delay Input to Output (High to Low)		t_{PHL}		12	18		10	15	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)		t_{PLH}		12	18		10	15	ns	C_L = 15 pF
Pulse Width Distortion[2] | tPHL- tPLH |		PWD		2	3		2	3	ns	C_L = 15 pF
Propagation Delay Skew[3]		t_{PSK}		4	6		4	6	ns	C_L = 15 pF
Output Rise Time (10-90%)		t_R		2	4		1	3	ns	C_L = 15 pF
Output Fall Time (10-90%)		t_F		2	4		1	3	ns	C_L = 15 pF
Transient Immunity (Output Logic High or Logic Low)[4]		|CMH| |CML|	20	30		20	30		kV/µs	Vcm =300V
Channel to Channel Skew		T_{CSK}		2	3		2	3	ns	C_L = 15 pF

Timing Diagram



Legend

t_{PLH}	Propagation Delay, Low to High
t_{PHL}	Propagation Delay, High to Low
t_{PW}	Minimum Pulse Width
t_R	Rise Time
t_F	Fall Time

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Notes:

1. Absolute Maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as $| t_{PHL} - t_{PLH} |$. %PWD is equal to the PWD divided by the pulse width.
3. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at 25°C.
4. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD}$. CM_L is the maximum common mode input voltage that can be sustained while maintaining $V_O < 0.8$ V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
5. Device is considered a two terminal device: pins 1–4 shorted and pins 5–8 shorted.

Application Notes:

Power Consumption

Isoloop® devices achieve their low power consumption from the manner by which they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5ns wide, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers whose power consumption is heavily dependent on its on-state and frequency.

The approximate power supply current per channel for *Isoloop*® is: $\mathbf{I(input) = 40 \cdot \frac{f}{fmax} \cdot \frac{1}{4} mA}$

where **f= operating frequency**
fmax= 50 MHz

Power Supplies

Because the IL711 and IL712 operate internally by using narrow current pulses, it is recommended that low ESR ceramic capacitors be used to decouple the supplies. 47nF capacitors should be placed as close to the device as possible between V_{DD1} and GND_1 as well as between V_{DD2} and GND_2.

Signal Status on Start-up and Shut Down

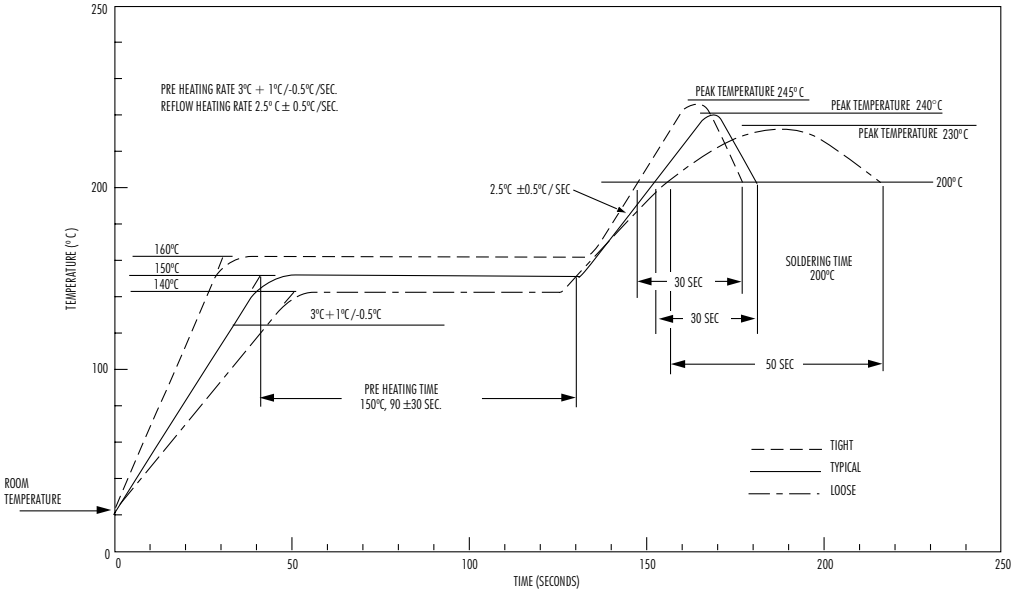
To minimize power dissipation, the input signals to the IL711 and IL712 are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider the inclusion of an initialization signal in his start–up circuit.

Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

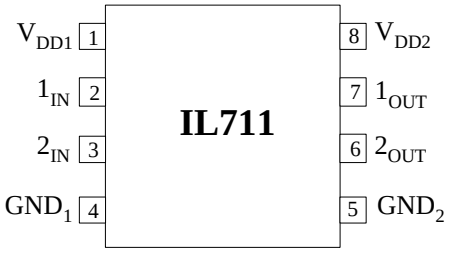
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IR Soldering Profile

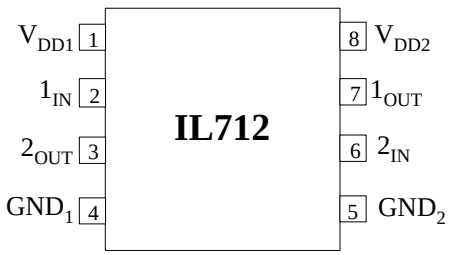


Pin Connections

1	V_{DD1}	Input Power Supply
2	1_{IN}	Channel 1 Logic Input Signal
3	2_{IN}	Channel 2 Logic Input Signal
4	GND_1	Input Power Supply Ground
5	GND_2	Output Power Supply Ground
6	2_{OUT}	Channel 2 Logic Output Signal
7	1_{OUT}	Channel 1 Logic Output Signal
8	V_{DD2}	Output Power Supply

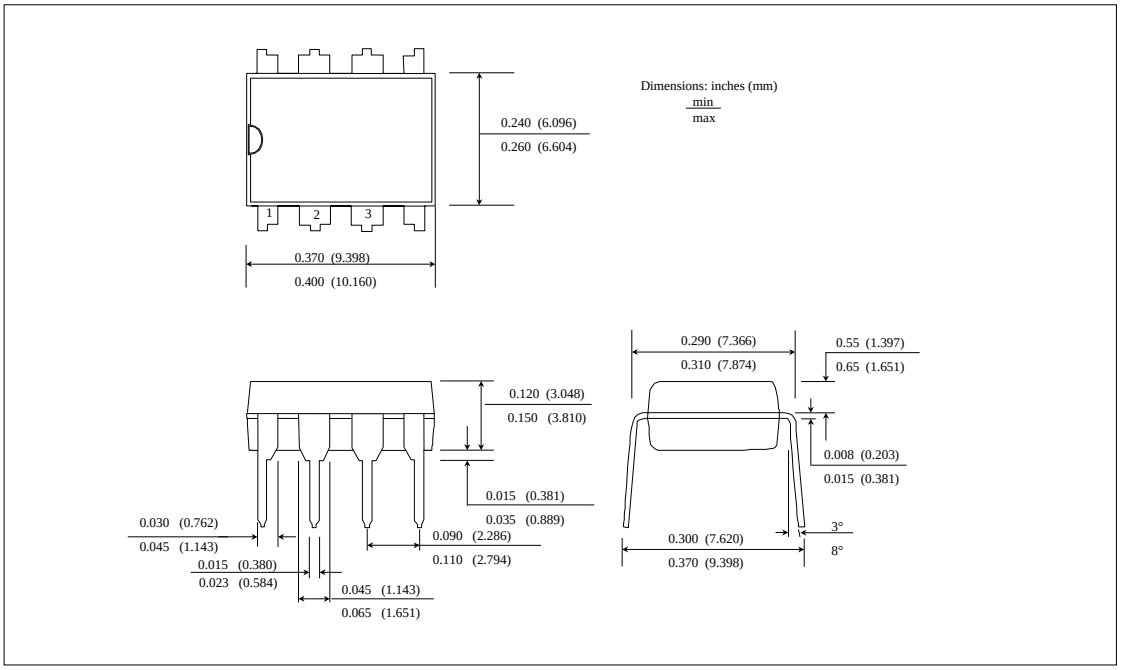


1	V_{DD1}	Input Power Supply
2	1_{IN}	Channel 1 Logic Input Signal
3	2_{OUT}	Channel 2 Logic Output Signal
4	GND_1	Input Power Supply Ground
5	GND_2	Output Power Supply Ground
6	2_{IN}	Channel 2 Logic Input Signal
7	1_{OUT}	Channel 1 Logic Output Signal
8	V_{DD2}	Output Power Supply

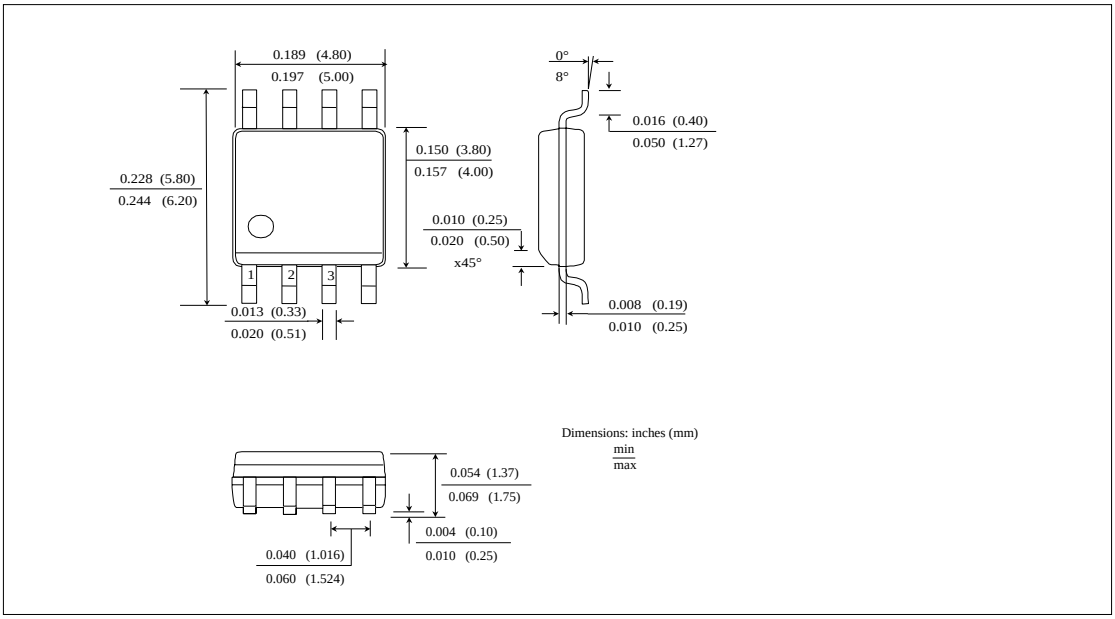


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IL711-2 and IL712-2 (8-Pin PDIP Package)



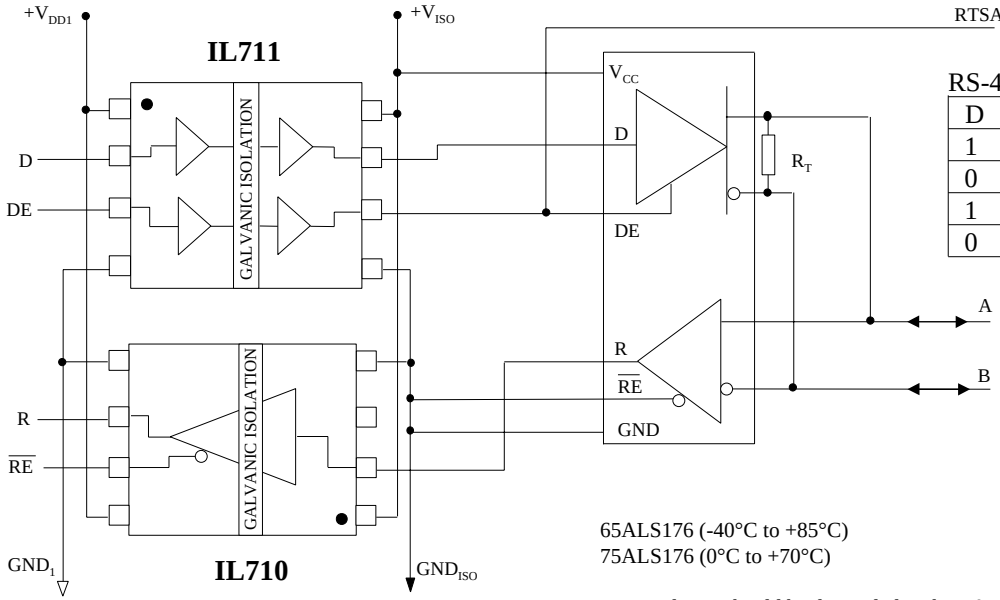
IL711-3 and IL712-3 (Small Outline SOIC-8 package)



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Applications

Isolated PROFIBUS / RS-485



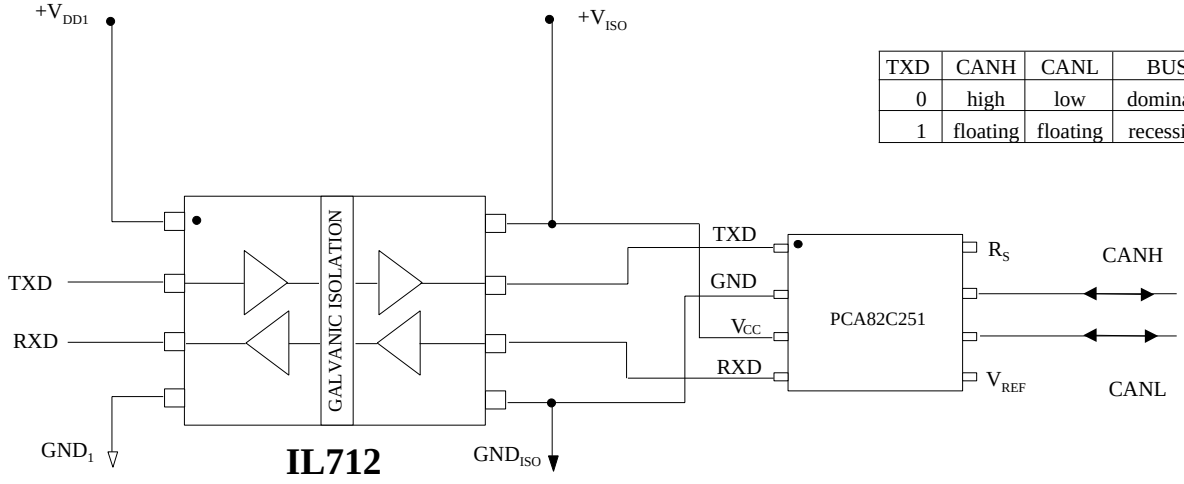
RS-485 Truth Table

D	DE	A	B	R
1	0	Z	Z	X
0	0	Z	Z	X
1	1	1	0	1
0	1	0	1	0

65ALS176 (-40°C to +85°C)
75ALS176 (0°C to +70°C)

V_{DD1} and V_{ISO} should be decoupled with a 10nF capacitor at the IL710 supply pins and a 47 nF capacitor at the IL711.

Isolated DeviceNet / CAN Transceiver



TXD	CANH	CANL	BUS	RXD
0	high	low	dominant	0
1	floating	floating	recessive	1

V_{DD1} and V_{ISO} should be decoupled with 47nF capacitors at the IL712 supply pins.

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