

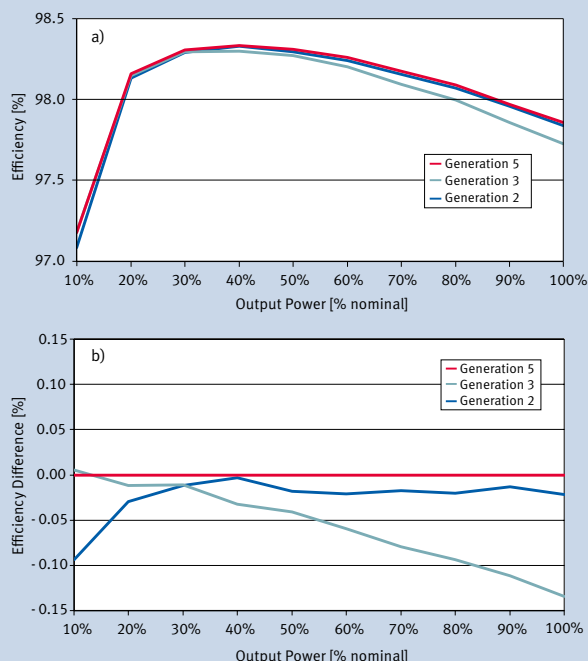


650V SiC thinQ!™ Generation 5 diodes

Your way is our way: improve efficiency and solution costs

ThinQ!™ Generation 5 represents Infineon's leading edge technology for SiC Schottky Barrier diodes. The Infineon proprietary diffusion soldering process, already introduced with G3, is now combined with a new, more compact design and thin wafer technology. The result is a new family of products showing improved efficiency over all load conditions, coming from both the improved thermal characteristics and a lower figure of merit ($Q_c \times V_p$).

The new thinQ!™ Generation 5 has been designed to complement our 650V CoolMOS™ families: this ensures meeting the most stringent application requirements in this voltage range.



Experimental results

Efficiency comparison among the three IFX generations of 8A SiC diodes

a) Absolute values

b) Referred to thinQ!™ Gen 5

(CCM PFC, High line, $P_{out\ max}=1800\ W$,
 $f_{sw}=65\ kHz$, $T_{HS}=60^\circ C$,
 MOSFET: IPW60R075CP)

Features

- V_{br} at 650V
- Improved Figure of Merit ($Q_c \times V_p$)
- No reverse recovery charge
- Soft switching reverse recovery waveform
- Temperature independent switching behavior
- High operating temperature ($T_{j\ max}\ 175^\circ C$)
- Improved surge capability
- Pb-free lead plating
- 10 years manufacturing of SiC diodes

Benefits

- Higher safety margin against Overvoltage; best match with CoolMOS™ 650V products
- Improved efficiency over all load conditions
- Increased efficiency compared to Silicon Diode alternatives
- Reduced EMI compared to snappier Silicon diode reverse recovery waveform
- Highly stable switching performance
- Reduced cooling requirements
- Reduced risks of thermal runaway
- RoHS compliant
- High quality know-how and capacity in SiC diode manufacture

Applications

- Telecom/Server SMPS
- Solar/UPS
- PC Silverbox
- LED/LCD TV
- Motor Drives
- HID lighting

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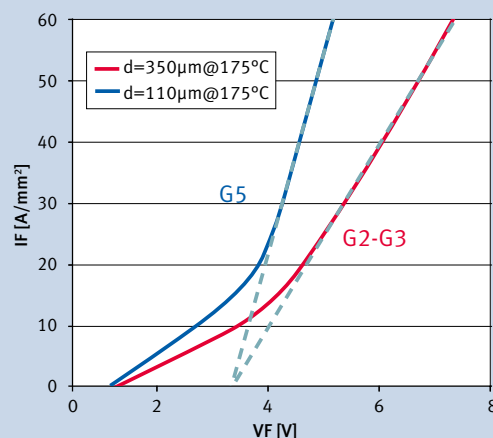
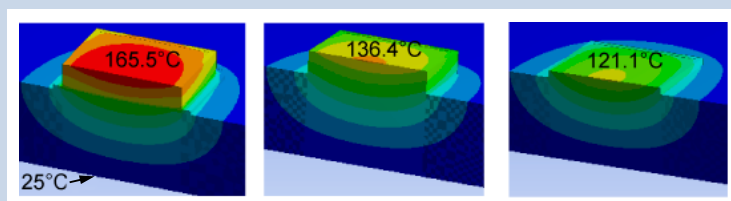
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Infineon: leading technology

An important achievement with Gen 5 is the industrial implementation of a thinning process which allows reducing the wafer thickness to almost 1/3 while maintaining the proven quality and yield levels. The thinning reduces the resistive contribution of the substrate (see picture on the right) and one of its most striking benefit is a consistent improvement of the surge current robustness, now at comparable level or even higher (for $IF < 10A$) than for G2 in spite of a smaller chip size.

In combination with our proprietary diffusion soldering, the reduced thickness further contributes to decrease the overall thermal resistance in the package. The pictures below show the temperature increase at the junction under given forward current conditions for the same device area:

Left: 350µm chip with 60µm soft solder; middle: 350µm chip with diff. solder; right: 110µm chip with diff. solder



Planned product portfolio



650V	TO-220 R2L	TO-247 New!	D ² PAK R2L New!	ThinPAK 8x8 New!
2A	IDH02G65C5		IDK02G65C5	IDL02G65C5
3A	IDH03G65C5		IDK03G65C5	
4A	IDH04G65C5		IDK04G65C5	IDL04G65C5
5A	IDH05G65C5		IDK05G65C5	
6A	IDH06G65C5		IDK06G65C5	IDL06G65C5
8A	IDH08G65C5		IDK08G65C5	IDL08G65C5
9A	IDH09G65C5		IDK09G65C5	
10A	IDH10G65C5	IDW10G65C5	IDK10G65C5	IDL10G65C5
12A	IDH12G65C5	IDW12G65C5	IDK12G65C5	IDL12G65C5
16A	IDH16G65C5	IDW16G65C5		
20A	IDH20G65C5	IDW20G65C5		
30A		IDW30G65C5		
40A		IDW40G65C5		

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Published by
Infineon Technologies Austria AG
9500 Villach, Austria

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Order Number: B152-H9677-G1-X-7600-DB2012-0016
Date: 09 / 2012

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