Integrated Device Technology, Inc.

1M x 32 CMOS STATIC RAM MODULE

IDT7MP4120

FEATURES

- High-density 4MB Static RAM module
- Low profile 72-pin ZIP (Zig-zag In-line vertical Package) or 72-pin SIMM (Single In-line Memory Module)
- Fast access time: 20ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL-compatible

PIN CONFIGURATION(1)

NC	2	1	NC	PD_0 - GND
PD_3	4	3	PD_2	PD_1 - NC
PD_0	6	5	GND	PD_2 - GND
I/O_0	8	7	PD_1	PD_3 - NC
I/O_1	10	9	I/O_8	
I/O_2	12	11	I/O_9	
I/O_3	14	13	I/O_{10}	
V_{CC}	16	15	I/O_{11}	
A_7	18	17	A_0	
A_8	20	19	A_1	
A_9	22	21	A_2	
I/O_4	24	23	I/O_{12}	
I/O_5	26	25	I/O_{13}	
I/O_6	28	27	I/O_{14}	
I/O_7	30	29	I/O_{15}	
$\overline{WE}$	32	31	GND	
A_{14}	34	33	A_{15}	
$\overline{CS_1}$	36	35	$\overline{CS_2}$	
$\overline{CS_3}$	38	37	$\overline{CS_4}$	
A_{16}	40	39	A_{17}	
GND	42	41	$\overline{OE}$	
I/O_{16}	44	43	I/O_{24}	
I/O_{17}	46	45	I/O_{25}	
I/O_{18}	48	47	I/O_{26}	
I/O_{19}	50	49	I/O_{27}	
A_{10}	52	51	A_3	
A_{11}	54	53	A_4	
A_{12}	56	55	A_5	
A_{13}	58	57	V_{CC}	
I/O_{20}	60	59	A_6	
I/O_{21}	62	61	I/O_{28}	
I/O_{22}	64	63	I/O_{29}	
I/O_{23}	66	65	I/O_{30}	
GND	68	67	I/O_{31}	
A_{19}	70	69	A_{18}	
NC	72	71	NC	

3019 drw 01

ZIP, SIMM
TOP VIEW

NOTE:

1. Pins 3, 4, 6 and 7 (PD_0, PD_1, PD_2 and PD_3 respectively) are read by the user to determine the density of the module. If PD_0 reads GND, PD_1 reads NC, PD_2 reads GND and PD_3 reads NC, then the module has a 1M depth.

DESCRIPTION

The IDT7MP4120 is a 1M x 32 Static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 1M x 4 Static RAMs in plastic packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. The IDT7MP4120 is available with access time as fast as 20ns with minimal power consumption.

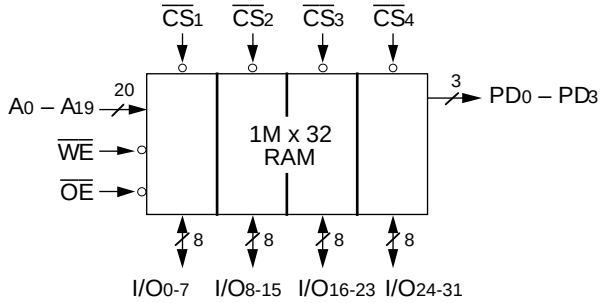
The IDT7MP4120 is packaged in a 72-pin FR-4 ZIP (Zig-zag In-line vertical Package)or a 72-pin SIMM (Single In-line Memory Module). The ZIP configuration allows 72 pins to be placed on a package 4.05" long and 0.365" wide. At only 0.60" high, this low-profile package is ideal for systems with minimum board spacing while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4120 are TTL-compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Four identification pins (PD_0, PD_1, PD_2 and PD_3) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD_0, PD_1, PD_2 and PD_3 to determine a 1M depth.

The contact pins are plated with 100 micro-inches of nickel covered by 30 micro-inches minimum of selective gold.

FUNCTIONAL BLOCK DIAGRAM



3019 drw 02

PIN NAMES

I/O_0–I/O_{31}	Data Inputs/Outputs
A_0–A_{19}	Addresses
$\overline{CS_1}$–$\overline{CS_4}$	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
PD_0–PD_3	Depth Identification
V_{CC}	Power
GND	Ground
NC	No Connect

3019 tbl 01

The IDT logo is a registered trademark of Integrated Device Technology Inc.

©1996 Integrated Device Technology, Inc.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
$C_{I/O}$	Data I/O Capacitance	$V_{(IN)}$ = 0V	15	pF
C_{IN1}	Input Capacitance (Address)	$V_{(IN)}$ = 0V	60	pF
C_{IN2}	Input Capacitance ($\overline{WE}$, $\overline{OE}$)	$V_{(IN)}$ = 0V	75	pF
C_{IN3}	Input Capacitance ($\overline{CS}$)	$V_{(IN)}$ = 0V	20	pF

NOTE: 3019 tbl 02
1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 3019 tbl 03
1. V_{IL} (min) = –1.5V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

3019 tbl 04

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Read	L	H	H	High-Z	Active

3019 tbl 05

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 3019 tbl 06
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output LOW	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output HIGH	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

3019 tbl 07

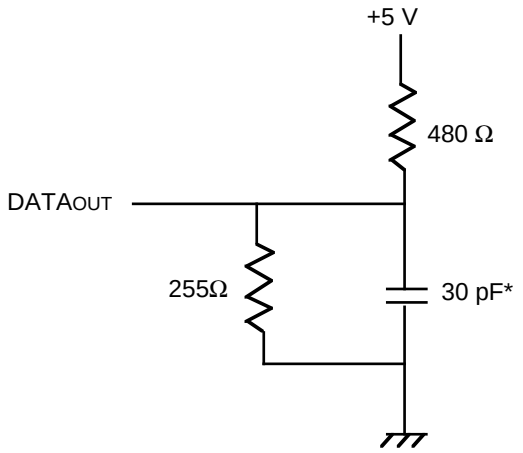
Symbol	Parameter	Test Conditions	7MP4120 Max.	Unit
I_{CC}	Dynamic Operating Current	f = f_{MAX}; $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	1280	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}	480	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V; f = 0 V_{IN} > V_{CC} – 0.2V or < 0.2V	120	mA

3019 tbl 08

AC TEST CONDITIONS

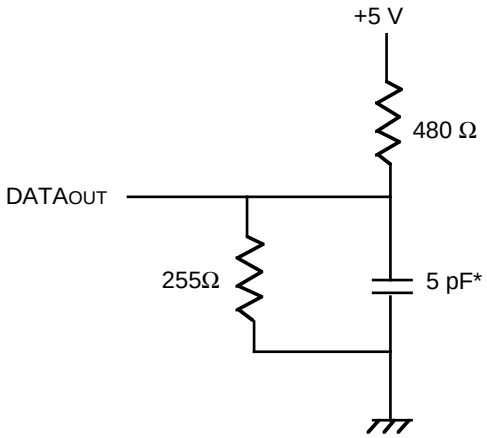
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2769 tbl 09



3019 drw 03

Figure 1. Output Load



3019 drw 04

Figure 2. Output Load
(for t_{OLZ},t_{OHZ}, t_{CHZ}, t_{CLZ}, t_{WHZ}, t_{OW})

*Includes scope and jig.

AC ELECTRICAL CHARACTERISTICS

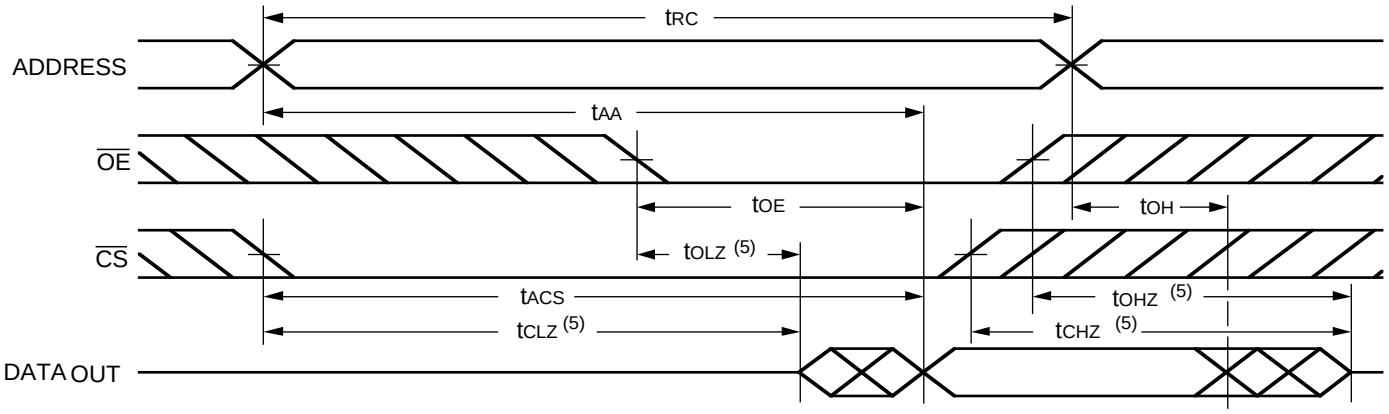
(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP4120SxxZ/M				Unit
		–20		–25		
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	20	—	25	—	ns
t_{AA}	Address Access Time	—	20	—	25	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	ns
t_{CLZ}(1)	Chip Select to Output in Low-Z	3	—	3	—	ns
t_{OE}	Output Enable to Output Valid	—	12	—	15	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	0	—	0	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High-Z	—	10	—	12	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	—	10	—	12	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	20	—	25	ns
Write Cycle						
t_{WC}	Write Cycle Time	20	—	25	—	ns
t_{CW}	Chip Select to End-of-Write	17	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	17	—	20	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	ns
t_{WR}	Write Recovery Time	3	—	3	—	ns
t_{WHZ}(1)	Write Enable to Output in High-Z	—	10	—	15	ns
t_{DW}	Data to Write Time Overlap	12	—	15	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	ns
t_{OW}(1)	Output Active from End-of-Write	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

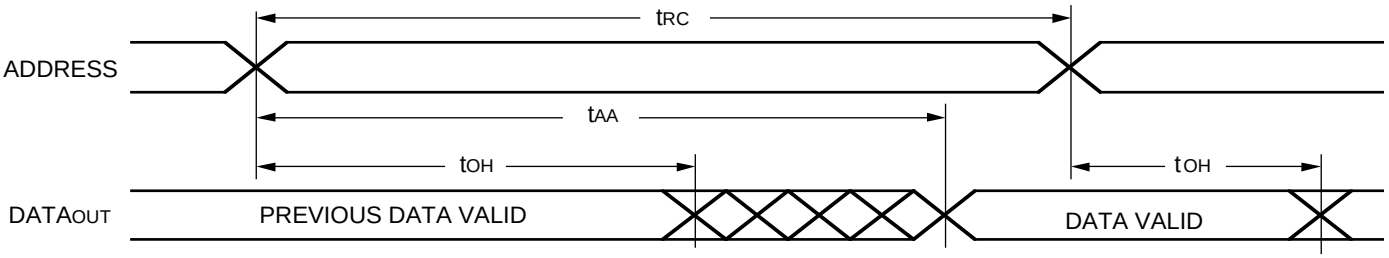
3019 tbl 10

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



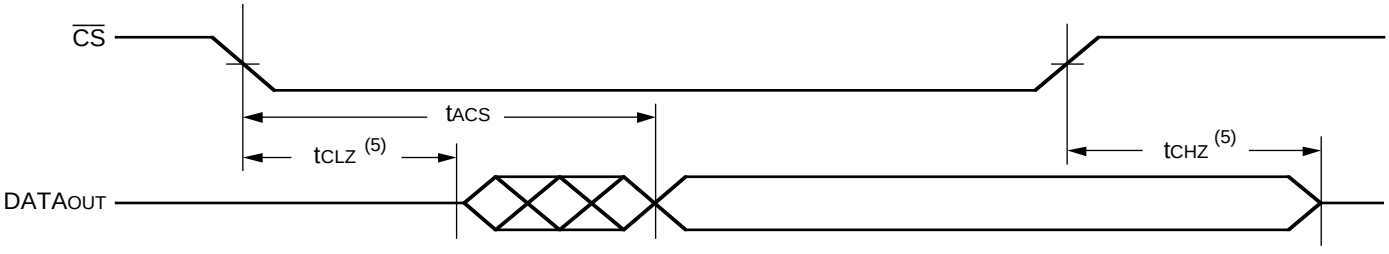
3019 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



3019 drw 06

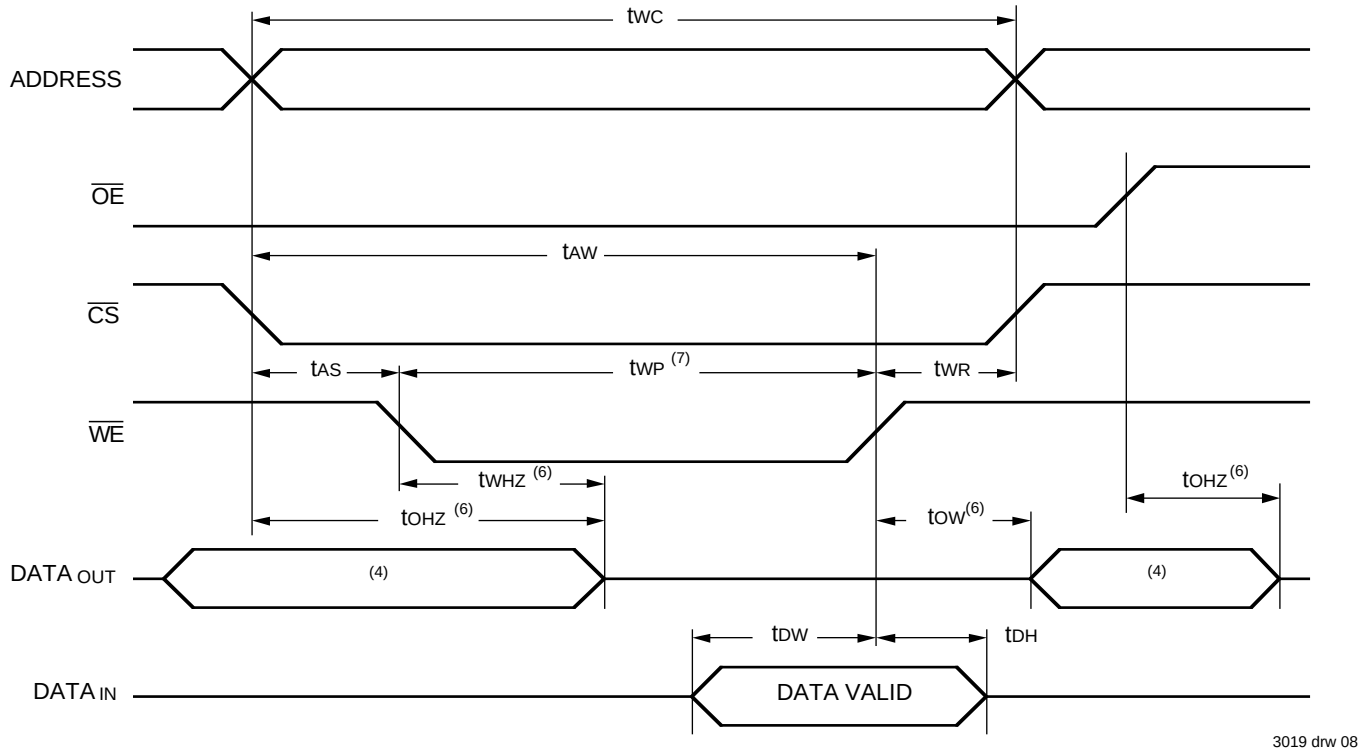
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



3019 drw 07

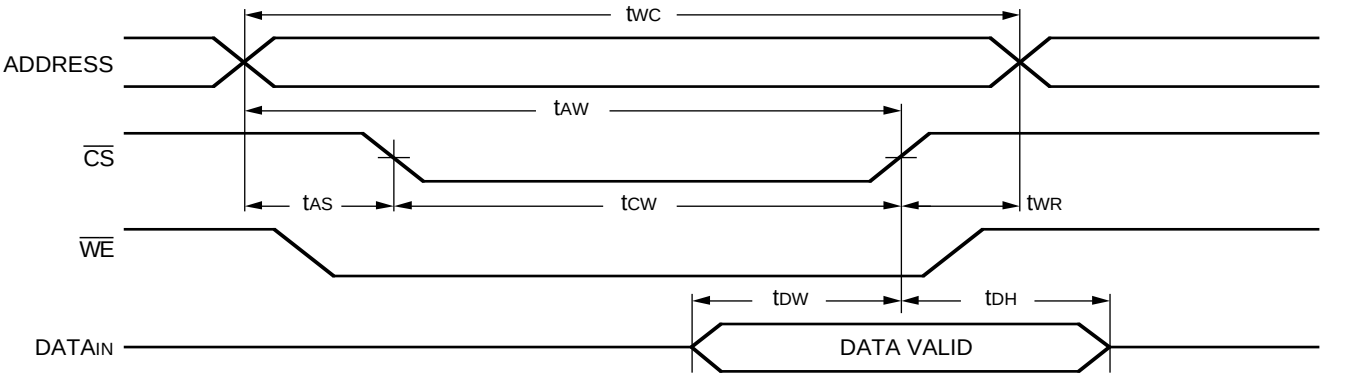
NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (1, 2, 3, 7)



3019 drw 08

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) (1, 2, 3, 5)

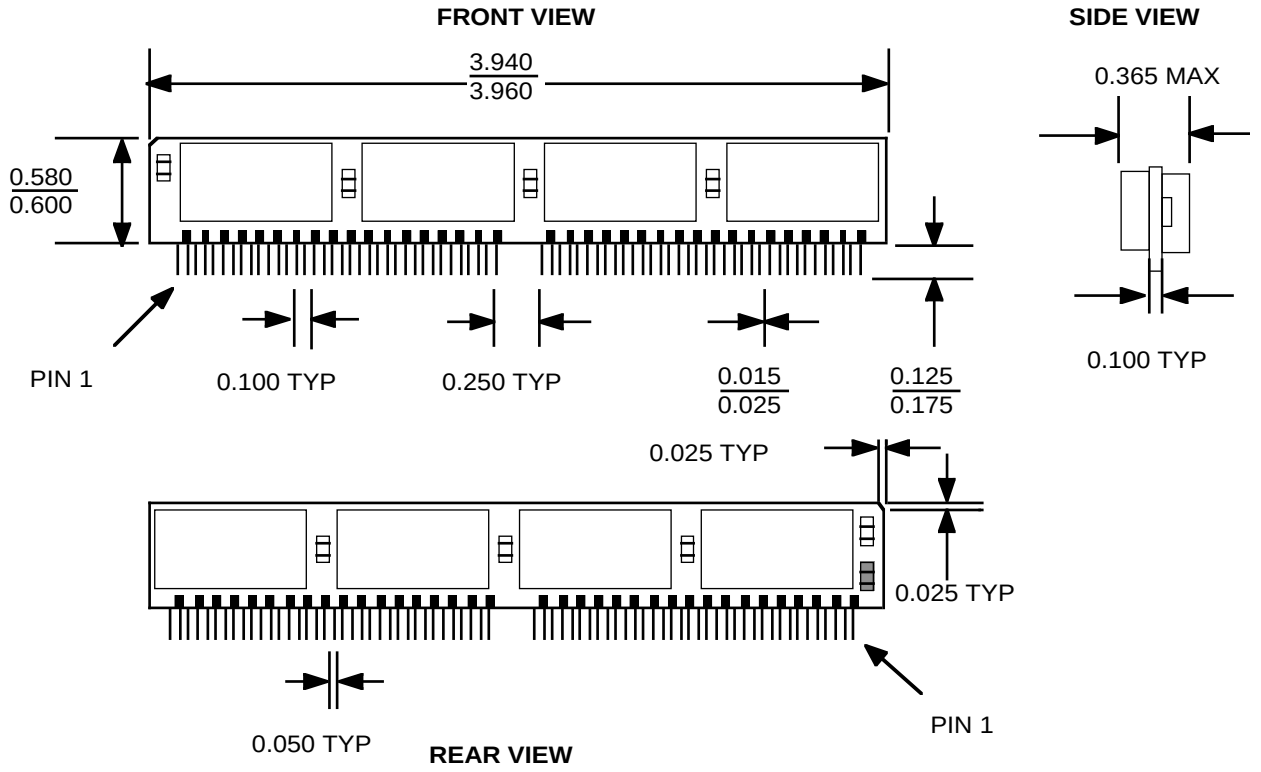


3019 drw 09

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

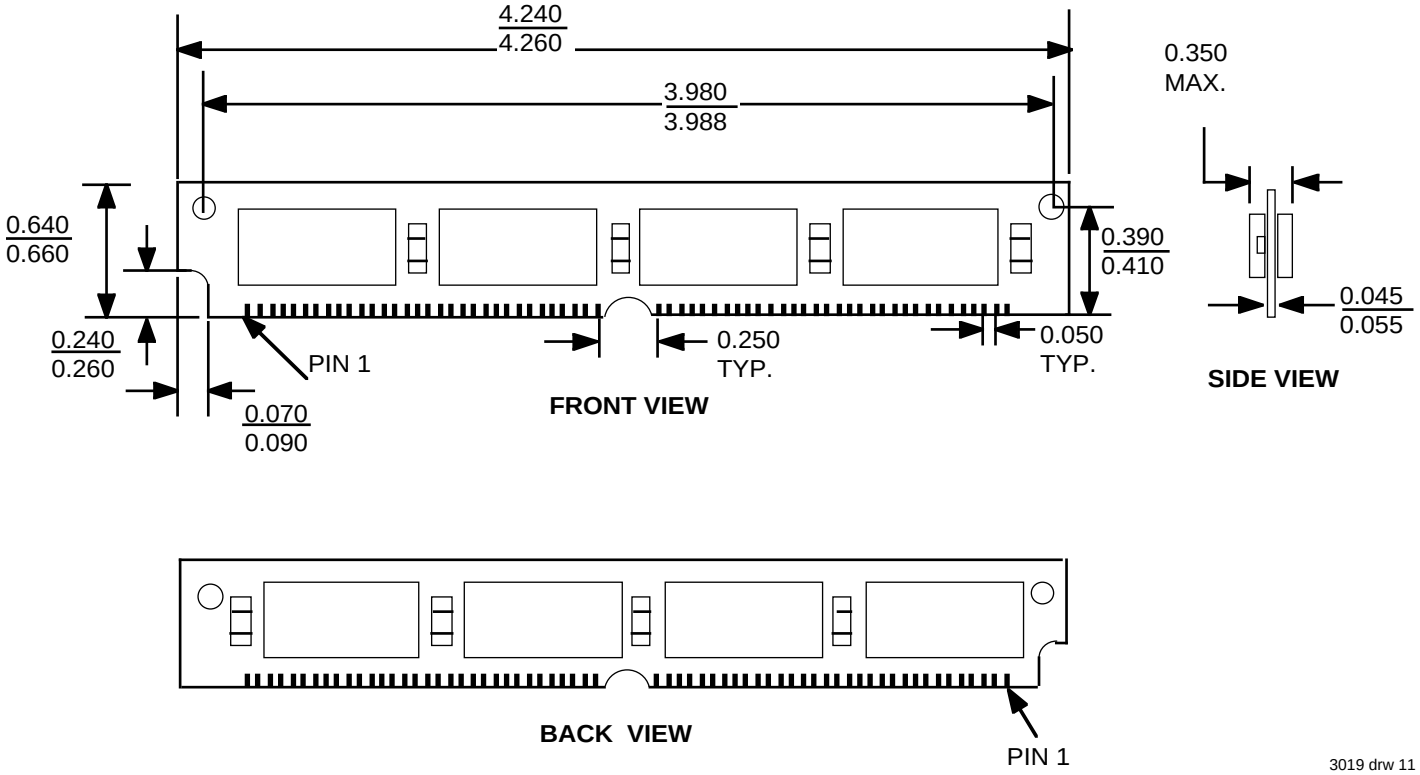
PACKAGE DIMENSIONS

ZIP VERSION



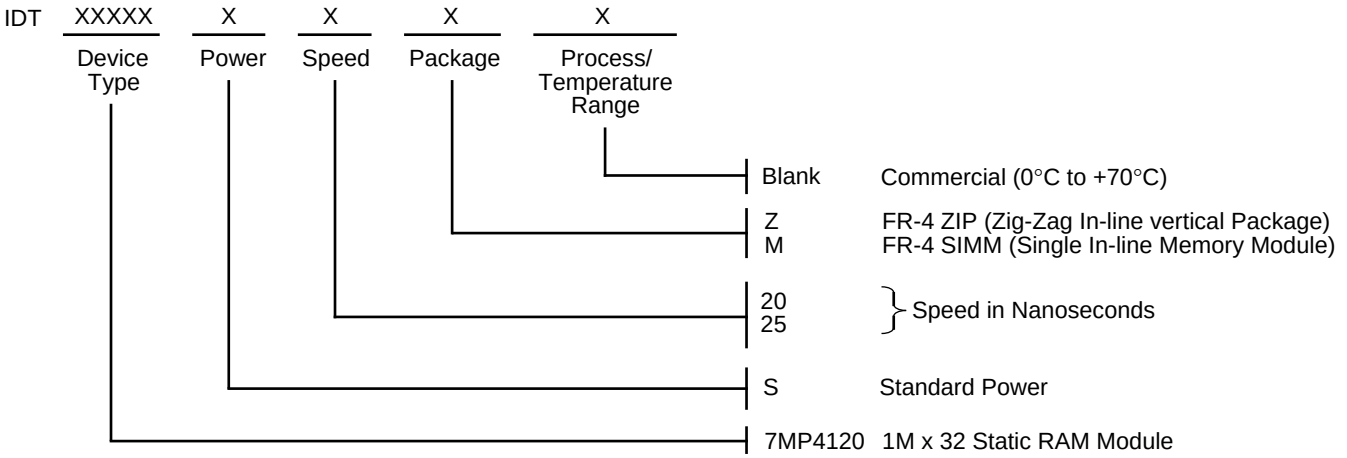
3019 drw 10

SIMM VERSION



3019 drw 11

ORDERING INFORMATION



3019 drw 12