PRODUCT SPECIFICATIONS

SHARP®

Integrated Circuits Group

ID243D01

2MB Flash Memory Card

(Model No.: ID243D01)

Spec No.: EL093030

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- Please direct all queries regarding the products covered herein to a sales representative of the company.

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1. General Descriptions

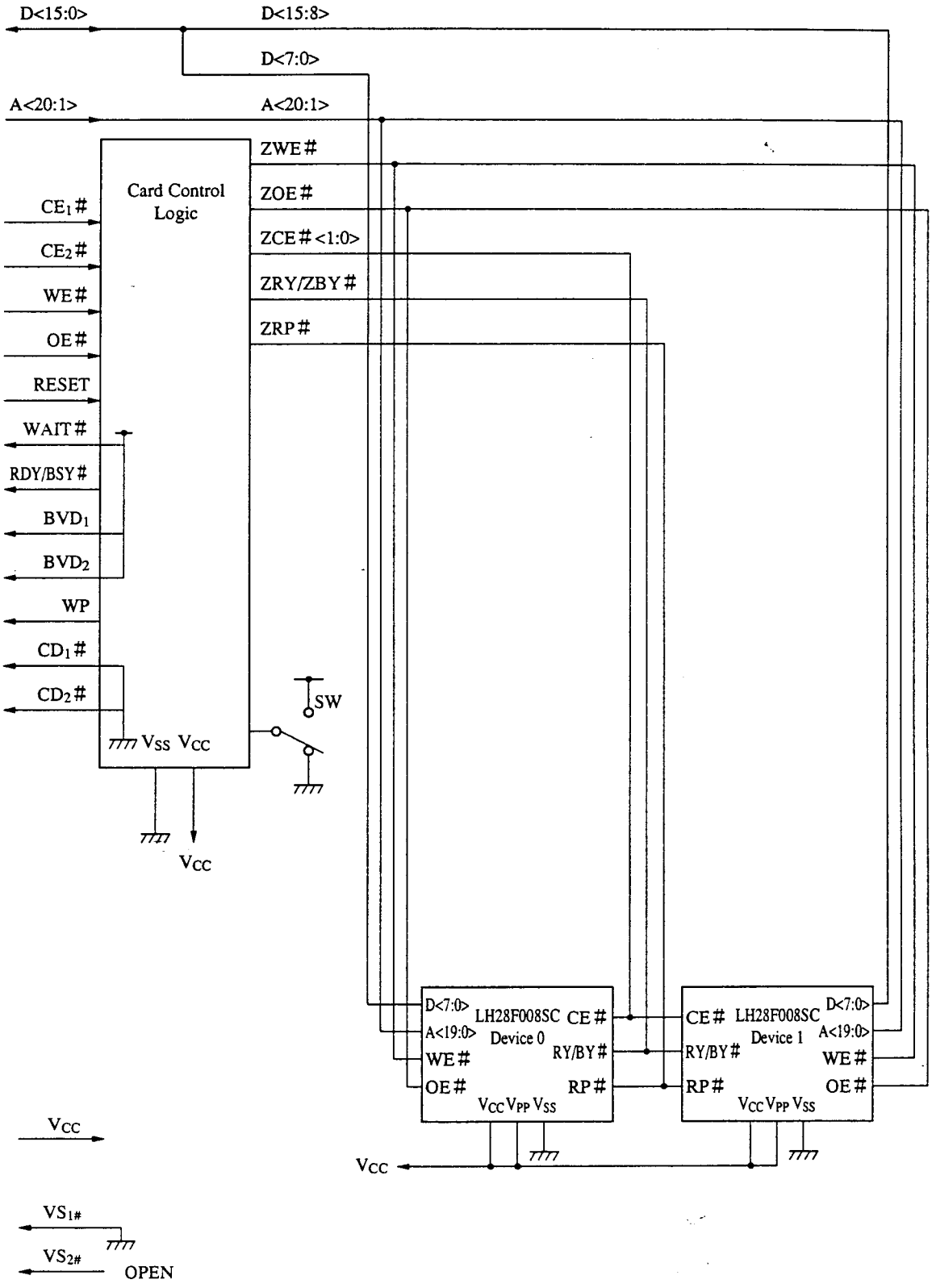
The SHARP ID243D01, which panel design is SHARP standard, is a 2MB Flash Memory PC Card conforms to PCMCIA/JEIDA Type 1 mechanical specifications and is offered to customers giving aim to confirm an external shape or electrical performances of the card. Before mass production, we will create a new product name dedicated for a customer and also present a specification which implies customer's request including panel design.

2. Features

2.1	Type	2MB Flash Memory Card (Conforms to PCMCIA/JEIDA Type 1 mechanical specifications)
2.2	Memory Capacity Main Memory	1M words × 16 bits (2M words × 8 bits)
2.3	Supply Voltage	5.0V ± 5% or 3.3V ± 0.3V
2.4	Erase Unit	64K word Blocks
2.5	Program/Erase Cycles	100,000 cycles per Block
2.6	Interface	Parallel I/O Interface
2.7	Function Table	See Function Table in page. 10
2.8	External Dimensions	54.0 × 85.6 × 3.3 mm
2.9	Pin Connections	See Pin Connections in page. 5
2.10	Type of Connector	Conforms to PCMCIA Rel. 2.0 Card Use Connector (Card connector: JC20-J68S-NB3 JAE or FCN-568J068-G/0 Fujitsu)
2.11	Average Weight	30g
2.12	Operating Temp. Range	0 to 60°C
2.13	Storage Temp. Range	–20 to 65°C
2.14	External Appearance	External appearance shall be free of any dirt, cratches and abnormalities that could adversely affect sales.
2.15	Manufacturer's Code	The manufacturer's code shall be printed on the memory card directly or on the seal which is then attached to the memory card.
2.16	Brand Name	The user's brand name will used.

2.17 Not designed for rated radiation hardened.

3. Block Diagram



4. Pin Connections

PIN	SIGNAL	I/O	FUNCTION	ACTIVE
1	GND		Ground	
2	D_3	I/O	Data Bit 3	
3	D_4	I/O	Data Bit 4	
4	D_5	I/O	Data Bit 5	
5	D_6	I/O	Data Bit 6	
6	D_7	I/O	Data Bit 7	
7	CE_1#	I	Card Enable 1	LOW
8	A_{10}	I	Address Bit 10	
9	OE#	I	Output Enable	LOW
10	A_{11}	I	Address Bit 11	
11	A_9	I	Address Bit 9	
12	A_8	I	Address Bit 8	
13	A_{13}	I	Address Bit 13	
14	A_{14}	I	Address Bit 14	
15	WE#	I	Write Enable	LOW
16	RDY/BSY#	O	Ready/Busy	LOW
17	V_{CC}		Supply Voltage	
18	V_{PP1}		Supply Voltage	N.C.
19	A_{16}	I	Address Bit 16	
20	A_{15}	I	Address Bit 15	
21	A_{12}	I	Address Bit 12	
22	A_7	I	Address Bit 7	
23	A_6	I	Address Bit 6	
24	A_5	I	Address Bit 5	
25	A_4	I	Address Bit 4	
26	A_3	I	Address Bit 3	
27	A_2	I	Address Bit 2	
28	A_1	I	Address Bit 1	
29	A_0	I	Address Bit 0	N.C.
30	D_0	I/O	Data Bit 0	
31	D_1	I/O	Data Bit 1	
32	D_2	I/O	Data Bit 2	
33	WP	O	Write Protect	HIGH
34	GND		Ground	

PIN	SIGNAL	I/O	FUNCTION	ACTIVE
35	GND		Ground	
36	CD_1#	O	Card Detect 1	LOW
37	D_{11}	I/O	Data Bit 11	
38	D_{12}	I/O	Data Bit 12	
39	D_{13}	I/O	Data Bit 13	
40	D_{14}	I/O	Data Bit 14	
41	D_{15}	I/O	Data Bit 15	
42	CE_2#	I	Card Enable 2	LOW
43	VS_1#	O	Voltage Sense 1	LOW
44	RFU		Reserved	
45	RFU		Reserved	
46	A_{17}	I	Address Bit 17	
47	A_{18}	I	Address Bit 18	
48	A_{19}	I	Address Bit 19	
49	A_{20}	I	Address Bit 20	
50	A_{21}	I	Address Bit 21	N.C.
51	V_{CC}		Supply Voltage	
52	V_{PP2}		Supply Voltage	N.C.
53	A_{22}	I	Address Bit 22	N.C.
54	A_{23}	I	Address Bit 23	N.C.
55	A_{24}	I	Address Bit 24	N.C.
56	A_{25}	I	Address Bit 25	N.C.
57	VS_2#	O	Voltage Sense 2	N.C.
58	RESET	I	Reset	HIGH
59	WAIT#	O	Extend Bus Cycle	LOW
60	RFU		Reserved	
61	REG#	I	Attribute Memory Select	N.C.
62	BVD_2	O	Battery Voltage Detect 2	
63	BVD_1	O	Battery Voltage Detect 1	
64	D_8	I/O	Data Bit 8	
65	D_9	I/O	Data Bit 9	
66	D_{10}	I/O	Data Bit 10	
67	CD_2#	O	Card Detect 2	LOW
68	GND		Ground	

5. Signal Description

SYMBOL	TYPE	NAME AND FUNCTION
A_0–A_{25}	INPUT	**ADDRESS INPUTS:** Address A_0 through A_{25} are address bus lines which enable direct addressing of up to 64 MB of memory on the card. Signal A_0 is not decoded since the card is × 16 only. The memory will wrap at the card density boundary. The system should NOT try to access memory beyond the card's density, since the upper addresses are not decoded.
D_0–D_{15}	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** D_0 through D_{15} constitute the bi-directional data bus. D_{15} is the most significant bit.
CE_1#, CE_2#	INPUT	**CARD ENABLE 1 & 2:** CE_1# enables EVEN byte accesses on $D_{0\text{-}7}$, CE_2# enables ODD byte accesses on $D_{8\text{-}15}$. Cannot access Odd Bytes on $D_{0\text{-}7}$.
OE#	INPUT	**OUTPUT ENABLE:** Active low signal gating read data from the memory card.
WE#	INPUT	**WRITE ENABLE:** Active low signal gating write data to the memory card.
RDY/BSY#	OUTPUT	**READY/BUSY OUTPUT:** Indicates status of internally timed erase or write activities. A high output indicates the memory card is ready to accept accesses.
CD_1#, CD_2#	OUTPUT	**CARD DETECT 1 & 2:** These signals provide for card insertion detection. The signals are connected to ground internally on the memory card, and will be forced low whenever a card is placed in the socket. The host socket interface circuitry shall supply 10K or larger pull-up resistors on these signal pins.
WP	OUTPUT	**WRITE PROTECT:** Write Protect reflects the status of the Write Protect switch on the memory card. WP set to high = write protected.
V_{PP1}, V_{PP2}	N.C.	**WRITE/ERASE POWER SUPPLY 1 & 2:** These power signals are not connected for the single supply.
V_{CC}		**CARD POWER SUPPLY:** 3.3V or 5.0V for all internal circuitry.
GND		GROUND for all internal circuitry.
REG#	N.C.	**REGISTER SELECT:** The memory card has no separate attribute memory. REG# is unconnected on the card.
RESET	INPUT	**RESET:** Active high signal for placing card in Power-On Default State. RESET can be used as a POWER-DOWN signal for the memory array.
WAIT#	OUTPUT	**WAIT:** (Extended Bus Cycle) This signal is pulled high for compatibility.
BVD_1, BVD_2	OUTPUT	**BATTERY VOLTAGE DETECT 1 & 2:** These signals are pulled high to maintain SRAM card compatibility.
VS_1#, VS_2#	OUTPUT	**VOLTAGE SENSE 1 & 2:** Notifies the host socket of the card's V_{CC} requirements. VS_1# is pulled down to ground and VS_2# is left open to indicate a 3.3V capable card has been inserted.
RFU		RESERVED FOR FUTURE USE
N.C.		NO INTERNAL CONNECTION TO CARD pin may be driven or left floating.

6. LH28F008SC Control Logic

6. 1 Bus Operations

The host executes read, write and erase operations by issuing the appropriate command to the flash device's Command User Interface (CUI). The CUI serves as the interface between the host processor and internal operation of the flash device. These commands can be issued to the CUI using standard microprocessor bus cycles.

6. 1. 1 Read Array

The host enables reads from the card by writing the appropriate read command to the CUI. The LH28F008SC automatically resets to read array mode upon initial device power-up, or after reset. CE1#, CE2#, and OE# must be logically active to obtain 16 data bits at the outputs. The Card Enables (CE1# and CE2#) are used to select the addressed devices. Output Enable (OE#) is the data input/output (D0–D15) direction control, and when active, drives data from the selected memory onto the data bus. WE# must be driven to V_{IH} during a read access.

6. 1. 2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Outputs (D0–D15) are placed in a high-impedance state.

6. 1. 3 Standby

CE1# and CE2# at a logic-high level (V_{IH}) places the card in standby mode. Standby operation disables much of the card's circuitry and substantially reduces device power consumption. The outputs (D0–D15) are placed in a high-impedance state independent of the status of OE#. If the host deselects the card during a write or erase, the card continues to function and consume normal active power until the operation completes.

6. 1. 4 Deep Power-Down

RESET at V_{IH} initiates the deep power-down mode.

During reads, an active RESET deselects the memory, places output drivers in a high-impedance state, and turns off all internal circuits. RESET must be held high for a minimum of 100 ns. After returning from deep power-down, the host must wait before initial memory access outputs are valid, as determined by t_{PHQV}. After this wake-up interval, the host can resume normal operations to the card. Card reset forces the CUI to reset to read array mode and sets the status register to 80H.

During block erase, byte write, or lock-bit configuration modes, an active RESET will abort the operation. RDY/BSY# remains low until the reset operation completes. Memory contents being altered are no longer valid; the data may be partially erased or written. The host must wait after RESET goes to logic-Low (V_{IL}) before it can write another command, as determined by t_{PHWL}.

It is important to assert RESET to the card during a system reset. If a CPU reset occurs without a card reset, the host will not be able to read from the card if that card is in a different mode when the system reset occurs.

For example, if an end-user initiates a host reset when the card is in read status register mode, the host will attempt to read code from the card, but will actually read status register data. Sharp's ID243 Series Flash Memory Card

allows proper card reset following a system reset through the use of the RESET input. System RESET circuitry can reset the host CPU in addition to the card.

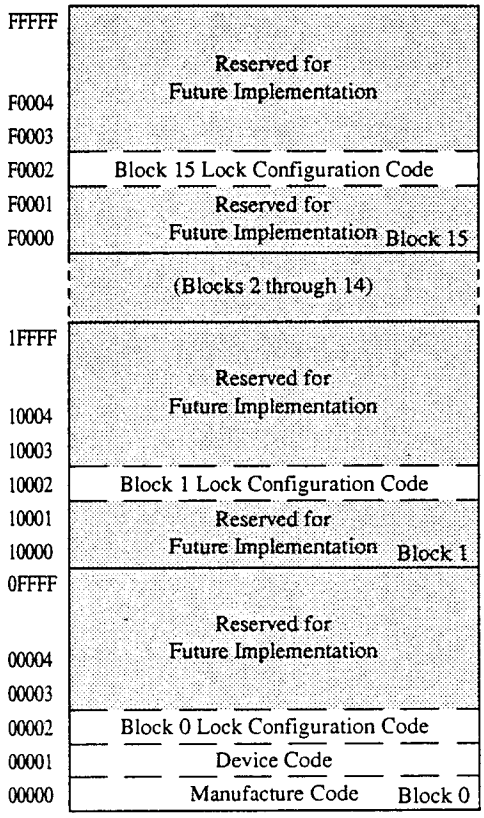


Figure 1. Device Identifier Code Memory Map

6. 1. 5 Read Identifier Codes Operation

The read identifier codes operation outputs the manufacturer code (Block 0), device code (Block 0), and block lock configuration codes (for each block), see Figure 1. Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The block lock codes identify locked and unlocked blocks.

6. 1. 6 CUI Writes

Writes to the CUI enable reading of device data and intelligent identifiers. They also control inspection and clearing of the Status Register. The contents of the interface register serves as input to the internal state machine on each component.

The CUI itself does not occupy an addressable memory location. The interface register is a latch used to store the command, address and data information needed to execute the command. Erase Setup and Erase Confirm commands require both appropriate command data and an address within the block to be erased. The Write Setup command requires both appropriate command data and the address of the location to be written, while the Write command consists of the data to be written and the address of the location to be written.

The CUI is written by bringing WE# to a logic-low level (V_{IL}) while CE# is low. Addresses and data are latched on the rising edge of WE#. Standard microprocessor write timings are used.

When a write or erase command has been issued to the CUI, the internal Write State Machine (WSM) becomes busy and will not be ready until it has completed the operation.

6. 2 SmartVoltage Technology

SmartVoltage technology provides a choice of V_{CC} at 3.3V or 5.0V. V_{CC} at 3.3V consumes low power. However, V_{CC} at 5.0V provides the highest read performance. Internal device detection circuitry automatically configures the device.

7. Card Control Logic

7. 1 Word Addressing

Sharp's ID243 Series Flash Memory Card uses two × 8 devices in parallel to form the Memory card × 16 data bus. If the host writes a command to the card, it must make sure that it writes the command to both devices in the card. For example, a component write command is 40H, so a card write command must be 4040H. This same procedure must be followed when reading from the status register. A component status register is only 8 bits and may return 80H when read. However, the card status register is 16 bits and may return 8080H.

7. 2 Decode Logic

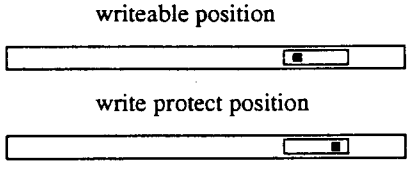
The decode logic enables the appropriate component device pair during a read or write access. Unused upper addresses for the ID243 Series Flash Memory Card will not be decoded. The address decoding will wrap around at the card's density.

7. 3 Write Protect Switch

The ID243 Series Flash Memory Card has a write protect switch on the back of the card. When the switch is in the write protect position, the card blocks all writes to the card (see Figure 2).

NOTE

When the write protect switch is in the write protect position, all writes are disabled to the flash array including all commands to the CUI.



NOTE:

The write protect switch is represented by the solid black rectangle.

Figure 2. Write Protect Switch

7. 4 Data Control

As shown in Table 1. data paths and directions are selected by the Data Control logic using WE#, OE#, CE1#, and CE2#, as logic inputs. The Data Control logic selects any of the PCMCIA word-wide, EVEN-byte and ODD-byte modes for either reads or writes to common memory.

NOTE:

This card has a ×16 interface. The ODD byte CANNOT be accessed on the lower data path (D_{0-7}). A_0 is not decoded.

Mode	RESET	CE_2#	CE_1#	OE#	WE#	A_1	V_{PP}	D_{8-15}	D_{0-7}	RY/BY#	Notes
Even Byte-Read	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	×	×	High-Z	Even	×	1.2.3
Odd Byte-Read	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	×	×	Odd	High-Z	×	1.2.3
Word-Read	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	×	×	Odd	Even	×	1.2.3
Even Byte-Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	×	×	×××	Even	V_{OL}	3.4
Odd Byte-Write	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	×	×	Odd	×××	V_{OL}	3.4
Word-Write	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	×	×	Odd	Even	V_{OL}	3.4
Manufacturer ID	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	×	89H	89H	V_{OH}	—
Device ID	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	×	A6H	A6H	V_{OH}	5
Standby	V_{IL}	V_{IH}	V_{IH}	×	×	×	×	High-Z	High-Z	×	—
Output Disable	V_{IL}	×	×	V_{IH}	V_{IH}	×	×	High-Z	High-Z	×	—
Power-Down	V_{IH}	×	×	×	×	×	×	High-Z	High-Z	×	—

Table 1. Function Table

NOTES:

1. Refer to DC Characteristics.
2. × can be V_{IL} or V_{IH} for control pins and address.
3. RDY/BSY# is V_{OL} when the WSM is executing internal byte write or block erase algorithms. It is V_{OH} when the WSM is not busy, in erase suspend mode, or deep power-down mode.
4. Refer to Table 2 for valid D_{IN} during a write operation.
5. The device code can be A6H or AAH. Software should check for all two cases for compatibility with future cards.

8. Command Definitions

Device operations are selected by writing specific commands into the Command User Interface. Table 2 defines the LH28F008SC commands.

NOTE:

When the write protect switch is in the write protect position, all writes are disabled to the flash array including commands to the CUI.

Table 2. Command Definitions (6)

Command	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
			Oper(1)	Addr(2)	Data(3)	Oper(1)	Addr(2)	Data(3)
Read Array/Reset	1	—	Write	×	FFFFH	—	—	—
Read Identifier Codes	≥2	4	Write	×	9090H	Read	IA	ID
Read Status Register	2	—	Write	×	7070H	Read	×	SRD
Clear Status Register	1	—	Write	×	5050H	—	—	—
Block Erase	2	—	Write	BA	2020H	Write	BA	D0D0H
Word Write	2	5	Write	WA	4040H or 1010H	Write	WA	WD
Block Erase and Word Write Suspend	1	—	Write	×	B0B0H	—	—	—
Block Erase and Word Write Resume	1	—	Write	×	D0D0H	—	—	—
Set Block Lock-Bit	2	—	Write	BA	6060H	Write	BA	0101H
Clear Block Lock-Bits	2	—	Write	×	6060H	Write	×	D0D0H

NOTES:

1. Bus operations are defined in Table 1.
2. × = Any valid address within the device.
   IA = Identifier Code Address: see Figure 1.
   BA = Address within the block being erased or locked.
   WA = Address of memory location to be written.
3. SRD = Data read from status register. See Table 4 for a description of the status register bits.
   WD = Data to be written at location WA. Data is latched on the rising edge of WE# or CE# (Whichever goes high first).
   ID = Data read from identifier codes.
4. Following the Read Identifier Codes command, read operations access manufacturer, device and block lock configuration codes. See Section 8.2 for read identifier code data.
5. Either 40H or 10H are recognized by the WSM as the byte write setup.
6. Commands other than those shown above are reserved for future device implementations and should not be used.

8. 1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the card defaults to read array mode. The host can also read by writing the Read Array command. The device remains enabled for reads until the host writes another valid command. Once the internal WSM has started a block erase, byte write or lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation. However, the host can suspend the WSM using an Erase Suspend or Byte Write Suspend command.

8. 2 Read Identifier Codes Command

The host initiates the identifier code operation by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 1 retrieve the manufacturer, device and block lock configuration codes (see Table 3 for identifier code data). To terminate the operation, write another valid command. Although Table 3 lists the device code as A6A6, this family of Sharp's ID243 Series Flash Memory Card could also have device codes AAAA. Host software should check for all two cases for compatibility with future cards.

Table 3. Identifier Codes

Code	Address	Data(2)
Manufacture Code	00000	8989
Device Code	00001	A6A6
Block Lock Configuration	× 0002(1)	
• Block is Unlocked		$D_{0,8} = 0$
• Block is Locked		$D_{0,8} = 1$
• Reserved for Future Use		$D_{1\text{-}7,9\text{-}15}$

NOTES:

1. × selects the specific block lock configuration code to be read. See Figure 1 for the device identifier code memory map.
2. The addresses listed are word addresses and store 16 bits of data.

8. 3 Read Status Register Command

The LH28F008SC components on the ID243 Series Flash Memory Card each contain a Status Register which may be read to determine when a write, block erase, or lock bit configuration is complete, and whether that operation completed successfully (see Table 4). The host may read the Status Register at any time by writing the Read Status Register command to the CUI. After writing this command, all subsequent read operations output data from the Status Register, until the host writes another valid command to the CUI. The flash components latch the contents of the Status Register on the falling edge of OE# or CE#, whichever occurs first. OE# or CE# must be toggled to V_{IH} before further reads to update the Status Register latch.

NOTE:

The ID243 Series Flash Memory Card arranges two LH28F008SC devices in parallel to from a ×16 bus. Both status registers need to be checked when determining the status of a ×16 erase/write operation.

8. 4 Clear Status Register Command

The WSM sets the Erase Status and Write Status bits to "1"s and they can only be reset by the Clear Status Register command. The WSM sets these bits to "1" when a write or erase operation has failed. The host can issue additional write and erase commands to the CUI without clearing the status register. This allows a system to write a sequence of bytes before checking the write status bit. However, if an error has occurred the system will not know which write in the sequence has failed. To clear the Status Register, the Clear Status Register command (5050H) is written to the CUI.

NOTE:

If V_{PP} has not been turned on, the WSM sets the V_{PP} status bit. However, the ID243 Series Flash Memory Card ties V_{PP} and V_{CC} on the LH28F008SC devices together so if V_{CC} is on then V_{PP} will also be on. If for some reason the WSM sets the V_{PP} Status bit, the host must clear the status register before it attempts further writes or block erases.

8.5 Block Erase Command

The host executes an erase command one block at a time using a two-cycle command. The host writes a block erase setup command first, followed by a block erase confirm command. These two commands require appropriate sequencing and an address within the block to complete (erase changes all block data to FFH). The WSM handles block preconditioning, erase, and verify internally (invisible to the system). After the host writes the two-cycle block erase sequence, the device automatically outputs status register data when read. The CPU can detect block erase completion by analyzing the output data of the RDY/BSY# signal or status register bit SR.7.

When the block erase completes, status register bit SR.5 should be checked. If a block erase error is detected, the host should clear the status register before system software attempts corrective actions. The CUI remains in read status register mode until the host issues a new command.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in the WSM setting status register bits SR.4 and SR.5 to "1". Successful block erase requires that the corresponding block lock-bits is not set. If the host attempts a block erase when the corresponding block lock-bit is set, the WSM will set SR.1 and SR.5 to "1".

8.6 Word Write Command

The host executes a word write by a two-cycle command sequence. The host writes word write setup (standard 4040H or alternate 1010H) first, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the word write and write verify algorithms internally. After the host writes the word write sequence, the device automatically output status register data when read. The CPU can detect the completion of the byte write event by analyzing the RDY/BSY# pin or status register bit SR.7.

When the WSM completes the word writes, the host should check status register bit SR.4. If the host detects a write error, it should clear the status register. The internal WSM verify only detects errors for "1"s that do not

successfully writes to "0"s. The CUI remains in read status register mode until it receives another command.

Successful word writes requires that the corresponding block lock-bit is not set. If the host attempts a write when the corresponding block lock-bit is set, the WSM will set SR.1 and SR.4 "1".

8. 7 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or write data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. After the host writes the Block Erase Suspend command, the host should then write the Read Status Register command. Polling status register bits SR.7 and SR.6 can determine when the WSM suspends the block erase operation (both will be set to "1"). RDY/BSY# will also transition to V_{OH} Specification t_{WHRH2} defines the block erase suspend latency. It is also possible that the block erase completes before the device has an opportunity to suspend. The host should also check for this condition.

After the block erase has been suspended, the host can issue a read array command or a word write command to any block except the one that has been suspended. Using the Word Write Suspend command (see Section 8.8), a word write operation can also be suspended. During a word write operation with block erase suspended, status register bit SR.7 will return to "0" and the RDY/BSY# output will transition to V_{OL}. However, SR.6 will remain "1" to indicate block erase suspend status. The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After the host writes a Block Erase Resume command to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and RDY/BSY# will return to V_{OL}. After the host writes the Erase Resume command, the device automatically outputs status register data when read. Block erase cannot resume until word write operation initiated during block erase suspend have completed.

8. 8 Word Write Suspend Command

The Word Write Suspend command allows word write interruption to read data in other flash memory locations. Once the word write process starts, writing the Word Write Suspend command requests that the WSM suspend the word write sequence at a predetermined point in the algorithm. After the host writes the Word Write Suspend command, it should write the Read Status Register command. Polling status register bits SR.7 and SR.2 can determine when the WSM suspends the byte write operation (both will be set to "1"). RDY/BSY# will also transition to V_{OH}. Specification t_{WHRH1} defines the word write suspend latency. It is also possible that the word write completes before the device has an opportunity to suspend. The host should also check for this condition.

After the word write has been suspended, the host can write the Read Array command to read data from any location except the suspended location. The only other valid commands while word write is suspended are Read Status Register and Word Write Resume. After the host writes a Word Write Resume to the CUI, the WSM will continue the word write process. Status register bits SR.2 and SR.7 will automatically clear and RDY/BSY# will return to V_{OL}. After the host writes the Word Write Resume command, the device automatically outputs status register data when read.

8. 9 Set Block Lock-Bit Command

The host can enable a flexible block locking and unlocking scheme using the Set Block Lock-Bit command. This command enables the host to lock individual blocks within the flash array. The block lock-bits gate program and erase operations.

The host sets the block lock-bit using a two-cycle command sequence. The host writes the set block lock-bit setup command along with the appropriate block or device address. This command is followed by the set block lock-bit confirm command (and an address within the block to be locked). The WSM controls the set lock-bit algorithm. After the host completes the command sequence, the card automatically outputs status register data when read. The CPU can detect the completion of the set lock-bit event by analyzing the RDY/BSY# pin output or status register bit SR.7.

When the WSM completes the set lock-bit operation, the host should check status register bit SR.4. If the host detects an error it should clear the status register. The CUI will remain in read status register mode until the host issues a new command.

This two-step sequence of set-up followed by execution ensures that the host does not accidentally set the lock-bits. An invalid Set Block Lock-Bit command will result in the WSM setting status register bits SR.4 and SR.5 to "1".

8.10 Clear Block Lock-Bits Command

The host clears all set block lock-bits in parallel using the Clear Block Lock-Bits command. The host is free to clear block lock-bits using the Clear Block Lock-Bits command.

The host executes the clear block lock-bits operation using a two-cycle command sequence. The host must first issue a Clear Block Lock-Bits setup command. This command is followed by a confirm command. After the host completes the two-cycle command sequence, the device automatically outputs status register data when read. The CPU can detect completion of the clear block lock-bits event by analyzing the RDY/BSY# pin output or status register bit SR.7.

When the WSM completes the operation, the host should check status register bit SR.5. If the host detects a clear block lock-bit error, the host should clear the status register. The CUI will remain in read status register mode until the host issues another command.

This two-step sequence of set-up followed by execution ensures that the host does not accidentally clear block lock-bits. An invalid Clear Block Lock-Bits command sequence will result in the WSM setting status register bits SR.4 and SR.5 to "1".

If a clear block lock-bits operation is aborted due to V_{CC} transitioning out of valid range or RESET active transition, block lock-bit values are left in an undetermined state. The host must repeat the clear block lock-bits command to initialize block lock-bit contents to known values.

8.11 Status Register

The memory devices in this card have Status Register which shows state of the device.

Byte Access × 8 Bits

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SR. 7	SR. 6	SR. 5	SR. 4	SR. 3	SR. 2	SR. 1	SR. 0
WSMS	ESS	ECLBS	BWSLBS	VPPS	BWSS	DPS	RFU

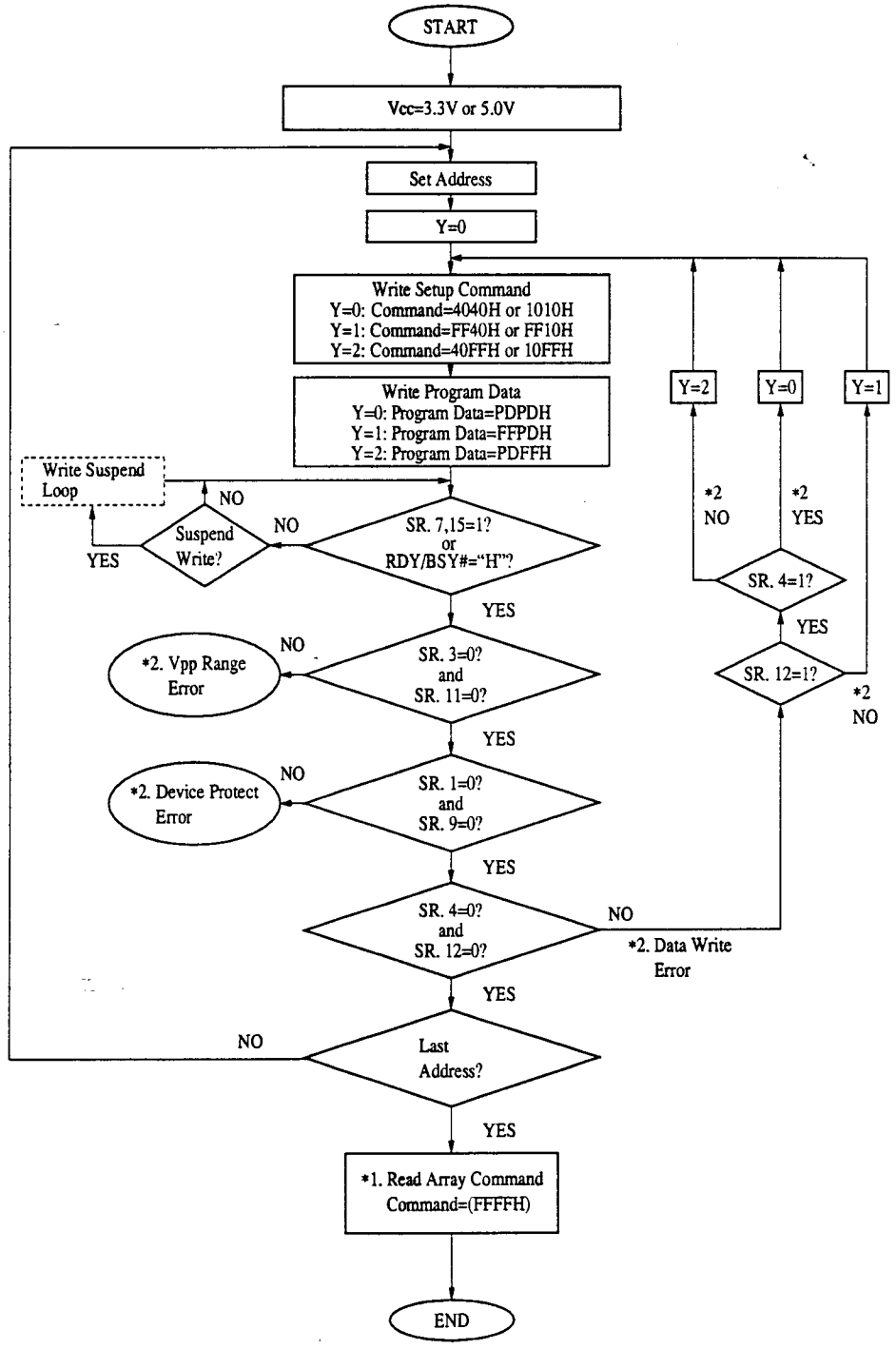
Table 4. Status Register Definition

SR. 7 = WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy SR. 6 = ERASE SUSPEND STATUS 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed SR. 5 = ERASE AND CLEAR LOCK-BITS STATUS 1 = Error in Block Erasure or Clear Lock-Bits 0 = Successful Block Erase or Clear Lock-Bits SR. 4 = BYTE WRITE AND SET LOCK-BIT STATUS 1 = Error in Byte Write or Set Block Lock-Bit 0 = Successful Byte Write or Set Block Lock-Bit SR. 3 = V_{PP} STATUS 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK SR. 2 = BYTE WRITE SUSPEND STATUS 1 = Byte Write Suspended 0 = Byte Write in Progress/Completed SR. 1 = DEVICE PROTECT STATUS 1 = Block Lock-Bit and/or RP# Lock Detected,Operation Abort 0 = Unlock SR. 0 = RESERVED FOR FUTURE ENHANCEMENTS	NOTES: Check RDY/BSY# or SR.7 to determine block erase, byte write, or lock-bit configuration completion. SR.6-0 are invalid while SR.7 = "0". If both SR.5 and SR.4 are "1"s after a block erase or lock-bit configuration attempt, an improper command sequence was entered. SR.3 indicates the V_{PP} status. However, the Memory Card internally ties V_{PP} to V_{CC} so this bit should not be set to "1". If for some reason this bit is set, the host should write the Clear Status Register command. SR.1 does not provide a continuous indication of block lock-bit values. The WSM interrogates the block lock-bit, and RP# only after Block Erase, Byte Write, or Lock-Bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set, and/or RP# is not V_{HH}. Reading the block lock configuration codes after writing the Read Identifier Codes command indicates block lock-bit status. SR.0 is reserved for future use and should be masked out when polling the status register.

Word Access × 16 bits

bit15							bit8	bit7							bit0
SR.15	SR.14	SR.13	SR.12	SR.11	SR.10	SR. 9	SR. 8	SR. 7	SR. 6	SR. 5	SR. 4	SR. 3	SR. 2	SR. 1	SR. 0
Odd Byte device								Even Byte device							

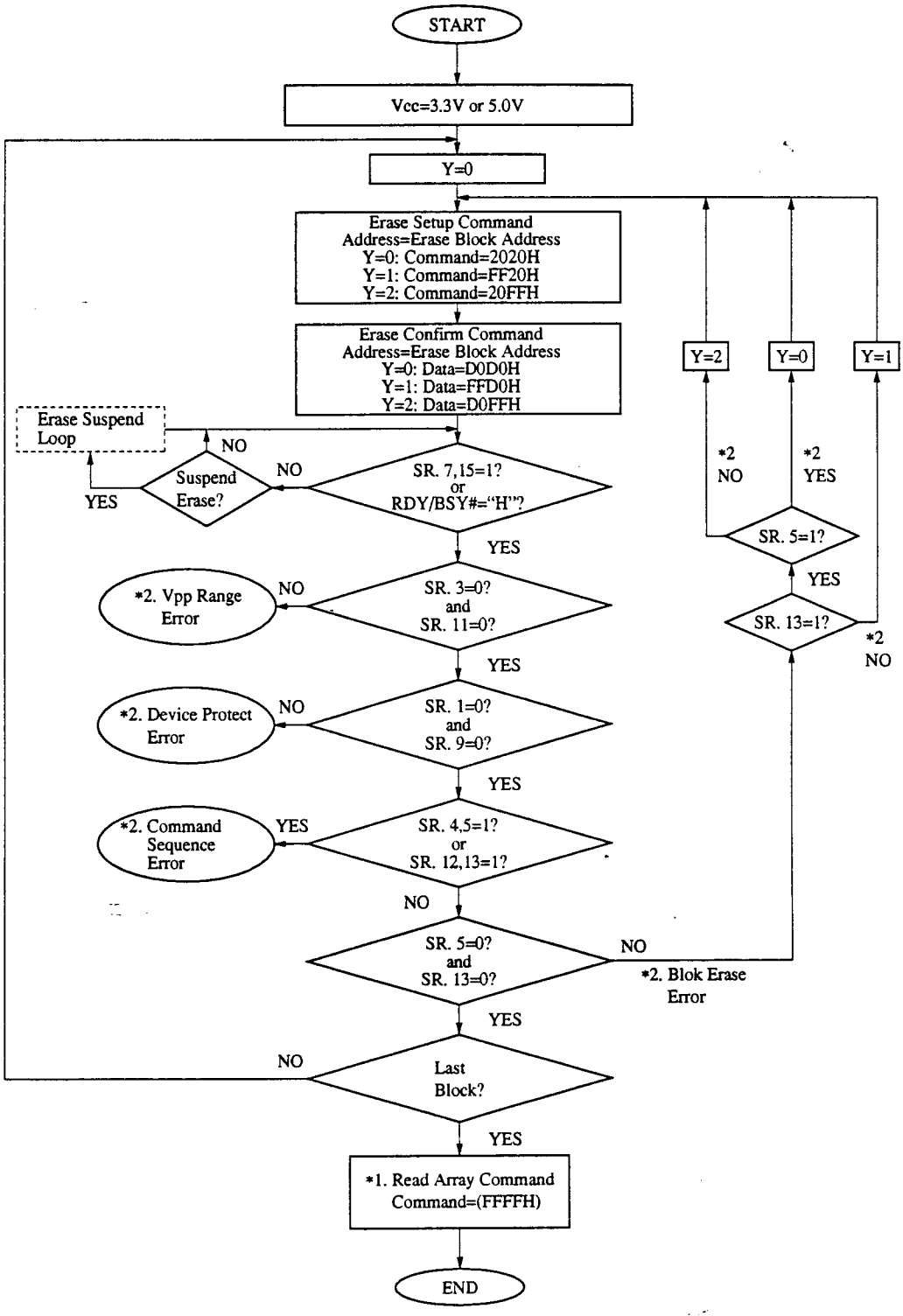
8.12 Automated Word Write Flowchart



Note) *1. Write FFFFH after the last word write operation to reset the device to Read Array Mode.

*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

8.13 Automated Block Erase Flowchart



Note) *1. Write FFFFH after the last block erase operation to reset the device to Read Array Mode.

*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

9. Electrical Specifications

9. 1 Absolute Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage (2)	V_{CC}	–0.5 to 7.0	V
Input Voltage (2)	V_{IN}	–0.5 to V_{CC} + 0.5 (Max: 7.0)	V
Output Short Circuit Current (3)	I_{OUT}	100	mA
Operating Temperature (1)	T_{OPR}	0 to 60	°C
Storage Temperature	T_{STG}	–20 to 65	°C

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. All specified voltages are with respect to GND.
3. Output shorted for no more than one second. No more than one output shorted at a time.

9. 2 Recommended Operating Conditions

PARAMETER	SYMBOL	MINIMUM	MAXMUM	UNIT
Operating Temperature	T_{OPR}	0	60	°C
Supply Voltage 1	V_{CC1}	3.0	3.6	V
Supply Voltage 2	V_{CC2}	4.75	5.25	V

9. 3 Capacitance

Ta = 25°C, f = 1MHz

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Input Capacitance	C_{IN}	—	12	16	pF	V_{IN} = 0.0V
Input/Output Capacitance	C_{IO}	—	8	12	pF	V_{OUT} = 0.0V

9. 4 AC Input/Output Test Conditions

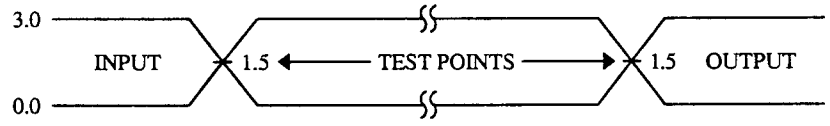


Figure 5. Transient Input/Output Reference Waveform for V_{CC} = 3.3V ± 0.3V and V_{CC} = 5.0V ± 5% (Standard Testing Configuration)
AC test inputs are driven at 3.0V for a Logic " 1 " and 0.0V for a Logic " 0 ". Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) < 10ns.

10. DC Characteristics

(Ta = 0~60°C)

PARAMETER	SYMBOL	NOTES	V_{CC} = 3.3V		V_{CC} = 5.0V		UNIT	TEST CONDITIONS
			MIN	MAX	MIN	MAX		
Input Leakage Current (A1–A20)	I_{LI1}	1	—	±1	—	±2	μA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
Input Leakage Current (RESET)	I_{LI2}	1	–1	40	–1	60	μA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
Input Leakage Current (CE1#, CE2#, WE#)	I_{LI3}	1	–40	1	–60	1	μA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
Input Leakage Current (OE#)	I_{LI4}	1	–45	1	–65	2	μA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
Output Leakage Current (D0–D15)	I_{LO}	1	—	±0.5	—	±10	μA	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND
V_{CC} Standby Current	I_{CCS}	1, 3	—	280	—	280	μA	V_{CC} = V_{CC} Max, CE1# ,CE2# = V_{CC} ± 0.2V, RESET = GND ± 0.2V
V_{CC} Deep Power-Down Current	I_{CCD}	1, 3	—	85	—	95	μA	RESET = V_{CC} ± 0.2V, I_{OUT} (RDY/BSY#)=0 mA
V_{CC} Read Current	I_{CCR}	1, 3, 4, 5	—	25	—	75	mA	V_{CC} = V_{CC} Max, CE1#,CE2#= GND±0.2V,t_{cycle}=150ns@3.3V, t_{cycle} =100ns@5.0V, I_{OUT} =0 mA
V_{CC} Word Write or Set Lock-Bit Current	I_{CCW}	1, 5	—	115	—	150	mA	
V_{CC} Block Erase or Clear Lock-Bit Current	I_{CCE}	1, 5	—	75	—	100	mA	
V_{CC} Word Write or Block Erase Suspend Current	I_{CCWS} I_{CCES}	1, 2, 5	—	12	—	20	mA	CE1# = CE2# = V_{IH}

PARAMETER	SYMBOL	NOTES	V_{CC} = 3.3V		V_{CC} = 5.0V		UNIT	TEST CONDITIONS
			MIN	MAX	MIN	MAX		
Input Low Voltage	V_{IL}		0	0.8	0	0.8	V	
Input High Voltage	V_{IH}		0.7 V_{CC}	V_{CC}	0.7 V_{CC}	V_{CC}	V	
Output Low Voltage	V_{OL}		—	0.4	—	0.45	V	V_{CC}=V_{CC}Min,I_{OL}=4mA@5.0V, I_{OL}=2mA@3.3V
Output High Voltage	V_{OH}		V_{CC}–0.4	—	V_{CC}–0.4	—	V	V_{CC} = V_{CC} Min I_{OH} = -100 μA
V_{CC} Lockout Voltage	V_{LKO}		2.0	—	2.0	—	V	

NOTES:

1. All currents are in RMS unless otherwise noted.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected.If read or byte written while in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. CMOS inputs are either V_{CC} ± 0.2V or GND ± 0.2V.
4. Automatic Power Savings (APS) reduces typical I_{CCR} to 2mA at 5V V_{CC} and 6 mA at 3.3V V_{CC} in static operation (addresses not switching).
5. All values are based on word accesses. Values for byte accesses are 50% of the specification listed.

11. AC Characteristics (Ta = 0~60°C)

Testing Conditions :

1) Input Pulse Level : 0.0V ~ 3.0V
2) Input Rise/Fall Time : 10ns
3) Input/Output Timing Reference Level : 1.5V
4) Output Load : 30pF (including scope and jig capacitance).

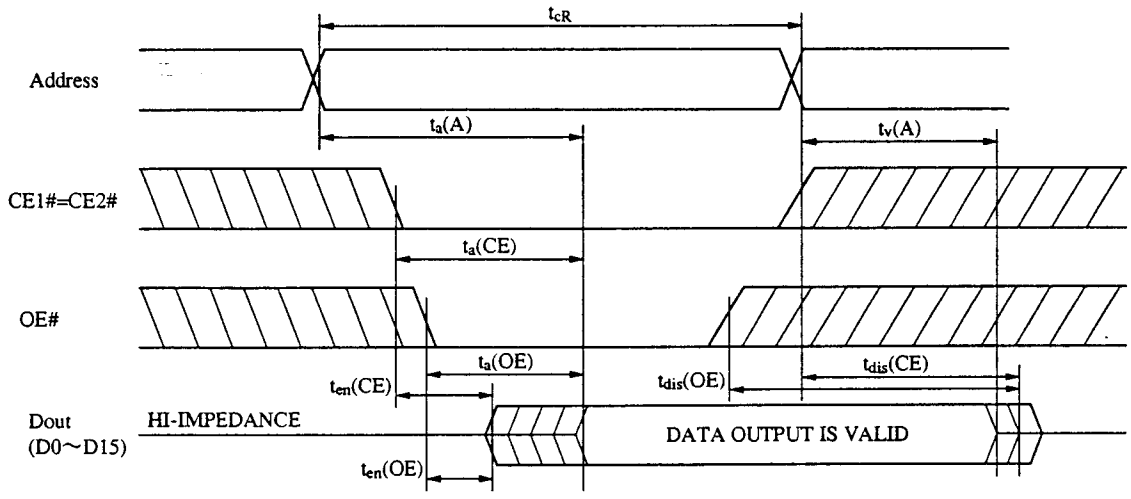
11. 1 Read Operations

(Ta = 0~60°C)

PARAMETER	SYMBOL		V_{CC} = 3.3V		V_{CC} = 5.0V		UNIT
	IEEE	PCMCIA	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{AVAV}	t_{cR}	150	—	100	—	ns
Address Access Time	t_{AVQV}	t_a (A)	—	150	—	100	
Card Enable Access Time	t_{ELQV}	t_a(CE)	—	150	—	100	
Output Enable Access Time	t_{GLQV}	t_a(OE)	—	75	—	50	
Output Disable Time from CE#*	t_{EHQV}	t_{dis} (CE)	—	75	—	50	
Output Disable Time from OE#*	t_{GHQZ}	t_{dis} (OE)	—	75	—	50	
Output Enable Time from CE#	t_{ELQNZ}	t_{en} (CE)	5	—	5	—	
Output Enable Time from OE#	t_{GLQNZ}	t_{en} (OE)	5	—	5	—	
Data Valid from Address Change	t_{AXQX}	t_v (A)	0	—	0	—	
Power-Down Recovery to Output Delay	t_{PHQV}		—	800	—	530	

* Time until output becomes floating. (The output voltage is not defined.)

11. 2 AC Waveforms for Read Operations



Note) 1. WE# = "HIGH", during a read cycle.

2. Either "HIGH" or "LOW" in diagonal areas.

3. The output data becomes valid when last interval, ta (A), ta (CE) or ta (OE) have concluded.

11. 3 Write Operations

11. 3. 1 WE# Controlled Write Operations

(Ta = 0~60°C)

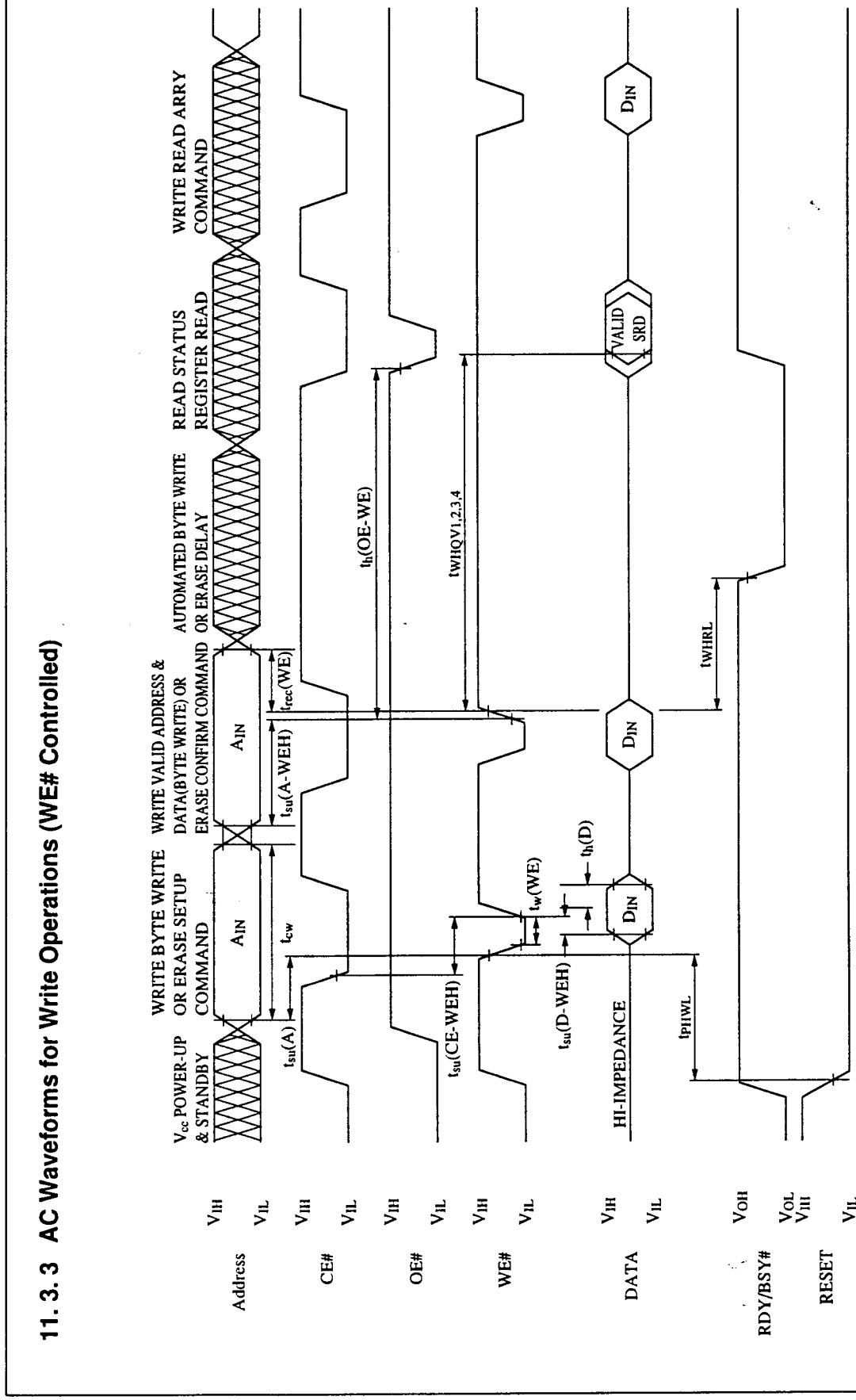
PARAMETER	SYMBOL		V_{CC} = 3.3V		V_{CC} = 5.0V		UNIT
	IEEE	PCMCIA	MIN	MAX	MIN	MAX	
Write Cycle Time	t_{AVAV}	t_{cW}	150	—	100	—	ns
Address Setup Time	t_{AVWL}	t_{su} (A)	20	—	10	—	
Write Recovery Time	t_{WHAX}	t_{rec} (WE)	20	—	15	—	
Data Setup Time for WE#	t_{DVWH}	t_{su} (D-WEH)	50	—	40	—	
Data Hold Time	t_{WHDX}	t_h (D)	20	—	15	—	
Output Enable Hold from WE#	t_{WHGL}	t_h (OE-WE)	10	—	10	—	
Card Enable Setup time for WE#	t_{ELWH}	t_{su} (CE-WEH)	100	—	70	—	
Address Setup for WE#	t_{AVWH}	t_{su} (A-WEH)	100	—	70	—	
Write Pulse Width	t_{WLWH}	t_w (WE)	80	—	60	—	
WE# High to RDY/BSY# Going Low	t_{WHRL}		—	300	—	150	
Power-Down Recovery to WE# Going Low	t_{PHWL}		1	—	1	—	μs

11. 3. 2 CE# Controlled Write Operations

(Ta = 0~60°C)

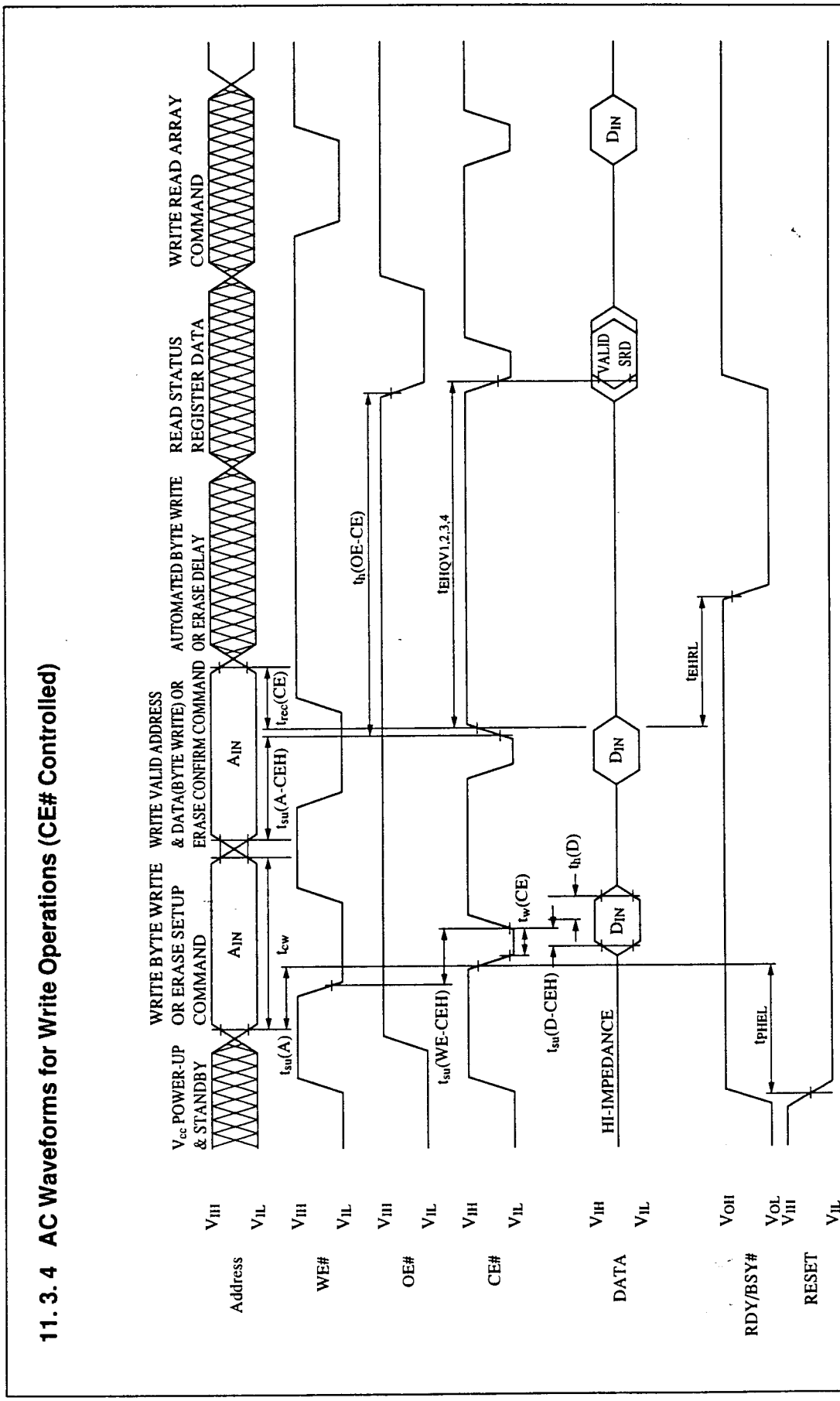
PARAMETER	SYMBOL		V_{CC} = 3.3V		V_{CC} = 5.0V		UNIT
	IEEE	PCMCIA	MIN	MAX	MIN	MAX	
Write Cycle Time	t_{AVAV}	t_{cW}	150	—	100	—	ns
Address Setup Time	t_{AVEL}	t_{su} (A)	20	—	10	—	
Write Recovery Time	t_{EHAX}	t_{rec} (CE)	20	—	15	—	
Data Setup Time for CE#	t_{DVEH}	t_{su} (D-CEH)	50	—	40	—	
Data Hold Time	t_{EHDX}	t_h (D)	20	—	15	—	
Output Enable Hold from CE#	t_{EHGL}	t_h (OE-CE)	10	—	10	—	
Write Enable Setup time for CE#	t_{WLEH}	t_{su} (WE-CEH)	100	—	70	—	
Address Setup for CE#	t_{AVEH}	t_{su} (A-CEH)	100	—	70	—	
Card Enable Pulse Width	t_{ELEH}	t_w (CE)	80	—	60	—	
CE# High to RDY/BSY# Going Low	t_{EHRL}		—	300	—	150	
Power-Down Recovery to CE# Going Low	t_{PHEL}		1	—	1	—	μs

11. 3. 3 AC Waveforms for Write Operations (WE# Controlled)



Note) While the data signal is in output mode, do not apply an opposite phase input signal.

11.3.4 AC Waveforms for Write Operations (CE# Controlled)



Note) While the data signal is in output mode, do not apply an opposite phase input signal.

11.4 Erase and Data Write Performance

(Ta = 0~60°C)

PARAMETER	SYMBOL	NOTES	V_{CC} = 3.3V			V_{CC} = 5.0V			UNIT
			MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
Byte Write Time	t_{WHQV1} t_{EHQV1}	2	15	17	—	6.5	8	—	µs
Block Write Time		2	1	1.1	—	0.4	0.5	—	s
Block Erase Time	t_{WHQV2} t_{EHQV2}	2	1.5	1.8	—	0.9	1.1	—	s
Set Lock-Bit Time	t_{WHQV3} t_{EHQV3}	2	18	21	—	9.5	12	—	µs
Clear Block Lock-Bits Time	t_{WHQV4} t_{EHQV4}	2	1.5	1.8	—	0.9	1.1	—	s
Byte Write Suspend Latency Time to Read	t_{WHRH1} t_{EHRH1}	—	—	6	7	—	5	6	µs
Erase Suspend Latency Time to Read	t_{WHRH2} t_{EHRH2}	—	—	16.2	20	—	9.6	12	µs

NOTES:

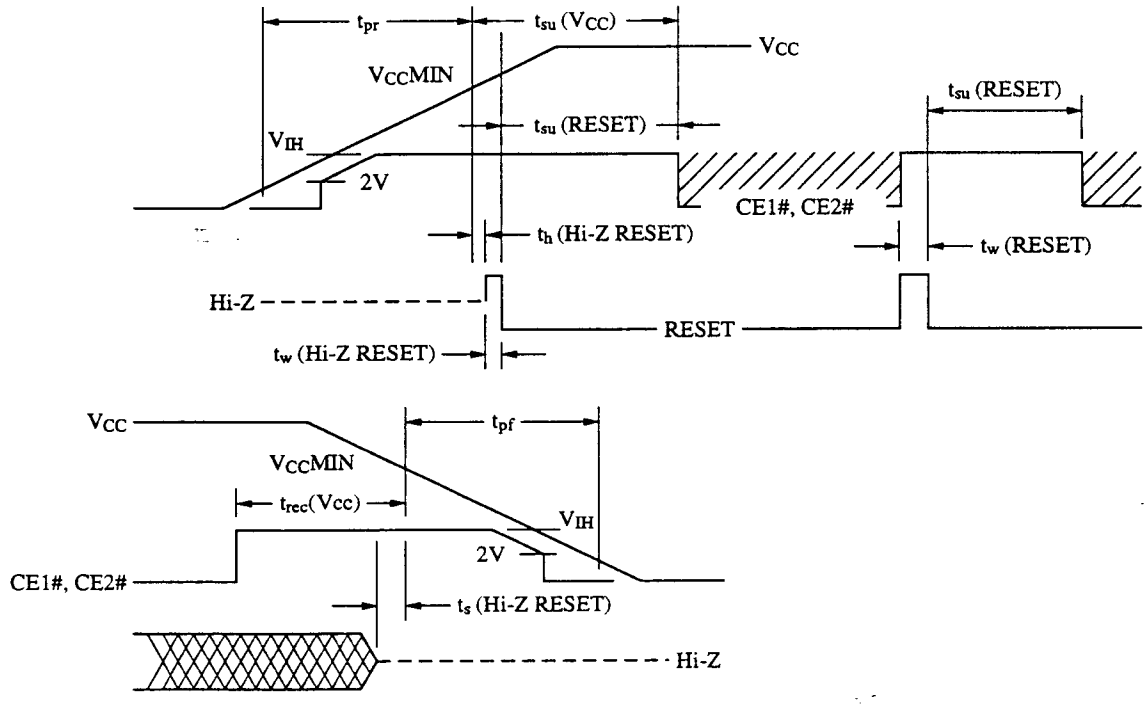
1. Typical values measured at Ta = 25°C and norminal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. Sampled but not 100% tested.

11.5 Power-Up/Power Down

PARAMETER	SYMBOL PCMCIA	NOTES	MIN	MAX	UNITS
CE# Signal Level (0.0V < V_{CC} < 2.0V)	V_i (CE)	1	0	V_{iMAX}	V
CE# Signal Level (2.0V < V_{CC} < V_{IH})		1	V_{CC}–0.1	V_{iMAX}	V
CE# Signal Level (V_{IH} < V_{CC})		1	V_{IH}	V_{iMAX}	V
CE# Setup Time	t_{su} (V_{CC})	—	20	—	ms
RESET Setup Time	t_{su} (RESET)	—	20	—	ms
CE# Recover Time	t_{rec} (V_{CC})	—	1.0	—	μs
V_{CC} Rising Time	t_{pr}	2	0.1	300	ms
V_{CC} Falling Time	t_{pf}	2	3.0	300	ms
RESET Width	t_w (RESET)	—	10	—	μs
RESET Width	t_h (Hi–Z RESET)	—	1	—	ms
RESET Width	t_s (Hi–Z RESET)	—	0	—	ms

NOTES:

1. V_{iMAX} means Absolute Maximum Voltage for input in the period of 0.0V < V_{CC} < 2.0 V, Vi (CE#) is only 0.00V-V_{iMAX}
2. The t_{pr} and t_{pf} are defined as "linear waveforms" in the period of 10% to 90%, or vice-versa. Even if the waveform is not a "liner waveform," its rising and falling time must meet this specification.



Power-Up/Down Timing fot Systems Supporting RESET

12. Specification Changes

Specifications may be changed upon discussion and agreement between both parties.

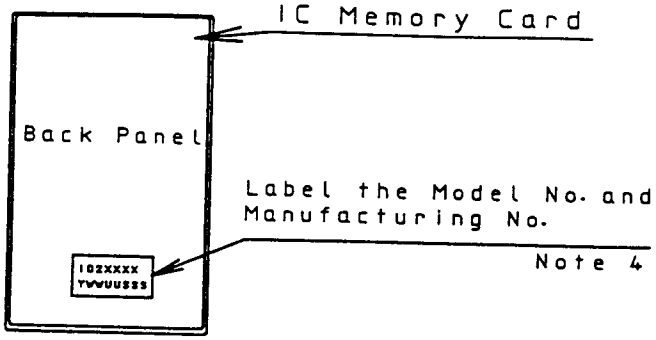
13. Other Precautions

- Permanent damage occures if the memory card is stressed beyond Absolute Maximum Ratings. Operation beyond the Recommended Operating Conditions is not recommended and extended exposure beyond the Recommeded Operating Conditions may affect device reliability.
- Writing to the memory card can be prevented by switching on the write protect switch on the end of the memory card.
- Avoid allowing the memory card connectors to come in contact with metals and avoid touching the connectors, as the internal circuits can be damaged by static electricity.
- Avoid storing in direct sunlight, high temperatures (do not place near heaters or radiators), high humidity and dusty areas.
- Avoid subjecting the memory card to strong physical abuse. Dropping, bending, smashing or throwing the card can result in loss of function.
- When the memory card is not being used, return it to its protective case.
- Do not allow the memory card to come in contact with fire.

SHARP

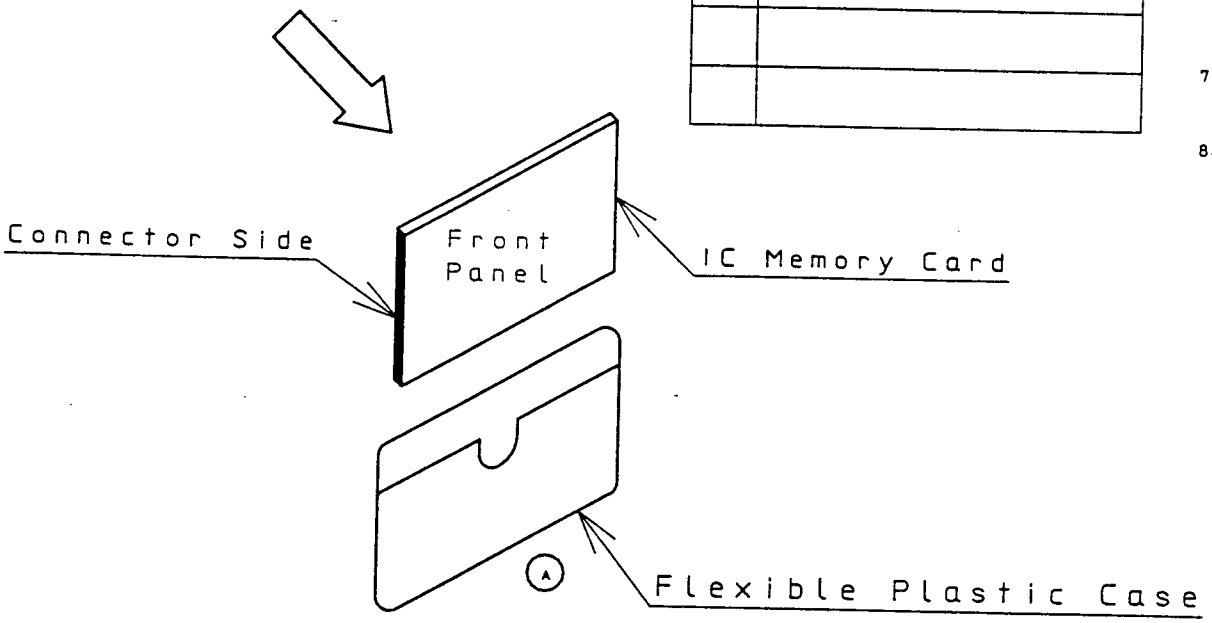
15. Packing Specification

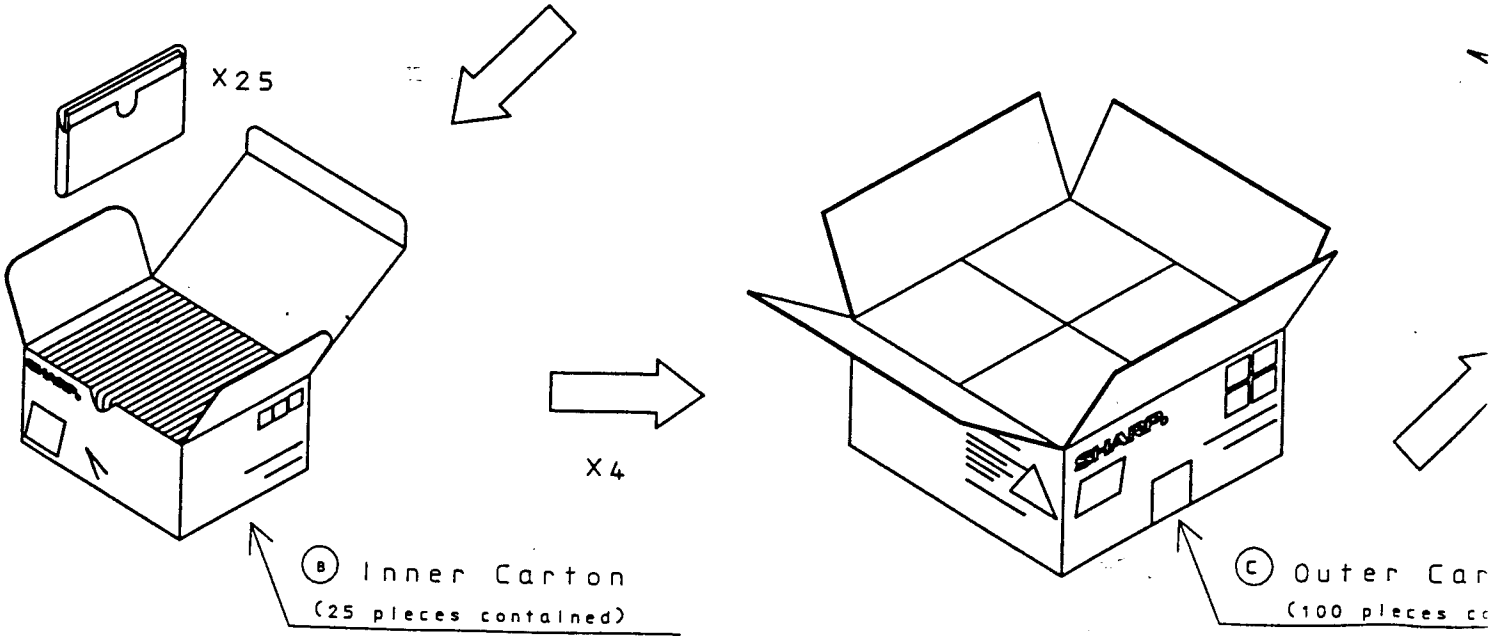
Connector Side



Parts List

	Parts Name
A	Flexible Plastic Case
B	Inner Carton (25 pieces contained)
C	Outer Carton (100 pieces contained)
D	Outer Case (400 pieces contained)





Packing S

1. Label the Mode of the card.
2. Each memory co (The frontside c is released, and point, so that th in the figure.)
3. The inner cart case. (Note 1.
4. The product na are either wri on the label w
5. The outer cart
6. The product na are either wri on the label w
7. The outer cart contains 4 out
8. The product nar are either wri label which is

king Specification

el the Model No. and Manufuring No. on the back panel the card.

h memory card is contained in the flexible plastic case. frontside of the card comes to the place where the card leased, and the connector side is placed against to this , so that the connector is not touched by finger, as shown e figure.)

inner carton contains 25 pieces of the card with the e. (Note 1.)

product name, Lot no. (product no.), quantity and the date either written directly on the inner carton, or printed the label which is then attached on inner carton.

outer carton contains 4 inner cartons. (Note 2.)

product name, lot no. (product no.), quantity and the date either written directly on the outer carton, or printed the label which is then attached on the outer carton.

outer carton is then put in the outer case, which tains 4 outer cartons. (Note 3.)

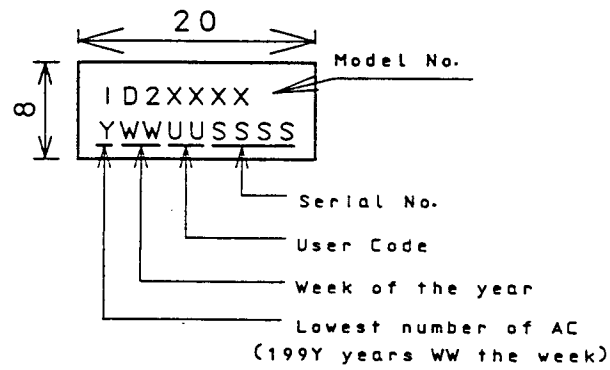
product name, Lot no. (product no.), quantity and the date either written directly on the case or printed on the el which is then attached on the case.

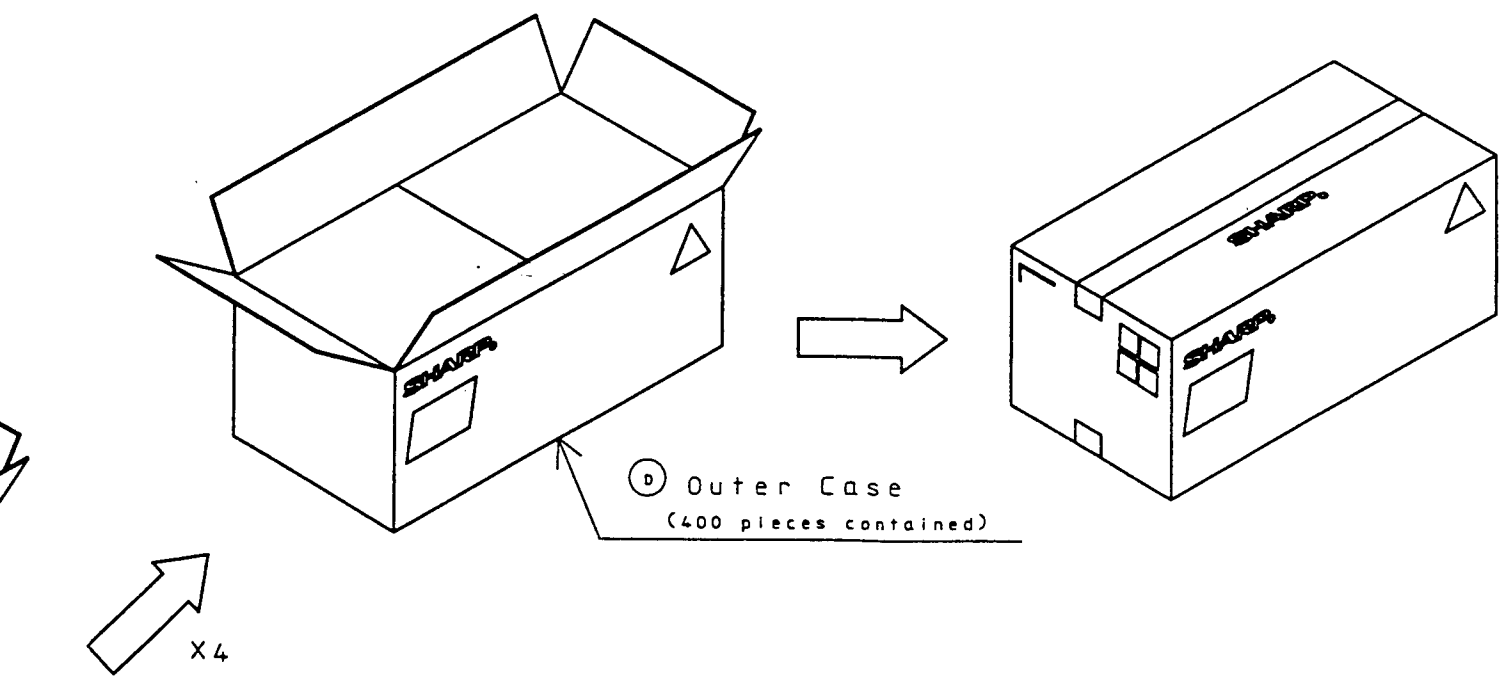
Note 1. The least packing unit is 25 pieces, which is the number contained in the inner carton.

2. The space inside the outer carton is filled card board.

3. The other size of outer case may be used if there is not enough quantity to fill the normal outer case which can contain 4 outer cartons.

4. Size of label and denetations are folloeus. [unit:mm]



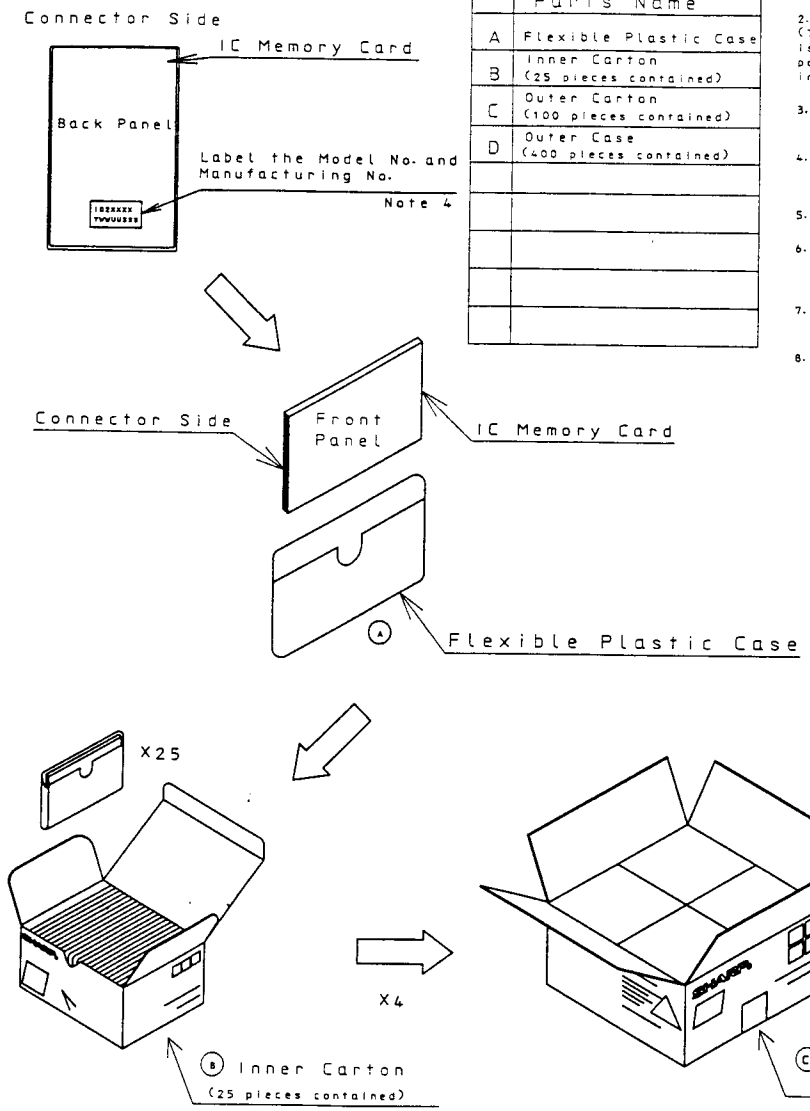


Outer Carton
(400 pieces contained)

APPLICABLE MODEL	ID243XXX	SCALE	UNIT mm	A		
				A		
				CH. DATE	REVISE	CHARGE
THICKNESS	DEFFERENCE	MATERIAL	FINISH	NAME	ID243XXX Packing Specification	
DATE	1996. 12. 25					
K. Bashiwato	S. Sasaki	S. Shintani	MEMORY CARD BUSINESS PROJECT TEAM INTEGRATED CIRCUITS GROUP SHARP CORPORATION	DRAWING NO.	IMC073-J300	

SHARP

15. Packing Specification



Parts List

	Parts Name
A	Flexible Plastic Case
B	Inner Carton (25 pieces contained)
C	Outer Carton (100 pieces contained)
D	Outer Case (400 pieces contained)

Packing Specification

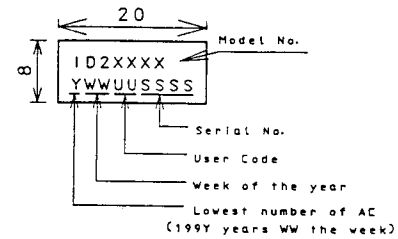
1. Label the Model No. and Manufuring No. on the back panel of the card.
2. Each memory card is contained in the flexible plastic case. (The fronts.de of the card comes to the place where the card is released, and the connector side is placed against to this point, so that the connector is not touched by finger, as shown in the figure.)
3. The inner carton contains 25 pieces of the card with the case. (Note 1.)
4. The product name, Lot no. (product no.), quantity and the date are either written directly on the inner carton, or printed on the label which is then attached on inner carton.
5. The outer carton contains 4 inner cartons. (Note 2.)
6. The product name, lot no. (product no.), quantity and the date are either written directly on the outer carton, or printed on the label which is then attached on the outer carton.
7. The outer carton is then put in the outer case, which contains 4 outer cartons. (Note 3.)
8. The product name, Lot no. (product no.), quantity and the date are either written directly on the case or printed on the label which is then attached on the case.

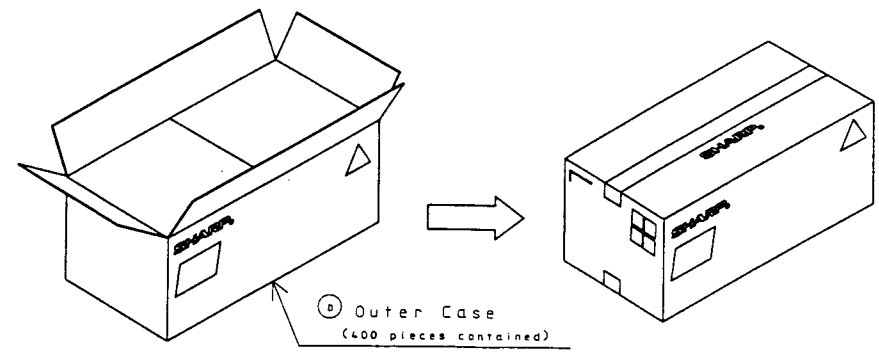
Note 1. The least packing unit is 25 pieces, which is the number contained in the inner carton.

2. The space inside the outer carton is filled card board.

3. The other size of 'outer case may be used if there is not enough quantity to fill the normal outer case which can contain 4 outer cartons.

4. Size of label and denetations are folloeus. [unit:mm]





APPLICABLE MODEL	ID243XXX	SCALE	UNIT mm	CH. DATE	REVISE	CHARGE
THICKNESS	DEFFERENCE	MATERIAL	FINISH	NAME	ID243XXX Packing Specification	
DATE	1996. 12. 25	MEMORY CARD BUSINESS PROJECT TEAM				
K. Deshiro	S. Sawaki	INTEGRATED CIRCUITS GROUP				
		SHARP CORPORATION		DRAWING NO.	IMC073-J300	

FLASH MEMORY FLASH NON-VOLATILE MEMORY FLASH E2ROM FLASH ROM READ ONLY MEMORY ETOX ID243D01 2M PC Card Conforms to PCMCIA Rel. 2.0