Integrated Circuit Systems, Inc.

# ICS952302

## Frequency Generator for Transmeta™ Efficeon™

**Recommended Application:**

Transmeta Effician, ATi M6

**Output Features:**

- 3 - CPUs @ 3.3V including 1 free running CPUCLK_F
- 7 - PCI @ 3.3V, including 4 free running PCICLK_F
- 1 - 27MHz clock @ 3.3V
- 2 - 48MHz clocks @ 3.3V
- 2 - REF clocks @3.3V

**Key Specifications:**

- CPU output jitter: < 250ps
- PCI output skew: < 250ps
- CPUT - PCI output skew: 1-3ns
- 27MHz Accuracy < 50ppm
- 48MHz Accuracy < 50ppm

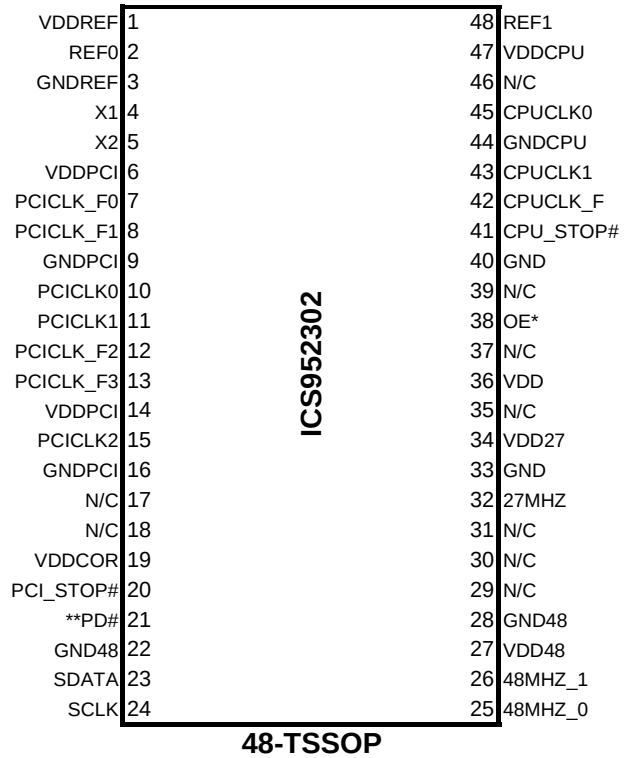
**Features:**

- Support I2C Index read/write and block read/write operations.
- Uses external 14.318MHz referience input or XTAL.
- Full Load Power consumption reduced >10% compared to reference device
- Power management via SMBus

## Functionality

| Byte 4b7 | Byte 4b6 | Byte 4b5 | Spread % | |
|---|---|---|---|---|
| 0 | 0 | 0 | +/-0.3 | CENTER |
| 0 | 0 | 1 | +/-0.6 | |
| 0 | 1 | 0 | +/-0.25 | |
| 0 | 1 | 1 | +/-0.45 | |
| 1 | 0 | 0 | -0.60% | DOWN |
| 1 | 0 | 1 | -1.20% | |
| 1 | 1 | 0 | -0.50% | |
| 1 | 1 | 1 | -0.90% | |

## Pin Configuration




**48-TSSOP**

* Internal Pull-Up Resistor

**No Diode Clamp to VDD

## Pin Descriptions

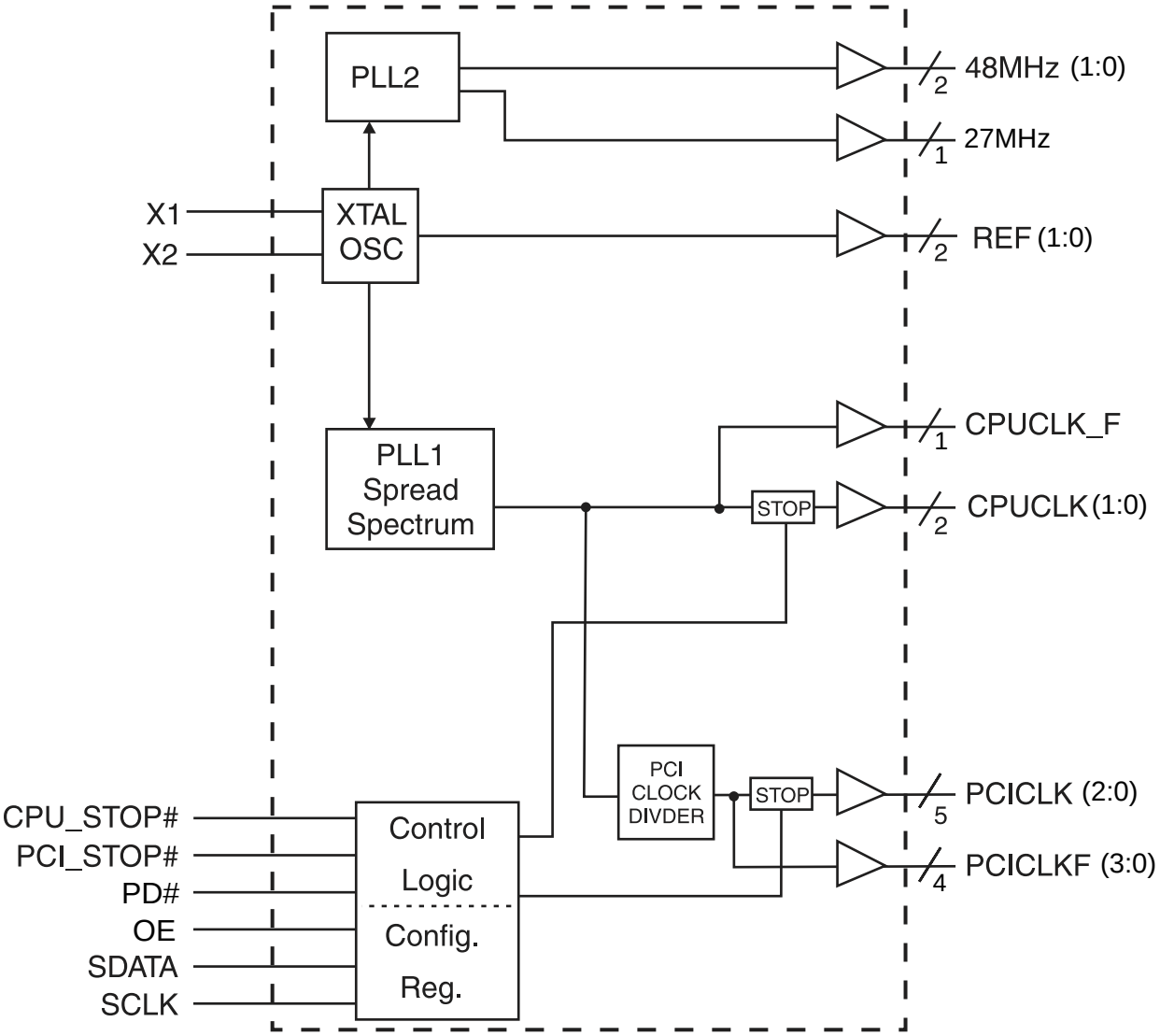
| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | VDDREF | PWR | Ref, XTAL power supply, nominal 3.3V |
| 2 | REF0 | OUT | 14.318 MHz reference clock. |
| 3 | GNDREF | PWR | Ground pin for the REF outputs. |
| 4 | X1 | IN | Crystal input, Nominally 14.318MHz. |
| 5 | X2 | OUT | Crystal output, Nominally 14.318MHz |
| 6 | VDDPCI | PWR | Power supply for PCI clocks, nominal 3.3V |
| 7 | PCICLK_F0 | OUT | Free running PCI clock not affected by PCI_STOP# . |
| 8 | PCICLK_F1 | OUT | Free running PCI clock not affected by PCI_STOP# . |
| 9 | GNDPCI | PWR | Ground pin for the PCI outputs |
| 10 | PCICLK0 | OUT | PCI clock output. |
| 11 | PCICLK1 | OUT | PCI clock output. |
| 12 | PCICLK_F2 | OUT | Free running PCI clock not affected by PCI_STOP# . |
| 13 | PCICLK_F3 | OUT | Free running PCI clock not affected by PCI_STOP# . |
| 14 | VDDPCI | PWR | Power supply for PCI clocks, nominal 3.3V |
| 15 | PCICLK2 | OUT | PCI clock output. |
| 16 | GNDPCI | PWR | Ground pin for the PCI outputs |
| 17 | N/C | N/C | No Connection. |
| 18 | N/C | N/C | No Connection. |
| 19 | VDDCOR | PWR | 3.3V power for the PLL core. |
| 20 | PCI_STOP# | IN | Stops all PCICLKs at logic 0 level, when low. Free running PCICLKs are not effected by this input. |
| 21 | **PD# | IN | Asynchronous active low input pin, with 120Kohm internal pull-up resistor, used to power down the device. The internal clocks are disabled and the VCO and the crystal are stopped. |
| 22 | GND48 | PWR | Ground pin for the 48MHz outputs |
| 23 | SDATA | I/O | Data pin for SMBus circuitry, 5V tolerant. |
| 24 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |
| 25 | 48MHZ_0 | OUT | 48MHz clock output. |
| 26 | 48MHZ_1 | OUT | 48MHz clock output. |
| 27 | VDD48 | PWR | Power pin for the 48MHz output.3.3V |
| 28 | GND48 | PWR | Ground pin for the 48MHz outputs |
| 29 | N/C | N/C | No Connection. |
| 30 | N/C | N/C | No Connection. |
| 31 | N/C | N/C | No Connection. |
| 32 | 27MHZ | OUT | 27.0000MHz Video Clock for ATi Chipset |
| 33 | GND | PWR | Ground pin. |
| 34 | VDD27 | PWR | Power pin for the 27MHz output.3.3V |
| 35 | N/C | N/C | No Connection. |
| 36 | VDD | PWR | Power supply, nominal 3.3V |
| 37 | N/C | N/C | No Connection. |
| 38 | OE* | IN | Active high input for enabling Memory Channel outputs.<br>0 = tri-state outputs, 1= enable outputs |
| 39 | N/C | N/C | No Connection. |
| 40 | GND | PWR | Ground pin. |
| 41 | CPU_STOP# | IN | Stops all CPUCLK, except those set to be free running clocks |
| 42 | CPUCLK_F | OUT | Free running CPU clock. Not affected by the CPU_STOP#. |
| 43 | CPUCLK1 | OUT | CPU clock outputs. 3.3V |
| 44 | GNDCPU | PWR | Ground pin for the CPU outputs |
| 45 | CPUCLK0 | OUT | CPU clock outputs. 3.3V |
| 46 | N/C | N/C | No Connection. |
| 47 | VDDCPU | PWR | Supply for CPU clocks, 3.3V nominal |
| 48 | REF1 | OUT | 14.318 MHz reference clock. |

* Internal Pull-Up Resistor ** No diode clamp to VDD.

## General Description

Spread spectrum may be enabled through SMBus programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS952302** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

## Block Diagram



**SMBus Table: Output Control Register**

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | 42 | CPUCLK_F | Output Enable | RW | Disable | Enable | 1 |
| **Bit 6** | 45 | CPUCLK0 | Output Enable | RW | Disable | Enable | 1 |
| **Bit 5** | 43 | CPUCLK1 | Output Enable | RW | Disable | Enable | 1 |
| **Bit 4** | 32 | 27MHZ | Output Enable | RW | Disable | Enable | 1 |
| **Bit 3** | 25 | 48MHZ_0 | Output Enable | RW | Disable | Enable | 1 |
| **Bit 2** | 26 | 48MHZ_1 | Output Enable | RW | Disable | Enable | 1 |
| **Bit 1** | 2 | REF0 | Output Enable | RW | Disable | Enable | 1 |
| **Bit 0** | 48 | REF1 | Output Enable | RW | Disable | Enable | 1 |

**SMBus Table: Output Control Register**

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | 7 | PCICLK_F0 | Test Mode | RW | Disable | Enable | 1 |
| **Bit 6** | 8 | PCICLK_F1 | Output Enable | RW | Disable | Enable | 1 |
| **Bit 5** | 12 | PCICLK_F2 | Output Enable | RW | Disable | Enable | 1 |
| **Bit 4** | 13 | PCICLK_F3 | Output Enable | RW | Disable | Enable | 1 |
| **Bit 3** | 10 | PCICLK0 | Spread Control | RW | Disable | Enable | 1 |
| **Bit 2** | 11 | PCICLK1 | Output Enable | RW | Disable | Enable | 1 |
| **Bit 1** | 15 | PCICLK2 | Output Enable | RW | Disable | Enable | 1 |
| **Bit 0** | - | Spread Spectrum Mode | Spread Control for PLL1 | RW | OFF | ON | 0 |

**SMBus Table: Output Control Register**

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | 42 | CPUCLK_F | Allow assertion of CPU_STOP# or setting of CPU_STOP control bit in SMBus register to stop CPU clocks | RW | Free Running | Stoppable | 0 |
| **Bit 6** | 45 | CPUCLK0 | | RW | Free Running | Stoppable | 1 |
| **Bit 5** | 43 | CPUCLK1 | | RW | Free Running | Stoppable | 1 |
| **Bit 4** | - | Reserved | Reserved | RW | - | - | x |
| **Bit 3** | - | Reserved | Reserved | RW | - | - | x |
| **Bit 2** | (note) | CPU_STOP | Stop all CPU clocks | RW | Enable | Disable | 1 |
| **Bit 1** | - | Reserved | Reserved | RW | - | - | x |
| **Bit 0** | 20, 41 | CPU_STOP# PCI_STOP# | H/w or S/w Select | RW | H/W | I2C | 1 |

**Note:** Byte2bit2=0 (Enable) to stop all CPUCLK's ONLY when Byte2 bit(5:7) at STOPPABLE MODE

**SMBus Table: Output Control Register**

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | 7 | PCICLK_F0 | Allow assertion of PCI_STOP# or setting of PCI_STOP control bit in SMBus register to stop PCI clocks | RW | Free Running | Stoppable | 0 |
| **Bit 6** | 8 | PCICLK_F1 | | RW | Free Running | Stoppable | 0 |
| **Bit 5** | 12 | PCICLK_F2 | | RW | Free Running | Stoppable | 0 |
| **Bit 4** | 13 | PCICLK_F3 | | RW | Free Running | Stoppable | 0 |
| **Bit 3** | 10 | PCICLK0 | | RW | Free Running | Stoppable | 1 |
| **Bit 2** | 11 | PCICLK1 | | RW | Free Running | Stoppable | 1 |
| **Bit 1** | 15 | PCICLK2 | | RW | Free Running | Stoppable | 1 |
| **Bit 0** | - | PCI_STOP | Stop all PCI clocks | RW | Enable | Disable | 1 |

**SMBus Table: Spread Spectrum Control Register**

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | Spread Position | Center or Down SS | RW | Center | Down | 1 |
| Bit 6 | - | SS1 | Spread Bit 1 | RW | See SS Table | | 0 |
| Bit 5 | - | SS2 | Spread Bit 2 | RW | | | 0 |
| Bit 4 | - | Reserved | | | | | - |
| Bit 3 | - | Reserved | | | | | - |
| Bit 2 | - | Reserved | | | | | - |
| Bit 1 | - | Reserved | | | | | - |
| Bit 0 | - | Reserved | | | | | - |

**SMBus Table: Control Register**

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | Reserved | | | | | - |
| Bit 6 | - | Reserved | | | | | - |
| Bit 5 | - | Reserved | | | | | - |
| Bit 4 | - | Reserved | | | | | - |
| Bit 3 | - | Reserved | | | | | - |
| Bit 2 | - | Reserved | | | | | - |
| Bit 1 | - | Reserved | | | | | - |
| Bit 0 | - | Reserved | | | | | - |

**SMBus Table: Control Register**

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | Reserved | | | | | - |
| Bit 6 | - | Reserved | | | | | - |
| Bit 5 | - | Reserved | | | | | - |
| Bit 4 | - | Reserved | | | | | - |
| Bit 3 | - | Reserved | | | | | - |
| Bit 2 | - | Reserved | | | | | - |
| Bit 1 | - | Reserved | | | | | - |
| Bit 0 | - | Reserved | | | | | - |

**SMBus Table: Vendor & Revision ID Register**

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | RID3 | REVISION ID | R | - | - | x |
| Bit 6 | - | RID2 | | R | - | - | x |
| Bit 5 | - | RID1 | | R | - | - | x |
| Bit 4 | - | RID0 | | R | - | - | x |
| Bit 3 | - | VID3 | VENDOR ID | R | - | - | 0 |
| Bit 2 | - | VID2 | | R | - | - | 0 |
| Bit 1 | - | VID1 | | R | - | - | 0 |
| Bit 0 | - | VID0 | | R | - | - | 1 |

## Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V
Logic Inputs . . . . . GND –0.5 V to $V_{DD}$ +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A$ = 0 - 70°C; Supply Voltage $V_{DD}$ = 3.3 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | | 2 | | $V_{DD}$ + 0.3 | V |
| Input Low Voltage | $V_{IL}$ | | $V_{SS}$ - 0.3 | | 0.8 | V |
| Input High Current | $I_{IH}$ | $V_{IN} = V_{DD}$ | | | 5 | mA |
| Input Low Current | $I_{IL1}$ | $V_{IN}$ = 0 V; Inputs with no pull-up resistors | -5 | | | mA |
| Input Low Current | $I_{IL2}$ | $V_{IN}$ = 0 V; Inputs with pull-up resistors | -200 | | | mA |
| Operating Supply Current | $I_{DD(op)}$ | $C_L$ = (full load); 66MHz | | 102 | 150 | mA |
| Power Down Supply Current | $I_{DDPD}$ | $C_L$ = 0 pF; With input address to Vdd or GND | | 320 | 600 | ◊A |
| Input frequency | $F_i$ | $V_{DD}$ = 3.3 V; | 11 | 14.3132 | 16 | MHz |
| Input Capacitance[1] | $C_{IN}$ | Logic Inputs | | | 5 | pF |
| | $C_{INX}$ | X1 & X2 pins | 27 | | 45 | pF |
| Clk Stabilization[1] | $T_{STAB}$ | From $V_{DD}$ = 3.3 V to 1% target Freq. | | 3 | 5.5 | ms |
| Skew[1] | $T_{CPU-PCI}$ | $V_T$ = 1.5 V | 1 | 1.5 | 4 | ns |

[1]Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - CPU

$T_A$ = 0 - 70°C; $V_{DD}$ = 3.3 V +/-5%; $C_L$ = 10 - 20 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output High Voltage | $V_{OH2B}$ | $I_{OH}$ = -20 mA | 2.4 | 2.9 | | V |
| Output Low Voltage | $V_{OL2B}$ | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | V |
| Output High Current | $I_{OH2B}$ | $V_{OUT}$ = 1 V | | -67 | -29 | mA |
| | | $V_{OUT}$ = 3.135V | -23 | -8 | | |
| Output Low Current | $I_{OL2B}$ | $V_{OUT}$ = 1.95 V | 27 | 56 | | mA |
| | | $V_{OUT}$ =0.4V | | 23 | 30 | |
| Rise Time[1] | $t_{r2B}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 1 | 1.4 | 2 | ns |
| Fall Time[1] | $t_{f2B}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 1 | 1.4 | 2 | ns |
| Duty Cycle[1] | $d_{t2B}$ | $V_T$ = 1.5 V | 45 | 51.5 | 55 | % |
| Skew[1] | $t_{sk2B}$ | $V_T$ = 1.5 V | | 60 | 175 | ps |
| Jitter, Cycle-to-cycle[1] | $t_{jcyc-cyc2B}$ | $V_T$ = 1.5 V | | 175 | 250 | ps |

[1]Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - PCICLK, PCICLK_F

$T_A$ = 0 - 70°C; $V_{DD}$ = 3.3 V +/-5%; $C_L$ = 10 - 20 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output High Voltage | $V_{OH2B}$ | $I_{OH}$ = -20 mA | 2.4 | 2.9 | | V |
| Output Low Voltage | $V_{OL2B}$ | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | V |
| Output High Current | $I_{OH2B}$ | $V_{OUT}$ = 1 V | | -67 | -29 | mA |
| | | $V_{OUT}$ = 3.135V | -23 | -8 | | |
| Output Low Current | $I_{OL2B}$ | $V_{OUT}$ = 1.95 V | 27 | 56 | | mA |
| | | $V_{OUT}$ =0.4V | | 23 | 30 | |
| Rise Time[1] | $t_{r2B}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 1 | 1.3 | 2 | ns |
| Fall Time[1] | $t_{f2B}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 1 | 1.2 | 2 | ns |
| Duty Cycle[1] | $d_{t2B}$ | $V_T$ = 1.5 V | 45 | 50.5 | 55 | % |
| Skew[1] | $t_{sk2B}$ | $V_T$ = 1.5 V | | 68 | 250 | ps |
| Jitter, Cycle-to-cycle[1] | $t_{jcyc-cyc2B}$ | $V_T$ = 1.5 V | | 100 | 250 | ps |

[1]Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - 27MHz

$T_A$ = 0 - 70°C; $V_{DD}$ = 3.3 V +/-5%; $C_L$ = 10 - 20 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Frequency Accuracy | $F_{ACC}$ | REF Out = 14.31818MHz | -50 | 0 | 50 | ppm |
| Output High Voltage | $V_{OH2B}$ | $I_{OH}$ = -20 mA | 2.4 | 2.9 | | V |
| Output Low Voltage | $V_{OL2B}$ | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | V |
| Output High Current | $I_{OH2B}$ | $V_{OUT}$ = 1 V | | -67 | -29 | mA |
| | | $V_{OUT}$ = 3.135V | -23 | -8 | | |
| Output Low Current | $I_{OL2B}$ | $V_{OUT}$ = 1.95 V | 27 | 56 | | mA |
| | | $V_{OUT}$ =0.4V | | 23 | 30 | |
| Rise Time[1] | $t_{r2B}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 1 | 1.1 | 2 | ns |
| Fall Time[1] | $t_{f2B}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 1 | 1.2 | 2 | ns |
| Duty Cycle[1] | $d_{t2B}$ | $V_T$ = 1.5 V | 45 | 51 | 55 | % |
| Jitter, Cycle-to-cycle[1] | $t_{jcyc-cyc2B}$ | $V_T$ = 1.5 V | | 340 | 400 | ps |

[1]Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - 48MHz

$T_A$ = 0 - 70°C; $V_{DD}$ = 3.3 V +/-5%; $C_L$ = 10 - 20 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Frequency Accuracy | $F_{ACC}$ | REF Out = 14.31818MHz | -50 | 0 | 50 | ppm |
| Output High Voltage | $V_{OH2B}$ | $I_{OH}$ = -20 mA | 2.4 | 2.9 | | V |
| Output Low Voltage | $V_{OL2B}$ | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | V |
| Output High Current | $I_{OH2B}$ | $V_{OUT}$ = 1 V | | -67 | -29 | mA |
| | | $V_{OUT}$ = 3.135V | -23 | -8 | | |
| Output Low Current | $I_{OL2B}$ | $V_{OUT}$ = 1.95 V | 27 | 56 | | mA |
| | | $V_{OUT}$ =0.4V | | 23 | 30 | |
| Rise Time[1] | $t_{r2B}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 1 | 1.1 | 2 | ns |
| Fall Time[1] | $t_{f2B}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 1 | 1.5 | 2 | ns |
| Duty Cycle[1] | $d_{t2B}$ | $V_T$ = 1.5 V | 45 | 52 | 55 | % |
| Jitter, Cycle-to-cycle[1] | $t_{jcyc-cyc2B}$ | $V_T$ = 1.5 V | | 200 | 350 | ps |

[1]Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - REF

$T_A$ = 0 - 70°C; $V_{DD}$ = 3.3 V +/-5%; $C_L$ = 10 - 30 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Frequency Accuracy | $F_{ACC}$ | REF Out = 14.31818MHz | -50 | 0 | 50 | ppm |
| Output High Voltage | $V_{OH2B}$ | $I_{OH}$ = -20 mA | 2.4 | 2.9 | | V |
| Output Low Voltage | $V_{OL2B}$ | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | V |
| Output High Current | $I_{OH2B}$ | $V_{OUT}$ = 1 V | | -67 | -29 | mA |
| | | $V_{OUT}$ = 3.135V | -23 | -8 | | |
| Output Low Current | $I_{OL2B}$ | $V_{OUT}$ = 1.95 V | 27 | 56 | | mA |
| | | $V_{OUT}$ =0.4V | | 23 | 30 | |
| Rise Time[1] | $t_{r2B}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 1 | 1.3 | 2 | ns |
| Fall Time[1] | $t_{f2B}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 1 | 1.7 | 2 | ns |
| Duty Cycle[1] | $d_{t2B}$ | $V_T$ = 1.5 V | 45 | 53 | 55 | % |
| Jitter, Cycle-to-cycle[1] | $t_{jcyc-cyc2B}$ | $V_T$ = 1.5 V | | 270 | 500 | ps |

[1]Guaranteed by design, not 100% tested in production.

## General SMBus serial interface information for the ICS952302

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1*** (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X***
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

**Index Block Write Operation**

| Controller (Host) | | | ICS (Slave/Receiver) |
|---|---|---|---|
| T | starT bit | | |
| Slave Address $D2_{(H)}$ | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| | O | | |
| | O | | O |
| | O | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

**Index Block Read Operation**

| Controller (Host) | | | ICS (Slave/Receiver) |
|---|---|---|---|
| T | starT bit | | |
| Slave Address $D2_{(H)}$ | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat starT | | |
| Slave Address $D3_{(H)}$ | | | |
| RD | ReaD | | |
| | | | ACK |
| | | | |
| | | | Data Byte Count = X |
| ACK | | | |
| | | X Byte | Beginning Byte N |
| ACK | | | |
| | | | O |
| | O | | O |
| | O | | O |
| | O | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

## Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

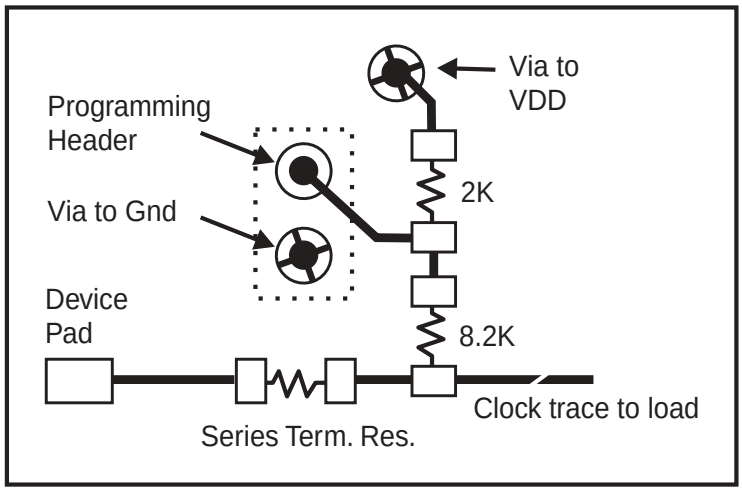
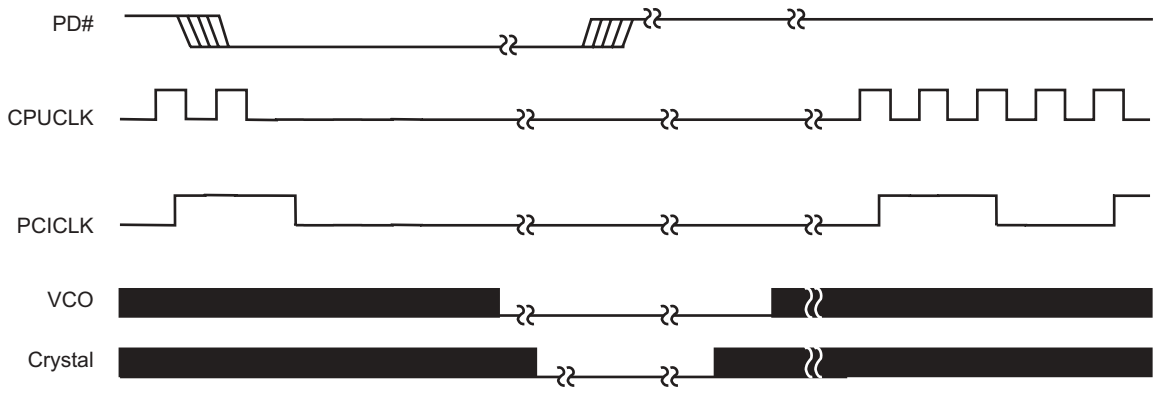



**Fig. 1**

## PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 4 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CLK_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

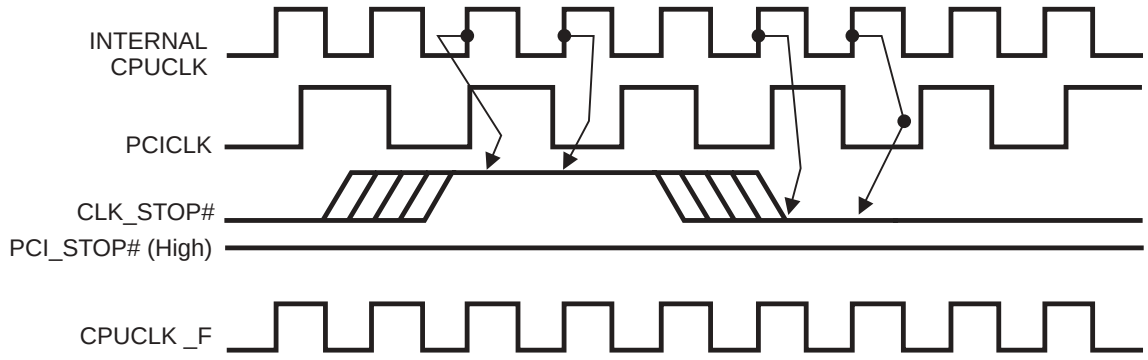



**Notes:**

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS952302 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.

## CLK_STOP# Timing Diagram

CLK_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CLK_STOP# is synchronized by the **ICS952302**. The minimum that the CPU clock is enabled (CLK_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.

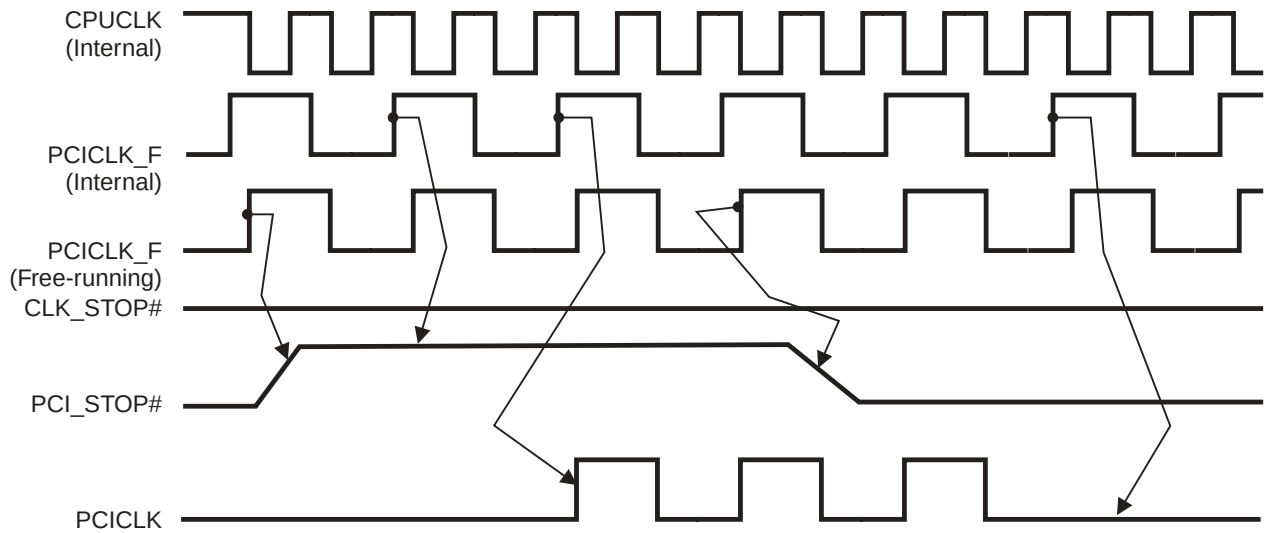



**Notes:**

1. All timing is referenced to the internal CPU clock.
2. CLK_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS952302.
3. CLK_STOP# signal.
4. All other clocks continue to run undisturbed.

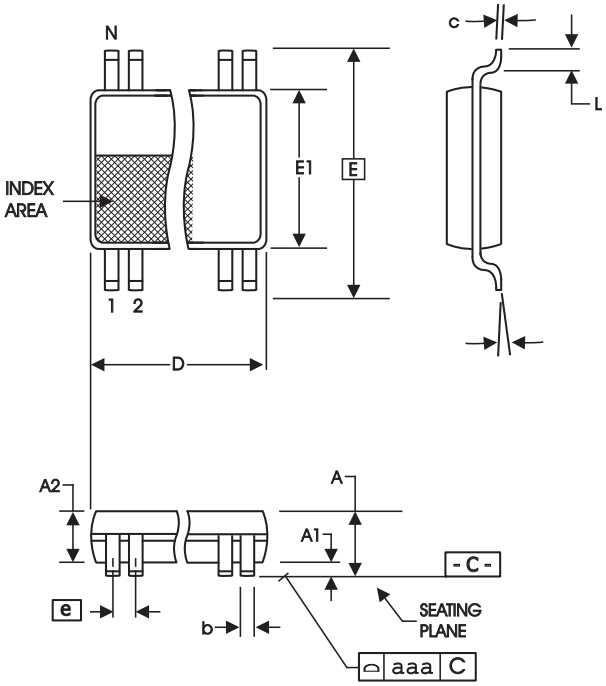
## PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS952302**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS952302** internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only three rising PCICLK clocks, off latency is one PCICLK clock.




**Notes:**

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS952302 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS952302.
3. All other clocks continue to run undisturbed.
4. CLK_STOP# is shown in a high (true) state.




**(240 mil) (0.020 mil)**
**6.10 mm. Body, 0.50 mm. pitch TSSOP**

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.17 | 0.27 | .007 | .011 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 8.10 BASIC | | 0.319 BASIC | |
| E1 | 6.00 | 6.20 | .236 | .244 |
| e | 0.50 BASIC | | 0.020 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 48 | 12.40 | 12.60 | .488 | .496 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

## Ordering Information

**ICS952302yGLF-T**

Example:

**ICS XXXX y G LF- T**

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0957B—10/05/04