Integrated Circuit Systems, Inc.

ICS951702
Advance Information

PIII™ System Clock Chip for DDR SDRAM

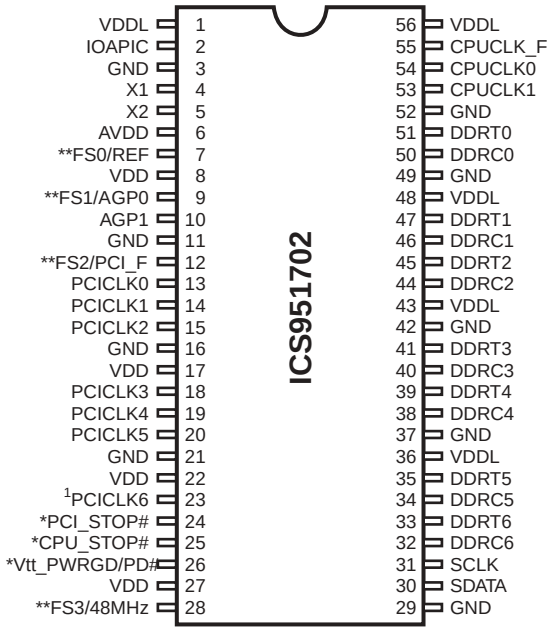
Recommended Application:
1644 and 1644T applications using DDR

Output Features:
- 7 - Differential pairs DDR SDRAM clocks
- 3 - CPU @ 2.5V (1 - Free running)
- 8 - PCI @ 3.3V (1 - Free running and 1 - 2 X optional)
- 2 - AGP @ 3.3V
- 1 - IOAPIC @ 2.5V
- 1 - 48MHz, @3.3V
- 1 - REF @ 3.3V

Features:
- Up to 147MHz frequency support
- Power management through PD#
- Spread spectrum for EMI control (0 to -0.5% down spread, ± 0.25% center spread).
- Uses external 14.318MHz crystal

Skew Specifications:
- CPU - CPU: <250ps
- PCI - PCI: <500ps
- SDRAM - SDRAM: <250ps
- AGP - AGP: <250ps
- PCI - AGP: <750ps
- CPU - SDRAM: <750ps
- CPU - PCI: <3ns

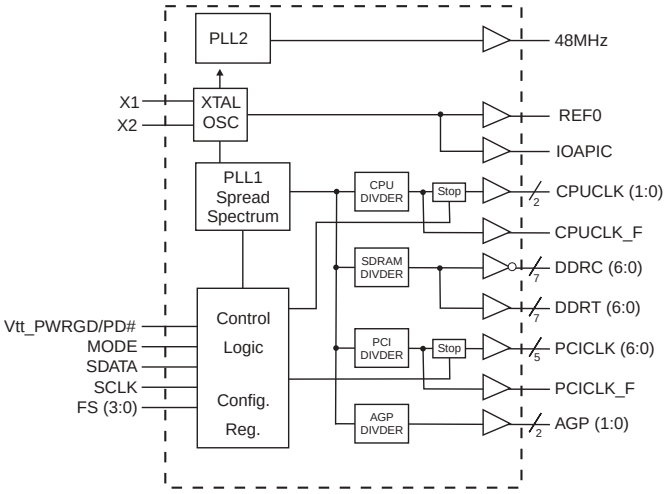
Pin Configuration



56-Pin 240 mil TSSOP

Notes:
* Internal Pull-up Resistor of 120K to VDD
** Internal Pull-down of 120K to GND
1. PCICLK6 is selectable 2X via I^2C

Block Diagram



Functionality

FS3	FS2	FS1	FS0	CPU	SDRAM
0	0	0	0	66.66	66.66
0	0	0	1	66.66	100.00
0	0	1	0	100.00	66.66
0	0	1	1	100.00	100.00
0	1	0	0	100.00	133.33
0	1	0	1	133.33	66.66
0	1	1	0	133.33	100.00
0	1	1	1	133.33	133.33
1	0	0	0	66.66	66.66
1	0	0	1	66.66	100.00
1	0	1	0	100.00	66.66
1	0	1	1	100.00	100.00
1	1	0	0	100.00	133.33
1	1	0	1	133.33	66.66
1	1	1	0	133.33	100.00
1	1	1	1	133.33	133.33

Note:
PCICLK = 33.33MHz
AGP = 66.66MHz

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Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 36, 43, 48, 56	VDDL	PWR	Power supply pins, nominal 2.5V
2	IOAPIC	OUT	2.5V clock outputs
3, 11, 16, 21, 29, 37, 42, 49, 52	GND	PWR	Ground pins
4	X1	IN	Crystal input,nominally 14.318MHz.
5	X2	OUT	Crystal output, nominally 14.318MHz.
6	AVDD	PWR	Analog power supply for 3.3V
7	FS0[2, 3]	IN	Frequency select pin.
	REF0	OUT	14.318 MHz reference clock.
8, 17, 22, 27	VDD	PWR	Power supply pins, nominal 3.3V
9	FS1[2, 3]	IN	Frequency select pin.
	AGP0	OUT	AGP outputs defined as 2X PCI.
10	AGP1	OUT	AGP output defined as 2X PCI.
12	PCICLK_F	OUT	Free running PCI clock
	FS2[1, 2]	IN	Frequency select pin.
20, 19, 18, 15, 14, 13	PCICLK (5:0)	OUT	PCI clock outputs.
23	PCICLK6	OUT	PCI clock output (selectable 1X or 2X via I^2C)
24	PCI_STOP#	IN	Stops all PCICLKs at logic 0 level, when input low besides the PCICLK_F clocks which are controllable by I^2C bits whether they are free running or stopped by PCI_STOP.
25	CPU_STOP#	IN	Stops all CPUCLKs at logic 0 level, when input low. The individual CPU clocks are controllable by I^2C bits whether they are free running or stopped by CPU_STOP.
26	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
	Vtt_PWRGD	IN	This pin acts as a dual function input pin for Vtt_PWRGD and PD# signal. When Vtt_PWRGD goes high the frequency select will be latched at power on thereafter the pin is an asynchronous active low power down pin.
28	FS3[2, 3]	IN	Frequency select pin
	48MHz	OUT	48MHz output clock
30	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
31	SCLK	IN	Clock pin of I^2C circuitry 5V tolerant
33, 35, 39, 41, 45, 47, 51	DDRT (6:0)	OUT	"True" clocks of differential pair DDR SDRAM outputs - 2.5V
32, 34, 38, 40, 44, 46, 50	DDRC (6:0)	OUT	"Complementry" clocks of differential pair DDR SDRAM outputs - 2.5V
53, 54	CPUCLK (1:0)	OUT	2.5V CPU clocks
55	CPUCLK_F	OUT	Free running CPU clock. Not affected by the CPU_STOP#.

Notes:
1: Internal Pull-up Resistor of 120K to 3.3V on indicated inputs
2: Internal pull-down resistor of 120K to GND on indicated inputs.
3: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

General Description

The **ICS951702** is a main clock synthesizer chip for PIII based systems with ALI 1644 style chipset. This provides all clocks required for such a system.
Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS951702** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.
Serial programming I^2C interface allows changing functions, stop clock programming and frequency selection.

Mode Pin - Power Management Input Control

STATE	Pin 24	Pin 25	Pin 26
0	PCI_STOP# (Input)	CPU_STOP# (Input)	PD# (Input)
1	PCICLK4 (Output, Active)	CPUCLKs (Output, Active)	Active

Power Groups

AVDD = PLL Core & Xtal
VDD48 = 48MHz, PLL2
VDDL, VDD = Digital

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description										PWD
		FS3	FS2	FS1	FS0	CPUCLK	SDRAM	PCICLK	AGP	Spread Precentage	
	Bit2	Bit7	Bit6	Bit5	Bit4	(MHz)	(MHz)	(MHz)	(MHz)		
Bit 2, Bit 7:4	0	0	0	0	0	66.66	66.66	33.33	66.66	+/- 0.25% Center Spread	00000 Note1
	0	0	0	0	1	66.66	100.00	33.33	66.66	+/- 0.25% Center Spread	
	0	0	0	1	0	100.00	66.66	33.33	66.66	+/- 0.25% Center Spread	
	0	0	0	1	1	100.00	100.00	33.33	66.66	+/- 0.25% Center Spread	
	0	0	1	0	0	100.00	133.33	33.33	66.66	+/- 0.25% Center Spread	
	0	0	1	0	1	133.33	66.66	33.33	66.66	+/- 0.25% Center Spread	
	0	0	1	1	0	133.33	100.00	33.33	66.66	+/- 0.25% Center Spread	
	0	0	1	1	1	133.33	133.33	33.33	66.66	+/- 0.25% Center Spread	
	0	1	0	0	0	66.66	66.66	33.33	66.66	0 to -0.5% Down Spread	
	0	1	0	0	1	66.66	100.00	33.33	66.66	0 to -0.5% Down Spread	
	0	1	0	1	0	100.00	66.66	33.33	66.66	0 to -0.5% Down Spread	
	0	1	0	1	1	100.00	100.00	33.33	66.66	0 to -0.5% Down Spread	
	0	1	1	0	0	100.00	133.33	33.33	66.66	0 to -0.5% Down Spread	
	0	1	1	0	1	133.33	66.66	33.33	66.66	0 to -0.5% Down Spread	
	0	1	1	1	0	133.33	100.00	33.33	66.66	0 to -0.5% Down Spread	
	0	1	1	1	1	133.33	133.33	33.33	66.66	0 to -0.5% Down Spread	
	1	0	0	0	0	69.99	69.99	35.00	69.99	+/- 0.25% Center Spread	
	1	0	0	0	1	69.99	105.00	35.00	69.99	+/- 0.25% Center Spread	
	1	0	0	1	0	105.00	69.99	35.00	69.99	+/- 0.25% Center Spread	
	1	0	0	1	1	105.00	105.00	35.00	69.99	+/- 0.25% Center Spread	
	1	0	1	0	0	105.00	140.00	35.00	69.99	+/- 0.25% Center Spread	
	1	0	1	0	1	140.00	69.99	35.00	69.99	+/- 0.25% Center Spread	
	1	0	1	1	0	140.00	105.00	35.00	69.99	+/- 0.25% Center Spread	
	1	0	1	1	1	140.00	140.00	35.00	69.99	+/- 0.25% Center Spread	
	1	1	0	0	0	73.33	73.33	36.66	73.33	+/- 0.25% Center Spread	
	1	1	0	0	1	73.33	110.00	36.66	73.33	+/- 0.25% Center Spread	
	1	1	0	1	0	110.00	73.33	36.66	73.33	+/- 0.25% Center Spread	
	1	1	0	1	1	110.00	110.00	36.66	73.33	+/- 0.25% Center Spread	
	1	1	1	0	0	110.00	146.66	36.66	73.33	+/- 0.25% Center Spread	
	1	1	1	0	1	146.66	73.33	36.66	73.33	+/- 0.25% Center Spread	
	1	1	1	1	0	146.66	110.00	36.66	73.33	+/- 0.25% Center Spread	
	1	1	1	1	1	146.66	146.66	36.66	73.33	+/- 0.25% Center Spread	
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 2, 7:4										0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled										0
Bit 0	0 - Running 1- Tristate all outputs										0

Note1: Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3. The I^2C readback of the power up default indicates the revision ID in bits 2, 7:4 as shown.

Byte 1: Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	FS3#
Bit 6	10	1	AGP1
Bit 5	9	1	AGP0
Bit 4	28	1	48MHz
Bit 3	2	1	IOAPIC
Bit 2	55	1	CPUCLK_F
Bit 1	54	1	CPUCLK0
Bit 0	53	1	CPUCLK1

Byte 2: Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	13	1	PCICLK0
Bit 6	14	1	PCICLK1
Bit 5	15	1	PCICLK2
Bit 4	18	1	PCICLK3
Bit 3	19	1	PCICLK4
Bit 2	51, 50	1	SDRAMT0, SDRAMC0
Bit 1	47, 46	1	SDRAMT1, SDRAMC1
Bit 0	45, 44	1	SDRAMT2, SDRAMC2

Byte 3: Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	FS0#
Bit 6	-	X	FS1#
Bit 5	-	X	FS2#
Bit 4	12	1	PCICLK_F
Bit 3	-	1	Reserved
Bit 2	39, 38	1	SDRAMT3, SDRAMC3
Bit 1	35, 34	1	SDRAMT4, SDRAMC4
Bit 0	33, 32	1	SDRAMT5, SDRAMC5

Byte 4: Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	20	1	PCICLK5
Bit 5	23	1	PCICLK6
Bit 4	23	1	PCICLK6; 1=1X, 0=2X
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	33, 32	1	SDRAMT6, SDRAMC6

Byte 5: Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Byte 6: Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	Reserved
Bit 6	-	0	Reserved
Bit 5	-	0	Reserved
Bit 4	-	0	Reserved
Bit 3	-	0	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Note: Don't write into this register, writing into this register can cause malfunction

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage $V_{DD = 3.3V,}$ V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}			5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			mA
Operating Supply Current	$I_{DD3.3OP66}$	C_L = 0 pF; Select @ 66MHz			77	mA
	$I_{DD3.3OP100}$	C_L = 0 pF; Select @ 100MHz			100	
Input frequency	F_i	V_{DD} = 3.3 V;	12		16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms

[1]Guaranteed by design, not 100% tested in production.

TARGET SPECIFICATION SUBJECT TO CHANGE WITH FULL PRODUCT CHARACTERIZATION

Electrical Characteristics - CPUCLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA			0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V			-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19			mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V			1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V			1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45		55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V			250	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc2B}$[1]	V_T = 1.25 V			250	ps
Jitter, One Sigma	t_{j1s2B}[1]	V_T = 1.25 V			150	ps

[1]Guaranteed by design, not 100% tested in production.

TARGET SPECIFICATION SUBJECT TO CHANGE WITH FULL PRODUCT CHARACTERIZATION

Electrical Characteristics - PCICLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	25			mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45		55	%
Skew[1]	t_{sk1}	V_T = 1.5 V			500	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc2B}$[1]	V_T = 1.5 V			250	ps
Jitter, One Sigma[1]	t_{j1s1}	V_T = 1.5 V			150	ps
Jitter, Absolute[1]	t_{jabs1}	V_T = 1.5 V	-500		500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAMT & C

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA			0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V			-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19			mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V			1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V			1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	47		53	%
Skew	t_{sk2B}[1]	V_T = 1.25 V			250	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc2B}$[1]	V_T = 1.25 V			250	ps
Jitter, One Sigma	t_{j1s2B}[1]	V_T = 1.25 V			150	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH4B}	I_{OH} = -12 mA	2			V
Output Low Voltage	V_{OL4B}	I_{OL} = 12 mA			0.4	V
Output High Current	I_{OH4B}	V_{OH} = 1.7 V			-19	mA
Output Low Current	I_{OL4B}	V_{OL} = 0.7 V	19			mA
Rise Time[1]	T_{r4B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V			2	ns
Fall Time[1]	T_{f4B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V			2	ns
Duty Cycle[1]	D_{t4B}	V_T = 1.25 V	45		55	%
Jitter, One Sigma[1]	T_{j1s4B}	V_T = 1.25 V			0.5	ns
Jitter, Absolute[1]	T_{jabs4B}	V_T = 1.25 V	-1		1	ns

[1]Guaranteed by design, not 100% tested in production.

TARGET SPECIFICATION SUBJECT TO CHANGE WITH FULL PRODUCT CHARACTERIZATION

Electrical Characteristics - 24MHz, 48MHz, REF

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -16 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			2	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			2	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45		55	%
Jitter, One Sigma[1]	t_{j1s5}	V_T = 1.5 V			0.5	ns
Jitter, Absolute[1]	t_{jabs5}	V_T = 1.5 V	-1		1	ns

[1]Guaranteed by design, not 100% tested in production.

TARGET SPECIFICATION SUBJECT TO CHANGE WITH FULL PRODUCT CHARACTERIZATION

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 6
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Byte 7	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 7***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
	Byte 7
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9248-174 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

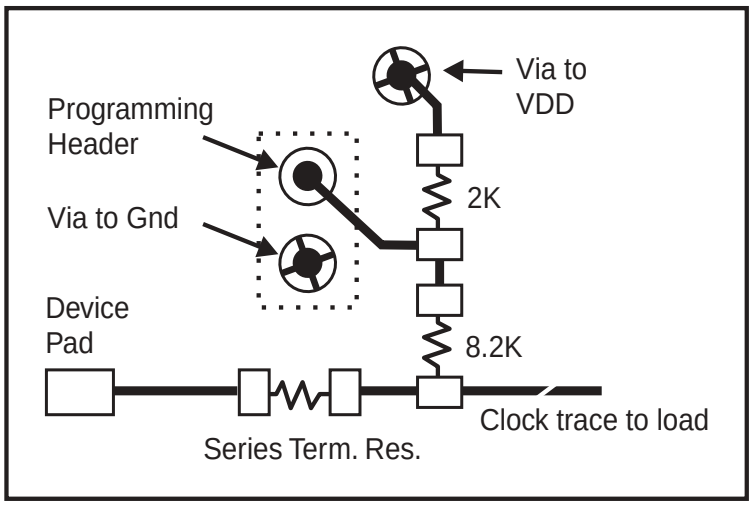
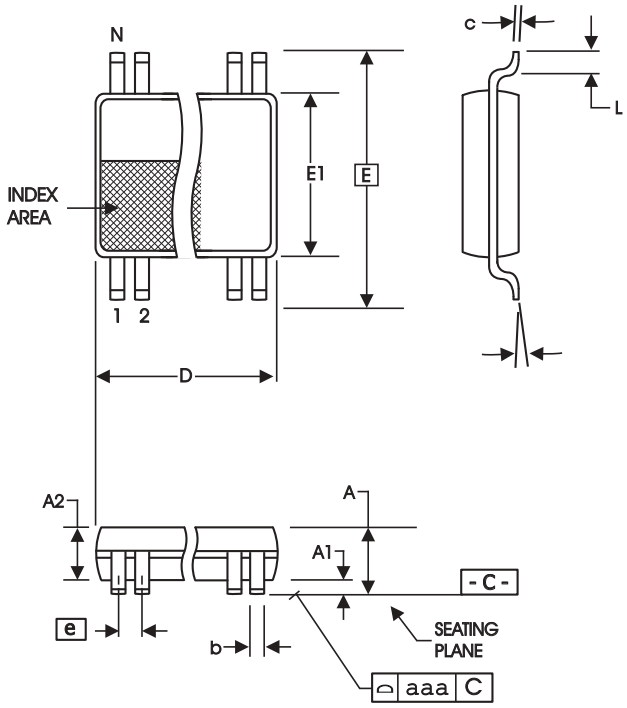


Fig. 1



6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

ICS951702yG-T

Example:

ICS XXXXXX y G - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  G=TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

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