Integrated Circuit Systems, Inc.

ICS93725

DDR and SDRAM Zero Delay Buffer

Recommended Application:

DDR & SDRAM Zero Delay Buffer for SIS 635/640/645/650 & 735/740/746 style chipsets.

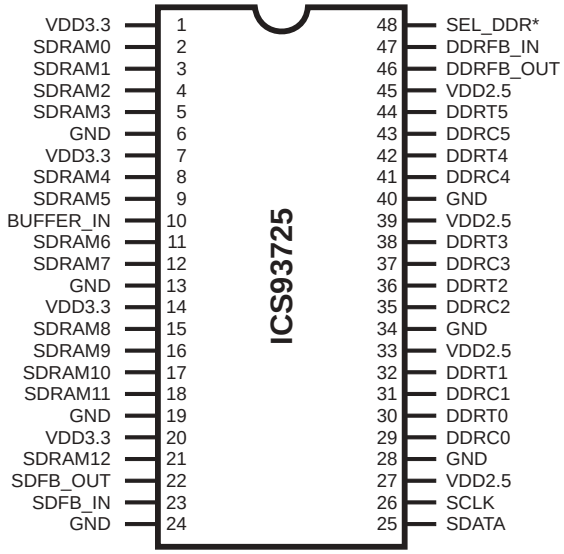
Product Description/Features:

- Low skew, Zero Delay Buffer
- 1 to 13 SDRAM PC133 clock distribution
- 1 to 6 pairs of DDR clock distribution
- I^2C for functional and output control
- Separate feedback path for both memory mode to adjust synchronization.
- Supports up to 2 DDR DIMMs or 3 SDRAM DIMMs
- Frequency support for up to 200MHz
- Individual I^2C clock stop for power mananagement
- CMOS level control signal input

Switching Characteristics:

- OUTPUT - OUTPUT skew: <100ps
- Output Rise and Fall Time for DDR outputs: 550ps - 1150ps
- DUTY CYCLE: 47% - 53%

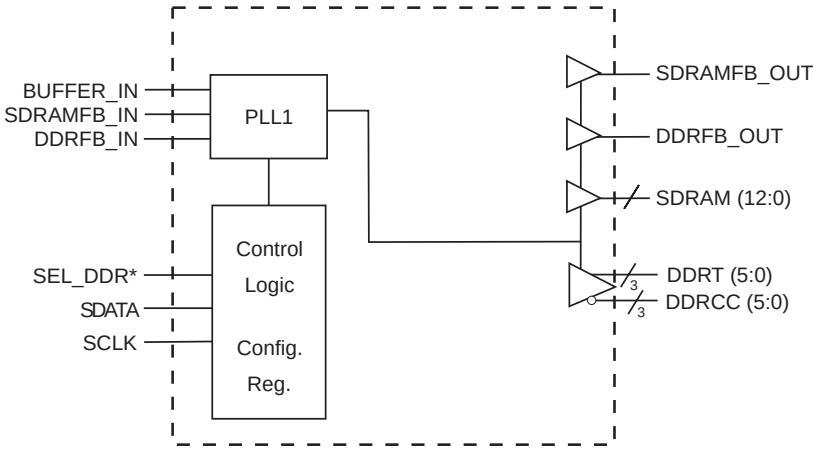
Pin Configuration



48-Pin SSOP

*Internal Pull-up Resistor of 120K to VDD

Block Diagram



Functionality

MODE	PIN 48	VDD 3.3_2.5
DDR Mode	SEL_DDR=1	2.5V
DDR/SD Mode	SEL_DDR=0	3.3V

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 7, 14, 20	VDD3.3	PWR	3.3V voltage supply for SDRAM.
6, 13, 19, 24, 34, 28, 40	GND	PWR	Ground
44, 42, 38, 36, 32, 30	DDRT (5:0)	OUT	"True" Clock of differential pair outputs.
43, 41, 37, 35, 31, 29	DDRC (5:0)	OUT	"Complementory" clocks of differential pair outputs.
21, 18, 17, 16, 15, 12, 11, 9, 8, 5, 4, 3, 2	SDRAM (12:0)	OUT	SDRAM clock outputs
27, 39, 45	VDD2.5	PWR	2.5V voltage supply for DDR.
10	BUFFER_IN	IN	Single ended buffer input
22	SDRAMFB_OUT	OUT	Feedback output for SDRAM
23	SDFB_IN	IN	Feedback input for SDRAM
25	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
26	SCLK	IN	Clock input of I^2C input, 5V tolerant input
46	DDRFB_OUT	OUT	Feedback output for DDR
47	DDRFB_IN	IN	Feedback input for DDR
48	SEL_DDR	IN	Select input for DDR mode or DDR/SD mode 0=SD mode 1=DDR mode

Byte 6: Output Control
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	48	-	SEL_DDR (Read back only)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	44, 43	1	DDRT5, DDRC5
Bit 3	42, 41	1	DDRT4, DDRC4
Bit 2	38, 37	1	DDRT3, DDRC3
Bit 1	36, 35	1	DDRT2, DDRC2
Bit 0	32, 31	1	DDRT1, DDRC1

Byte 7: Output Control
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	30, 29	1	DDRT0, DDRC0
Bit 6	21	1	SDRAM12
Bit 5	17, 18	1	SDRAM10 SDRAM11
Bit 4	15, 16	1	SDRAM8 SDRAM9
Bit 3	11, 12	1	SDRAM6 SDRAM7
Bit 2	8, 9	1	SDRAM4 SDRAM5
Bit 1	4, 5	1	SDRAM2 SDRAM3
Bit 0	2, 3	1	SDRAM1 SDRAM0

Absolute Maximum Ratings

Supply Voltage (VDD & VDD2.5) . . . . . -0.5V to 3.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +85°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

SEL_DDR=0 SDRAM Outputs V_{DD}=3.3V, T_A=0 - 85°C; (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD3.3}$	100MHz, RL=0Ω, CL = 0pF		130		
		133MHz, RL=0Ω, CL = 0pF		173		mA
		200MHz, RL=0Ω, CL = 0pF		247		mA
Output High Current	I_{OH}	V_{DD}=3.3V, V_{OUT}=1V		-40	-18	mA
Output Low Current	I_{OL}	V_{DD}=3.3V, V_{OUT}=1.2V	26	34		mA
High-level output voltage	V_{OH}	V_{DD}=3.3V I_{OH} = -12 mA	1.7	2		V
Low-level output voltage	V_{OL}	V_{DD}=3.3V I_{OH} = 12 mA		0.4	0.6	V
Input Capacitance[1]	C_{IN}	V_I = GND or V_{DD}		2		pF

[1]Guaranteed by design, not 100% tested in production.

Recommended Operating Condition

SEL_DDR=0 SDRAM Outputs V_{DD}=3.3V, T_A=0 - 85°C; (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	$V_{DD3.3}$		3	3.3	3.6	V
Input High Voltage	V_{IH}	SEL_DDR, PD# input	2			V
Input Low Voltae	V_{IL}	SEL_DDR, PD# input			0.8	V
Input Voltage Level	V_{IN}		0	3.3	3.6	V

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

SEL_DDR=1 DDR Outputs V_{DD}=2.5V, T_A=0 - 85°C; (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5}$	100MHz, RL=0Ω, CL = 0pF		141		mA
		133MHz, RL=0Ω, CL = 0pF		188		mA
		200MHz, RL=0Ω, CL = 0pF		271		mA
Output High Current	I_{OH}	V_{DD}=2.5V, V_{OUT}=1V		-43	-18	mA
Output Low Current	I_{OL}	V_{DD}=2.5V, V_{OUT}=1.2V	26	38		mA
High-level output voltage	V_{OH}	V_{DD}=2.5V I_{OH} = -12 mA	1.7	2		V
Low-level output voltage	V_{OL}	V_{DD}=2.5V I_{OH} = 12 mA		0.4	0.6	V
Output differential-pair Crossing voltage	V_{OC}	V_{DD} = 2.5V 100/133/166/ 200 Mhz	1.05	1.25	1.45	V
Input Capacitance[1]	C_{IN}	V_I = GND or V_{DD}	2			pF

[1]Guaranteed by design, not 100% tested in production.

Recommended Operating Condition

SEL_DDR=1 DDR Outputs V_{DD}=2.5V, T_A=0 - 85°C; (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	$V_{DD2.5}$		2.3	2.5	2.7	V
Input High Voltage	V_{IH}	SEL_DDR, PD# input	2			V
Input Low Voltage	V_{IL}	SEL_DDR, PD# input			0.8	V
Input Voltage Level	V_{IN}		0	2.5	2.7	V

[1]Guaranteed by design, not 100% tested in production.

Switching Characteristics

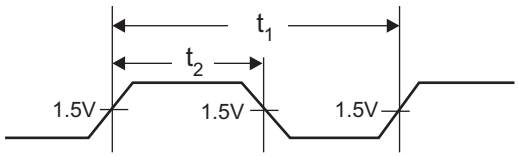
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency			66		200	MHz
Input Clock Duty Cycle	d_{in}		40		60	%
DDR Static Phase Error	tped		-100	-50	100	ps
SDRAM Static Phase Error	tpes		-100	-20	100	ps
DDR output to output Skew	T_{skewd}	Not including FBOUT to outputs		60	100	ps
SDRAM output to output Skew	T_{skews}	Not including FBOUT to outputs		200	300	ps
DDR Duty Cycle	D_C[2]	66MHz to 100MHz	48		52	%
		101MHz to 200MHz	48		53	%
SDRAM Duty Cycle	D_C[2]	66MHz to 100MHz	48		52	%
		101MHz to 200MHz	48		56	%
DDR Rise Time	trd	Measured between	0.55	0.68	0.95	ns
DDR Fall Time	tfd	20% and 80% output, CL=16pF	0.63	0.91	1.15	ns
SDRAM Rise Time	trs	V_{OL} = 0.4V, V_{OH} = 2.4V,	0.5	1.4	1.7	ns
SDRAM Fall Time	tfs	CL=30pF	0.5	1.65	1.8	ns
DDR Cycle to Cycle Jitter	$t_{(C-C)D}$	SEL_DDR=1,V_{DD}=2.5V , CL=16pF	23		38	ps
SDRAM Cycle to Cycle Jitter	$t_{(C-C)S}$	SEL_DDR=0,V_{DD}=3.3V , CL=30pF	36		57	ps

[1]Guaranteed by design, not 100% tested in production.

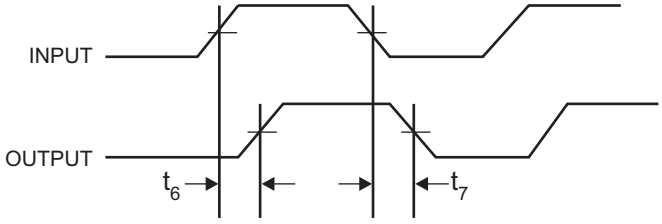
[2] While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle=t_2/t_1, where the cycle (t_1) decreases as the frequency goes up.

Switching Waveforms

Duty Cycle Timing



SDRAM Buffer LH and HL Propagation Delay



General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D4 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 6
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D4_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Byte 7	
	ACK
Stop Bit	

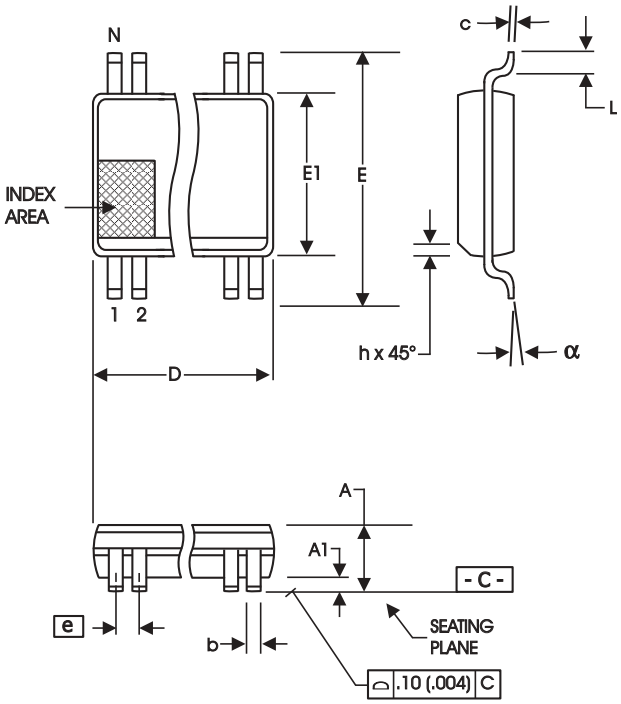
How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D5 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 7***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D5_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
	Byte 7
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS93725yFT

Example:

ICS XXXX y **F - T**

- **Designation for tape and reel packaging**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0606A—08/01/03