Integrated Circuit Systems, Inc.

ICS9248-110

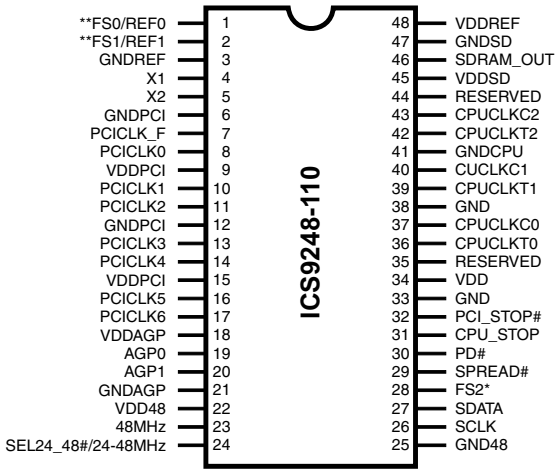
AMD-K7™ System Clock Chip

Recommended Application:
AMD-K7 based systems
Output Features:
- 3 differential pair open drain CPU clocks (2.7V external pull-up; up to 150MHz achieviable through I^2C)
- 2 - AGPCLK @ 3.3V
- 8 - PCI @3.3V, including 1 free running
- 1 - 48MHz @ 3.3V
- 1 - 24/48MHz @ 3.3V
- 2- REF @3.3V, 14.318MHz.

Features:
- Up to 150MHz frequency support
- Support power management: CPU, PCI, stop and Power down Mode from I^2C programming.
- Spread spectrum for EMI control -0.5% down spread
- Uses external 14.318MHz crystal
- FS pins for frequency select

Key Specifications:
- CPU – CPU: <250ps
- AGP-AGP: <250ps
- PCI – PCI: <400ps
- CPU - SDRAM_OUT: <400ps
- CPU-AGP <250ps

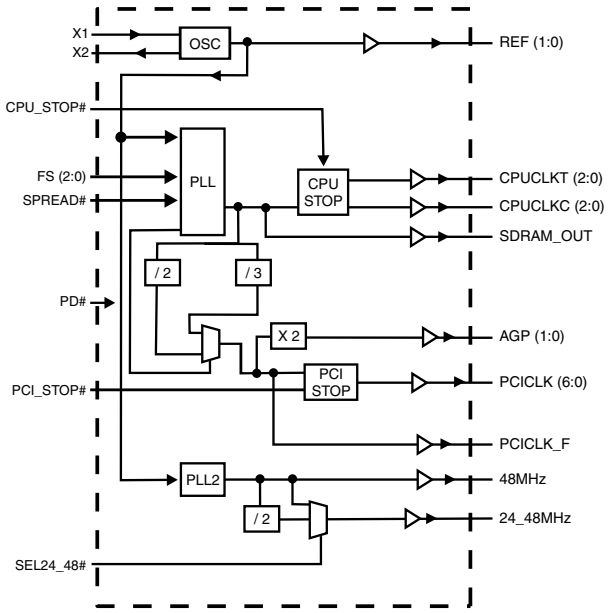
Pin Configuration



48-Pin 300mil SSOP

* Internal 120K pullup resistor on indicated inputs
** Internal 240K pullup resistor on indicated inputs

Block Diagram



Functionality

FS2	FS1	FS0	CPU, SDRAM	PCI	AGP
0	0	0	90	30.00	60.00
0	0	1	95	31.67	63.33
0	1	0	100.99	33.66	67.33
0	1	1	115	38.33	76.67
1	0	0	100.7	33.57	67.13
1	0	1	103	34.33	68.67
1	1	0	105	35.00	70.00
1	1	1	110	36.67	73.33

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ICS reserves the right to make changes in the device data identified in this publication without further notice. ICS advises its customers to obtain the latest version of all device data to verify that any information being relied upon by the customer is current and accurate.

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2, 1	FS (1:0)	IN	Frequency Select pins, has pull-up to VDD
	REF (1:0)	OUT	14.318MHz clock output
3	GNDREF	PWR	Ground for REF outputs
4	X1	IN	XTAL_IN 14.318MHz Crystal input, has internal 33pF load cap and feed back resistor from X2
5	X2	OUT	XTAL_OUT Crystal output, has internal load cap 33pF
6, 12	GNDPCI	PWR	Ground for PCI outputs
7	PCICLK_F	OUT	Free Running PCI output. Not affected by the PCI_STOP# input.
17, 16, 14, 13, 11, 10, 8	PCICLK (6:0)	OUT	PCI clock outputs. TTL compatible 3.3V
9, 15	VDDPCI	PWR	Power for PCICLK outputs, nominally 3.3V
18	VDDAGP	PWR	Power for AGP outputs, nominally 3.3V
20, 19	AGP (1:0)	OUT	AGP outputs defined as 2X PCI. These may not be stopped.
21	GNDAGP	PWR	Ground for AGP clock outputs
34	VDD	PWR	Isolated power for core, nominally 3.3V
33	GND	PWR	Isolated ground for core
22	VDD48	PWR	Power for USB, FDC outputs nominally 3.3V
23	48MHz	OUT	48MHz output
24	SEL24-48#	IN	Selects 24 or 48MHz output for pin 24 Low = 48MHz High = 24MHz
	24-48MHz	OUT	Fixed clock out selectable through SEL24-48#
25	GND48	PWR	Ground for 48MHz outputs
26	SCLK	IN	Clock input for I^2C
27	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
28	FS2	IN	Frequency Select pin, has pull-up to VDD
29	SPREAD#	IN	Enables Spread Spectrum feature when LOW. Down Spread 0.5% modulation frequency =50KHz
30	PD#	IN	Powers down chip, active low. Internal PLL & all outputs are disabled.
31	CPU_STOP#	IN	Halts CPUCLKs. CPUCLKTs driven LOW wheras CPUCLKC is driven HIGH when this pin is asserted (Active LOW).
32	PCI_STOP#	IN	Halts PCI Bus at logic "0" level when driven low. PCICLK_F is not affected by this pin
46	SDRAM_OUT	OUT	Reference clock for SDRAM zero delay buffer
34	VDD	PWR	Isolated power for core
35, 44	RESERVED	N/C	Furture CPU power rail
42, 39, 36	CPUCLKT (2:0)	OUT	"True" clocks of differential pair CPU outputs. These open drain outputs need an external 1.5V pull-up.
43, 40, 37	CPUCLKC (2:0)	OUT	"Complementory" clocks of differental pair CPU output. These open drain outputs need an external 1.5V pull_up.
38, 41	GNDCPU	PWR	Ground for CPUCLK outputs.
45	VDDSD	PWR	Power for SDRAM_OUT pin. Nominally 3.3V
47	GNDSD	PWR	Ground for SDRAM_OUT pins
48	VDDREF	PWR	Power for REF, X1, X2, nominally 3.3V

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General Description

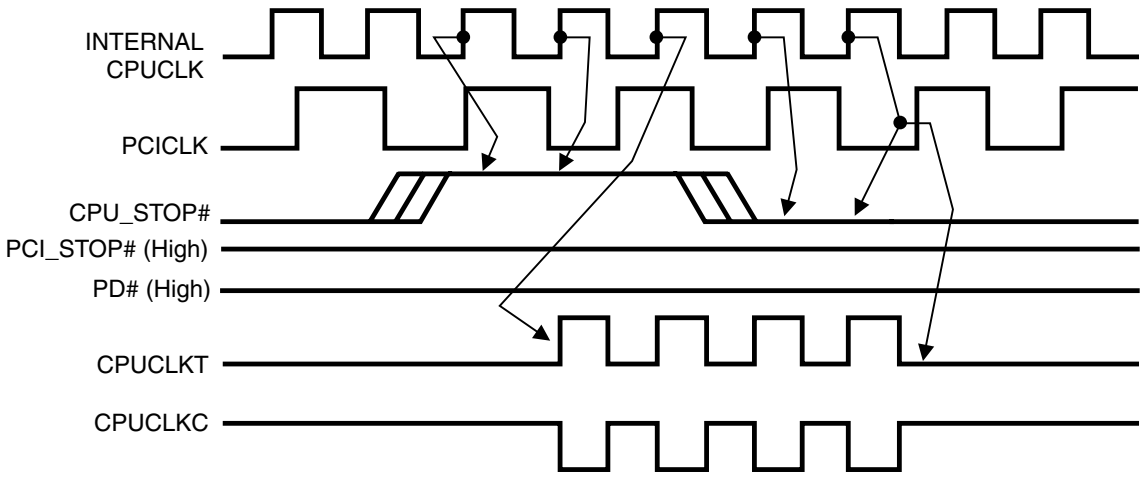
The **ICS9248-110** is a main clock synthesizer chip for AMD-K7 based systems. This provides all clocks required for such a system when used with a Zero Delay Buffer Chip such as the ICS9179-06.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9248-110 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I^2C interface allows changing functions, stop clock programming and frequency selection.

CPU_STOP# Timing Diagram

CPU_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the **ICS9248-110**. All other clocks will continue to run while the CPUCLKs clocks are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.

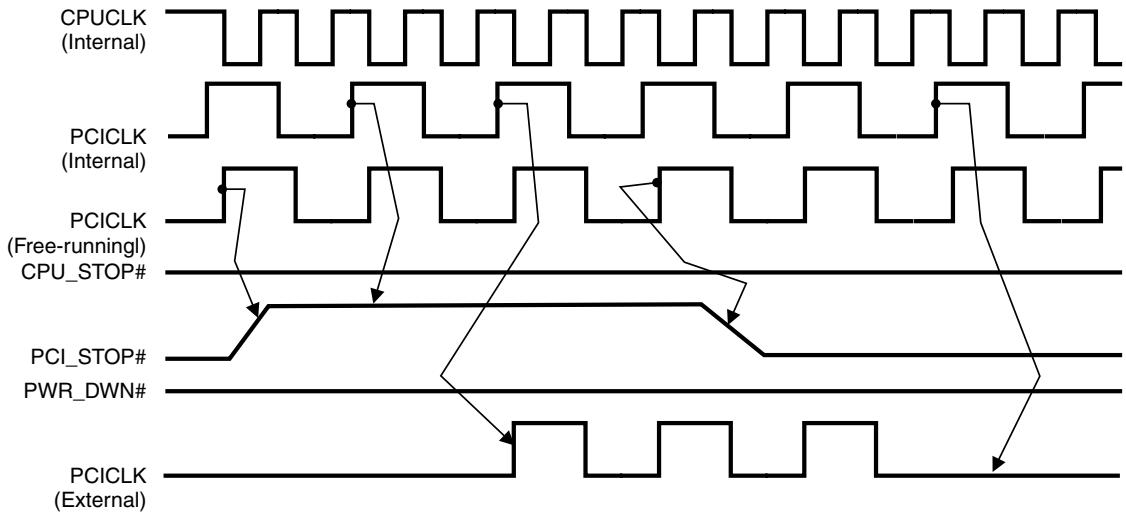


Notes:
1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS9248-110**.
3. All other clocks continue to run undisturbed.
4. PD# and PCI_STOP# are shown in a high (true) state.

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PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9248-110**. It is used to turn off the PCICLK (0:5) clocks for low power operation. PCI_STOP# is synchronized by the **ICS9248-110** internally. PCICLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:5) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:

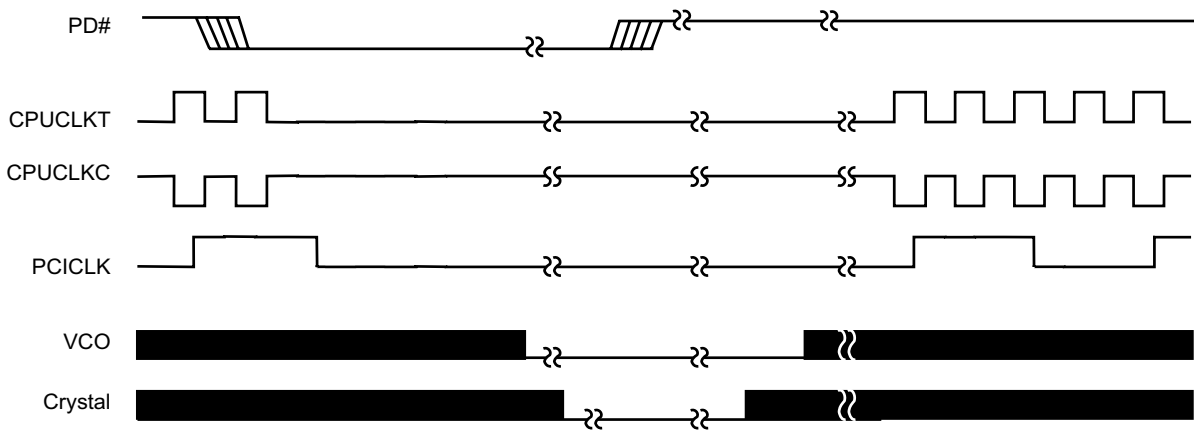
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248.
3. All other clocks continue to run undisturbed.
4. PD# and CPU_STOP# are shown in a high (true) state.

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PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CPU_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248-110 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

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Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9248-110 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

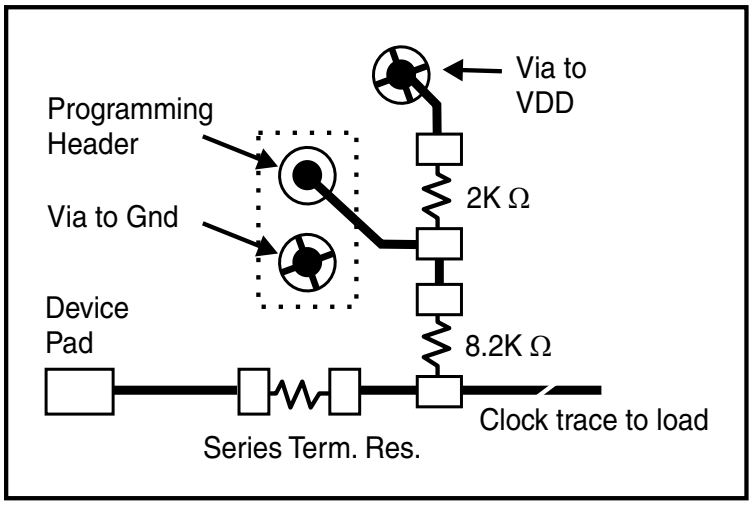


Fig. 1

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General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 6
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 6***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

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I²C Command Bitmaps

Byte 6: SDRAM Clock & Generator Mode Control Register

Bit	Description								PWD
7	Spread Spectrum enable (+/- 0.25% center spread) 1=ON 0=OFF								0
3,2, 6:4	Bit 3	Bit 2	FS2 Bit 6	FS1 Bit 5	FS0 Bit 4	CPU, SDRAM	PCI	AGP	Reserved Note1
	0	0	0	0	0	90	30.00	60.00	
	0	0	0	0	1	95	31.67	63.33	
	0	0	0	1	0	100.99	33.66	67.33	
	0	0	0	1	1	115	38.33	76.67	
	0	0	1	0	0	100.7	33.57	67.13	
	0	0	1	0	1	103	34.33	68.67	
	0	0	1	1	0	105	35.00	70.00	
	0	0	1	1	1	110	36.67	73.33	
	0	1	0	0	0	102	34.00	68.00	
	0	1	0	0	1	104	34.67	69.33	
	0	1	0	1	0	106	35.33	70.67	
	0	1	0	1	1	107	35.67	71.33	
	0	1	1	0	0	108	36.00	72.00	
	0	1	1	0	1	109	36.33	72.67	
	0	1	1	1	0	110	36.67	73.33	
	0	1	1	1	1	111	37.00	74.00	
	1	0	0	0	0	112	37.33	74.67	
	1	0	0	0	1	113	37.67	75.33	
	1	0	0	1	0	114	38.00	76.00	
	1	0	0	1	1	116	38.67	77.33	
	1	0	1	0	0	117	39.00	78.00	
	1	0	1	0	1	118	39.33	78.67	
	1	0	1	1	0	119	39.67	79.33	
	1	0	1	1	1	120	30.00	60.00	
	1	1	0	0	0	121	30.25	60.50	
	1	1	0	0	1	122	30.50	61.00	
	1	1	0	1	0	123	30.75	61.50	
	1	1	0	1	1	124	31.00	62.00	
	1	1	1	0	0	125	31.25	62.50	
	1	1	1	0	1	133.33	33.33	66.67	
	1	1	1	1	0	140	35.00	70.00	
	1	1	1	1	1	150	37.50	75.00	
1	0 - Frequency is selected by hardware select, latched input; Spread controlled by pin 29 1 - Frequency is selected by Bit 6:2; Spread controlled by bit 7								0
0	0 - SDRAM_OUT Disable 1 - SDRAM_OUT Enable								1

Notes:

1. Default at power-up will be latched logic inputs to define frequency, as displayed by Bit 1.
2. PWD = Power-Up Default

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I²C Command Bitmaps

Byte 4: Clock Control Register

Bit	Pin#	Default	Description
7	1	1	REF0 enable
6	23	1	24MHz/48MHz enable
5	22	1	USB0 enable
4	20	1	AGP1 enable
3	19	1	AGP0 enable
2	42, 43	1	CPUCLK2 enable (both of differential pair, True" and "Complimentary"
1	39, 40	1	CPUCLK1 enable (both of differential pair, True" and "Complimentary"
0	36, 37	1	CPUCLK0 enable (both of differential pair, True" and "Complimentary"

Notes: A value of '1'b is enable, '0'b is disable

Byte 5: PCI Clock Control Register

Bit	Pin#	Default	Description
7	2	1	REF1 enable
6	17	1	PCICLK6 enable
5	16	1	PCICLK5 enable
4	14	1	PCICLK4 enable
3	13	1	PCICLK3 enable
2	11	1	PCICLK2 enable
1	10	1	PCICLK1 enable
0	8	1	PCICLK0 enable

Notes: A value of '1'b is enable, '0'b is disable

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Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			5	uA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA
Operating Supply Current	$I_{DD3.3OP}$	C_L =20 pF; Select @ 66 MHz		87	160	mA
		C_L =20 pF; Select @ 100 MHz		116	160	
		C_L = 20 pF; Select @ 133 MHz		127	160	mA
Power Down	PD				600	uA
Input frequency	F_i	V_{DD} = 3.3 V	12	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew[1]	$T_{CPU-SDRAM}$	Vt=50% CPU - 1.5V SDRAM; CPU Leads		120	400	ps
	$T_{CPU-PCI}$	Vt=50% CPU - 1.5V PCI; CPU Leads		160	550	ps
	$T_{CPU-AGP}$	Vt =50% CPU - 1.5V AGP; CPU Leads		65	250	ps

[1]Guaranteed by design, not 100% tested in production.

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Electrical Characteristics - USB, REF

T_A = 0 - 70C; V_{DD} = 3.3V +/-5%; C_L = 20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O=V_{DD}*(0.5)$	20	47	60	Ω
Output Impedance	R_{DSN2B}[1]	$V_O=V_{DD}*(0.5)$	20	44	60	Ω
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		2.6	4.0	ns
Fall Time[1]	t_{f5}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		2.5	4.0	ns
Duty Cycle[1]	d_{t5}[1]	V_T = 1.5 V	45	51	55	%
REF Jitter, Cyl-to-Cyl	$t_{jcyc-cyc5}$[1]	V_T = 1.5 V		320	700	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK (Open Drain)

T_A = 0 - 70C; V_{DD}=3.3V +/- 5%; C_L = 20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	Z_O[1]	$V_O=V_X$			60	Ω
Output High Voltage	V_{OH2B}	Termination to Vpull-up(external)	1		1.8	V
Output Low Voltage	V_{OL2B}	Termination to Vpull-up(external)			0.8	V
Output Low Current	I_{OL2B}	V_{OL} = 0.3 V	18			mA
Rise Time[1]	t_{r2B}[1]	V_{OL} = 20% , V_{OH} = 80%		2.4	2.6	ns
Fall Time[1]	t_{f2B}[1]	V_{OH} = 80%, V_{OL} = 20%		1.2	2.6	ns
Differential voltage-AC[1]	V_{DIF}	Note 2	0.4		Vpull-up(ext)	V
Differential voltage-DC[1]	V_{DIF}	Note 2	0.2		Vpull-up(ext)	V
Diff Crossover Voltage[1]	V_X	Note 3	1.1	1.4	1.7	V
Duty Cycle[1]	d_{t2B}[1]	V_T = 50%	44	46	54	%
Skew window[1]	t_{sk2B}[1]	V_T = 50%		40	200	ps
Jitter, Cycle-to-cycle1	tjcyc-cyc_{2B}[1]	$V_T = V_X$		80	250	ps
Jitter, Absolute1	tjabs$_{2B}$[1]	V_T = 50%		120	250	ps

Notes:

1 - Guaranteed by design, not 100% tested in production.

2 - V_{DIF} specifies the minimum input differential voltages (V_{TR}-V_{CP}) required for switching, where V_{TR} is the "true" input Level and V_{CP} is the "complement" input level.

3 - Vpull-up(external) = 2.7V, Min=Vpull-up(external)/2-150mV; Max=Vpull-up(external)/2 +150mV

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Electrical Characteristics - PCICLK

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3V +/-5%; C_L = 30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	V_O=V_{DD}*(0.5)	12	24	55	Ω
Output Impedance	R_{DSN2B}[1]	V_O=V_{DD}*(0.5)	12	23	55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.6			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-16	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	19			mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.65	2.5	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.60	2.5	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	50	55	%
Skew window[1]	t_{sk1}	V_T = 1.5 V		300	400	ps
Jitter, Cyc-to-Cyc	$t_{jcyc-cyc1}$	V_T = 1.5 V		70	200	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK_F

T_A = 0 - 70C; V_{DD} = 3.3V +/-5%; C_L = 20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	V_O=V_{DD}*(0.5)	12	24	55	Ω
Output Impedance	R_{DSN2B}[1]	V_O=V_{DD}*(0.5)	12	23	55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.6			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-12	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	12			mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.4	2.0	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.3	2.0	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	51	55	%
Skew window[1]	t_{sk1}	V_T = 1.5 V		300	400	ps
Jitter, Cyc-to-Cyc	$t_{jcyc-cyc1}$	V_T = 1.5 V		70	200	ps

[1]Guaranteed by design, not 100% tested in production.

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Electrical Characteristics - AGP

T_A = 0 - 70C; V_{DD}=3.3V +/-5%; C_L = 20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP4B}[1]	$V_O=V_{DD}*(0.5)$	12		55	Ω
Output Impedance	R_{DSN4B}[1]	$V_O=V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH4B}	I_{OH} = -18 mA	2			V
Output Low Voltage	V_{OL4B}	I_{OL} = 18 mA			0.4	V
Output High Current	I_{OH4B}	V_{OH} = 2.0 V			-19	mA
Output Low Current	I_{OL4B}	V_{OL} = 0.8 V	19			mA
Rise Time[1]	t_{r4B}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1	2	ns
Fall Time[1]	t_{f4B}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1	2	ns
Duty Cycle[1]	d_{t4B}	V_T = 1.5 V	45	50	55	%
Skew window1	tsk[1]	V_T = 1.5 V		50	200	ps
Jitter Cyc-Cyc	tjcyc-cyc[1]	V_T = 1.5 V		288	450	ps

[1]Guaranteed by design, not 100% tested in production.

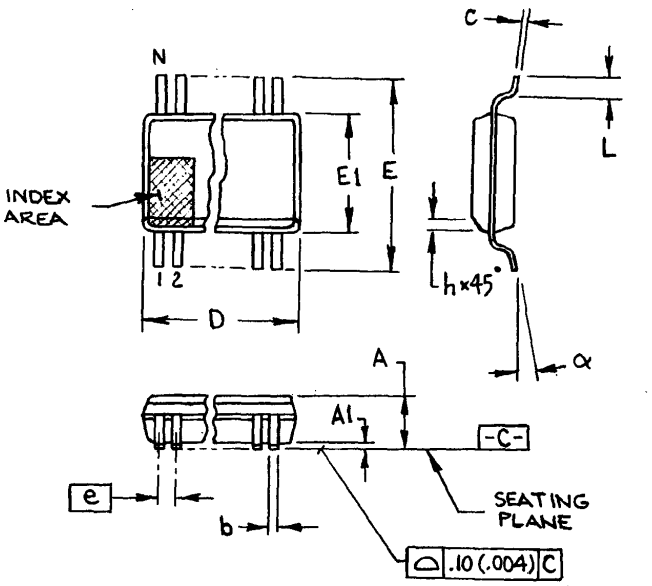
Electrical Characteristics - SDRAM_OUT

T_A = 0 - 70C; V_{DD}=3.3V +/-5%; C_L = 30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP}[1]	$V_O=V_{DD}*(0.5)$	12		55	Ω
Output Impedance	R_{DSN}[1]	$V_O=V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH3}	I_{OH} = -11 mA	2			V
Output Low Voltage	V_{OL3}	I_{OL} = 11 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-12	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8 V	12			mA
SD (0:1,3:12) Rise Time[1]	t_{r3}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1	2	ns
SD(0:1,3:12) Fall Time[1]	t_{f3}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1	2	ns
SD(0:1,3:12) Duty Cycle[1]	d_{t3}[1]	V_T = 1.5 V	45	50	55	%
Skew window[1]	t_{sk}[1]	V_T = 1.5 V		70	150	ps

[1]Guaranteed by design, not 100% tested in production.

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300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.748	16.002	.620	.630

JEDEC MO-118 6/1/00
DOC# 10-0034 REV B

Ordering Information

ICS9248yF-110

Example:

ICS XXXX y F - PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
F=SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device

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ICS reserves the right to make changes in the device data identified in this publication without further notice. ICS advises its customers to obtain the latest version of all device data to verify that any information being relied upon by the customer is current and accurate.