Integrated Circuit Systems, Inc.

ICS9147-03

Frequency Generator & Integrated Buffers for 686 Series CPUs

General Description

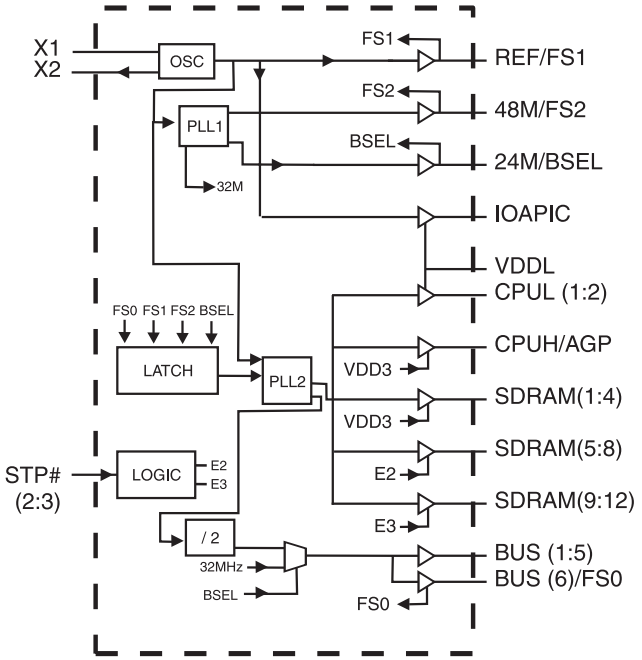
The **ICS9147-03** generates all clocks required for high speed RISC or CISC microprocessor systems such as Intel PentiumPro, AMD or Cyrix processors. Four bidirectional I/O pins (FS0, FS1, FS2, BSEL) are latched at power-on to the functionality table. The Six BUS clocks can be selected as either synchronous at 1/2 CPU speed or asynchronous at 32MHz selected by BSEL latched input.The inputs provide for tristate and test mode conditions to aid in system level testing.These multiplying factors can be customized for specific applications. Glitch-free stop clock controls provided for SDRAM(5:8) and SDRAM (9:12) banks (STP2#, STP3#).

High drive BUS and SDRAM outputs typically provide greater than 1 V/ns slew rate into 30 pF loads. CPU outputs typically provide better than 1V/ns slew rate into 20pF loads while maintaining 50±5% duty cycle. The REF clock outputs typically provide better than 0.5V/ns slew rates. Seperate buffer supply pin VDDL allows for nominal 3.3V voltage or reduced voltage swing (from 2.9 to 2.5V) for CPUL (1:2) and IOAPIC outputs.

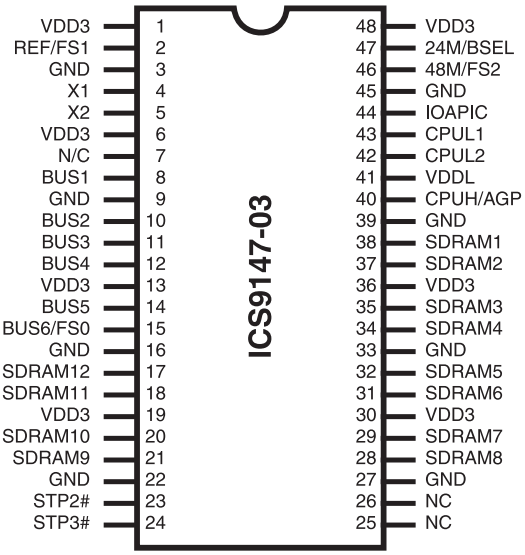
Features

- Total of 15 CPU speed clocks:
  - Two copies of CPU clock with VDDL (2.5 to 3.3V)
  - Twelve (12) SDRAM (3.3v) plus one CPUH/AGP (3.3V) clocks
- Six copies of BUS clocks (synchronous with CPU clock/2 or asynchronous 32 MHz)
- 250ps output skew window for CPU andSDRAM clocks and 500ps window BUS clocks. CPU clocks to BUS clocks skew 1-4ns (CPU early)
- Two copies of Ref. clock @14.31818 MHz (One driven by VDDL as IOAPIC)
- One 48 MHz (3.3 V TTL) for USB support and single 24 MHz.
- Separate VDDL for CPUL (1:2) clock buffers and IOAPIC to allow 2.5V output (or Std. Vdd)
- 3.0V – 3.7V supply range w/2.5V compatible outputs
- 48-pin SSOP package

Block Diagram



Pin Configuration



48-Pin SSOP

Pentium is a trademark of Intel Corporation

ICS reserves the right to make changes in the device data identified in this publication without further notice. ICS advises its customers to obtain the latest version of all device data to verify that any information being relied upon by the customer is current and accurate.

Functionality with (14.31818 MHz input)

Address Select			CPUL (1:2) CPUH SDRAM (1:12)	BUS (1:6) (MHz)		24M (MHz)	48M (MHz)
FS2	FS1	FS0	(MHz)	BSEL=1	BSEL=0	(MHz)	(MHz)
0	0	0	60	30	32	24	48
0	0	1	66.8	33.4	32	24	48
0	1	0	50	25	32	24	48
0	1	1	55	27.5	32	24	48
1	0	0	75	37.5	32	24	48
1	0	1	68.5	34.3	32	24	48
1	1	0	Test/2**	Test/4**	Test/3**	Test/4**	Test/2**
1	1	1	Tristate	Tristate	Tristate	Tristate	Tristate

**Test: is the frequency applied to the X1 input. Can be crystal or tester generated clock overriding crystal at X1 pin.

SDRAM Clock Enable

STP2#	STP3#	DIMM BANK1 SDRAM (1:4)	DIMM BANK2 SDRAM (5:8)	DIMM BANK3 SDRAM (9:12)
0	0	ON	Stopped Low	Stopped Low
0	1	ON	Stopped Low	ON
1	0	ON	ON	Stopped Low
1	1	ON	ON	ON

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2	REF	OUT	Reference clock output*
	FS1	IN	Logic input frequency select Bit1*. Input latched at Poweron.
3, 9, 16, 22, 27, 33, 39, 45	GND	PWR	Ground.
4	X1	IN	Crystal input. Nominally 14.318 MHz. Has internal load cap
5	X2	OUT	Crystal output. Has internal load cap and feedack resistor to X1
41	VDDL	PWR	2.5 or 3.3V buffer power for CPUL and IOAPIC output buffers.
8, 10, 11, 12, 14,	BUS (1:5)	OUT	BUS clock outputs. see select table for frequency
15	BUS6	OUT	BUS clock output. See select table for frequency.*
	FS0	IN	Logic input frequency select Bit0.*. Input latched at Poweron.
23, 24	STP# (2:3)	IN	Bank enable solutions for SDRAM clocks see table above, Clocks are enabled in groups of 4. (STP2# stops DIMM bank2, STP3# stops DIMM bank 3 when low).
47	24M	OUT	24MHz fixed clock.*
	BSEL	IN	Logic input* for selecting synchronous or asynchronous BUS frequency- see table above. Input latched at Poweron.*
1, 6, 13, 19, 30, 36, 48	VDD3	PWR	3.3 volt core logic and buffer power
17, 18, 20, 21, 28, 29, 31, 32, 34, 35, 37, 38	SDRAM (1:12)	OUT	SDRAM clocks at CPU speed. See select table for frequency.
40	CPUH/AGP	OUT	CPU clock operates at SDRAM VDD level (3.3V nom), for AGP etc.
42, 43	CPUL (1:2)	OUT	CPU clock output clocks .See select table for frequency. Operates at down to 2.5V controlled by VDDL pin.
7, 25, 26	N/C	—	Pins not internally connected.
46	48M	OUT	48 MHz fixed clock output*.
	FS2	IN	Logic input frequency select Bit 2*. Input latched at Poweron.
44	IOAPIC	OUT	Reference clock (14.318MHz) powered by VDDL, operating 2.5 to 3.3V.

* Bidirectional input/output pins, input logic level determined at internal power-on-reset are latched. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V

Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 – 70° C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	STP# and latched inputs	-	-	0.2VDD	V
Input High Voltage	V_{IH}	STP# and latched inputs	$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	VIN=0V (STP# inputs)	-28.0	-10.5	-	□A
Input High Current	I_{IH}	VIN=VDD (STP# inputs)	-5.0	-	5.0	□A
Output Low Current	I_{OL1}	VOL=0.8V; for IOAPIC, CPUH, SDRAM, BUS & REF (and CPUL at VDDL = 3.0 to 3.7V)	19	30.0	-	mA
Output High Current	I_{OH1}	VOH=2.0V; for IOAPIC, CPUH, SDRAM, BUS & REF (and CPUL at VDDL = 3.0 to 3.7V)	-	-26.0	-16	mA
Output Low Current	I_{OL2}	VOL=0.8V; for fixed 24, 48 CLKs	16	25.0	-	mA
Output High Current	I_{OH2}	VOH=2.0V; for fixed 24, 48 CLKs	-	-22.0	-14	mA
Output Low Current	I_{OL3}	VOL=0.8V; for CPUL at VDDL = 2.5V	19	30.0	-	mA
Output High Current	I_{OH3}	VOH = 1.7V; for CPUL at VDDL = 2.5V	-	-12.5	-9.5	mA
Output Low Voltage	V_{OL1}	IOL = 10mA; -10mA for IOAPIC, CPUH, SDRAM, BUS & REF (and CPUL at VDDL = 3.0 to 3.7V)	-	0.22	0.4	V
Output High Voltage	V_{OH1}	IOH = -10mA; for CPUH, SDRAM, BUS & REF (and CPUL at VDDL = 3.0 to 3.7V)	2.4	2.8	-	V
Output Low Voltage	V_{OL2}	IOL = 8mA; for fixed CLKs	-	0.25	0.4	V
Output High Voltage	V_{OH2}	IOH = -8mA; for fixed CLKs	2.4	2.6	-	V
Output Low Voltage	V_{OL3}	IOL = 8mA; for CPUL at VDDL = 2.5V	-	0.25	0.4	V
Output High Voltage	V_{OH3}	IOH = -8mA; for CPUL at VDDL = 2.5V	1.95	2.1	-	V
Supply Current	I_{DD}	@66.6 MHz; all outputs unloaded	-	90	180	mA

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7V, T_A = 0 – 70° C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]	T_{r1}	20pF load, 0.8 to 2.0V CPU, SDRAM, BUS & REF	-	0.9	1.5	ns
Fall Time[1]	T_{f1}	20pF load, 2.0 to 0.8V CPU, SDRAM, BUS & REF	-	0.8	1.4	ns
Rise Time[1]	T_{r2}	20pF load, 20% to 80% CPU, SDRAM, BUS & REF	-	1.5	2.5	ns
Fall Time[1]	T_{f2}	20pF load, 80% to 20% CPU, SDRAM, BUS & REF	-	1.4	2.4	ns
Rise Time[1]	T_{r3}	20pF load, 0.8 to 2.0V fixed 24 & 48 clocks	-	1.7	2.5	ns
Fall Time[1]	T_{f3}	20pF load, 2.0 to 0.8V fixed 24 & 48 clocks	-	1.2	2.0	ns
Rise Time[1]	T_{r4}	20pF load, 0.4 to 2.0V , CPUL with VDDL = 2.5V	-	2.0	3.0	ns
Fall Time[1]	T_{f4}	20pF load, 2.0 to 0.4V, CPUL with VDDL = 2.5V	-	1.5	2.5	ns
Duty Cycle[1]	D_t	20pF load @ VOUT=1.4V	45	50	55	%
Jitter, One Sigma[1]	T_{jis1}	CPU & BUS Clocks; Load=20pF, SDRAM; Load = 30pF 25 MHz, BSEL=1	-	50	150	ps
Jitter, Absolute[1]	T_{jab1}	CPU & BUS Clocks; Load=20pF, SDRAM; Load = 30pF FOUT=25 MHz, BSEL=1	-250	-	250	ps
Jitter, One Sigma[1]	T_{jis2}	Fixed CLK; Load=20pF	-	1	3	%
Jitter, Absolute[1]	T_{jab2}	Fixed CLK; Load=20pF	-5	2	5	%
Input Frequency[1]	F_i		12.0	14.318	16.0	MHz
Logic Input Capacitance[1]	C_{IN}	Logic input pins	-	5	-	pF
Crystal Oscillator Capacitance[1]	C_{INX}	X1, X2 pins	-	18	-	pF
Power-on Time[1]	t_{on}	From VDD=1.6V to 1st crossing of 66.6 MHz VDD supply ramp < 40ms	-	2.5	4.5	ms
Clock Skew[1]	T_{sk1}	CPU to CPU; Load=20pF; @1.4V (Same VDD)	-	150	250	ps
Clock Skew[1]	T_{sk2}	BUS to BUS; Load=20pF; @1.4V	-	300	500	ps
Clock Skew[1]	T_{sk3}	CPU to BUS; Load=20pF; @1.4V (CPU is early)	1	2.6	4	ns
Clock Skew[1]	T_{SR4}	SDCPU (@3.3V) to CPU (@2.5V) (2.5V CPU is late)		250	400	ps

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Shared Pin Operation - Input/Output Pins

Pins 2, 15, 46 and 47 on the **ICS9147-03** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 4-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm(10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figs. 1 and 2 show the recommended means of implementing this function. In Fig. 1 either one of the resistors is loaded onto the board (selective stuffing) to configure the device's internal logic. Figs. 2a and b provide a single resistor loading option where either solder spot tabs or a physical jumper header may be used.

These figures illustrate the optimal PCB physical layout options. These configuration resistors are of such a large ohmic value that they do not effect the low impedance clock signals. The layouts have been optimized to provide as little impedance transition to the clock signal as possible, as it passes through the programming resistor pad(s).

Test Mode Operation

The **ICS9147-03** includes a production test verification mode of operation. This requires that the FS2 and FS1 pins be programmed to a logic high and the FS0 pin be programmed to a logic low(see Shared Pin Operation section). In this mode the device will output the following frequencies.

Pin		Frequency
REF, IOAPIC		REF
48MHz		REF/2
24MHz		REF/4
CPU, SDRAM		REF2
BUS	BSEL=1	REF/4
BUS	BSEL=0	REF/3

Note: REF is the frequency of either the crystal connected between the devices X1and X2, or, in the case of a device being driven by an external reference clock, the frequency of the reference (or test) clock on the device's X1 pin.

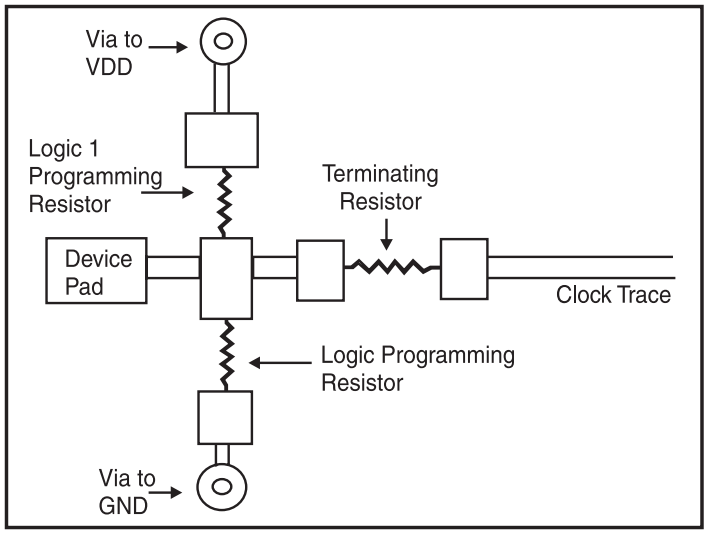


Fig. 1

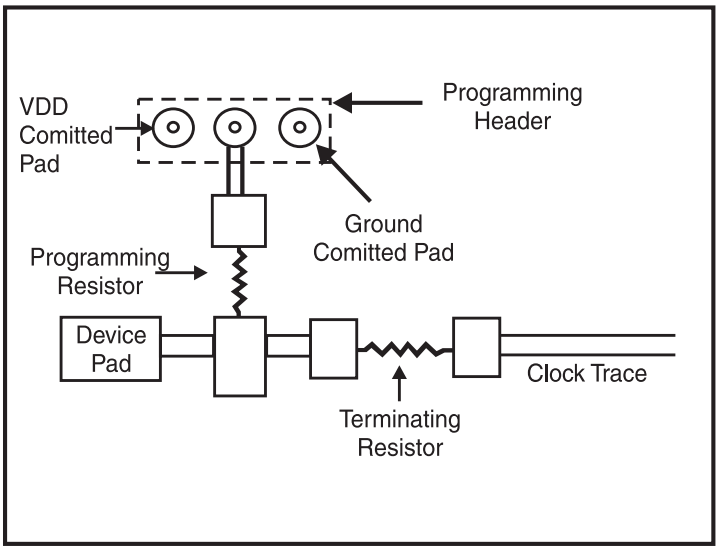

VDD
Comitted
Pad
Programming
Header
Ground
Comitted Pad
Programming
Resistor
Device
Pad
Clock Trace
Terminating
Resistor

Fig. 2a

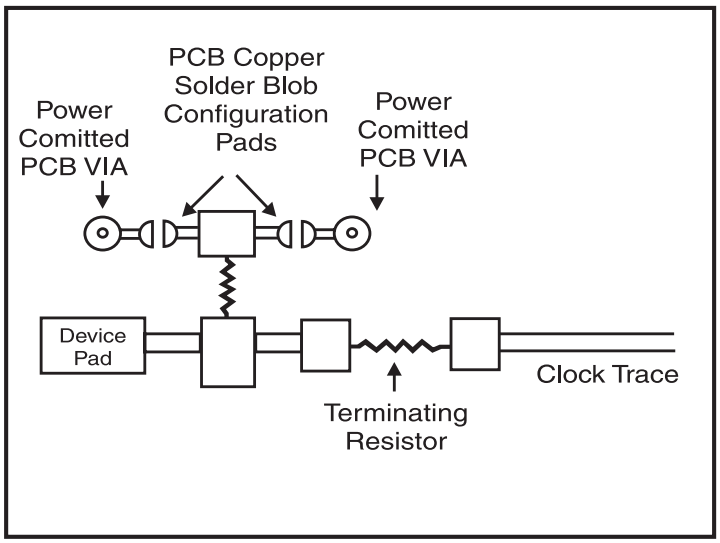
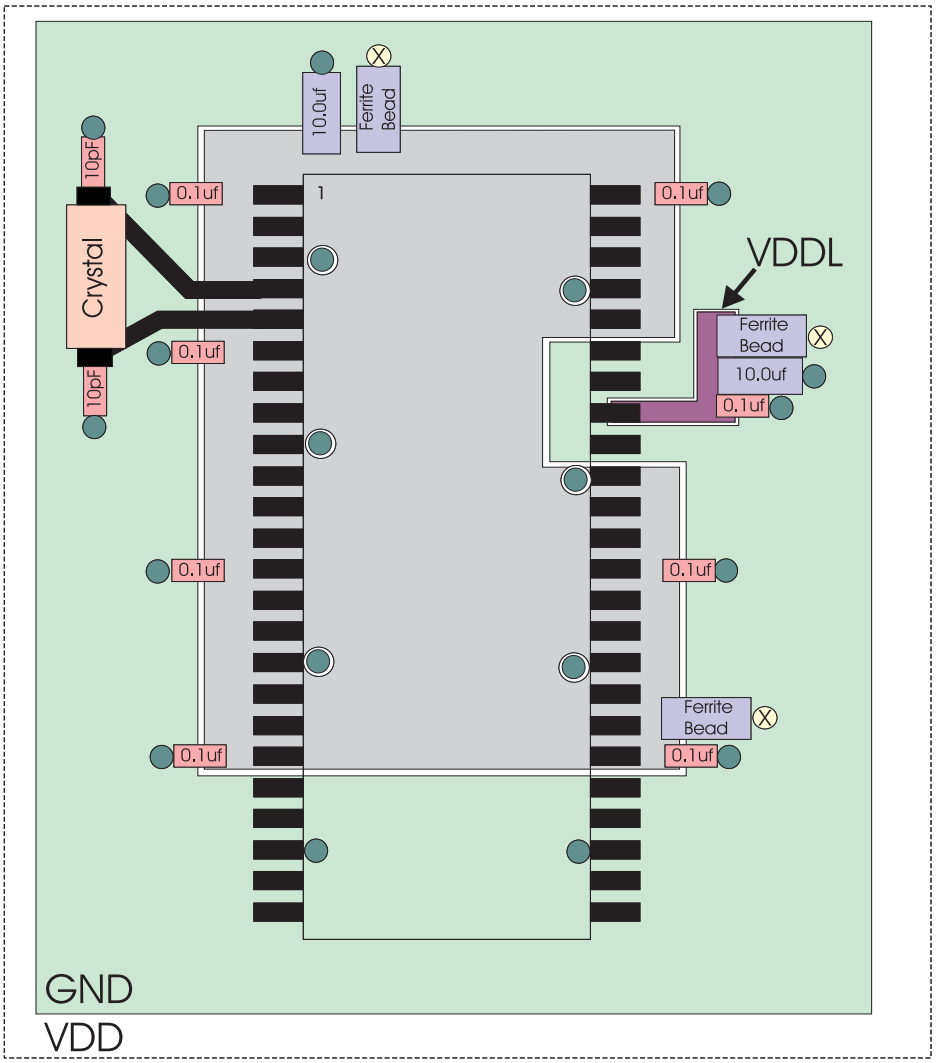

PCB Copper
Solder Blob
Configuration
Pads
Power
Comitted
PCB VIA
Power
Comitted
PCB VIA
Device
Pad
Clock Trace
Terminating
Resistor

Fig. 2b

Recommended PCB Layout for ICS9147-03



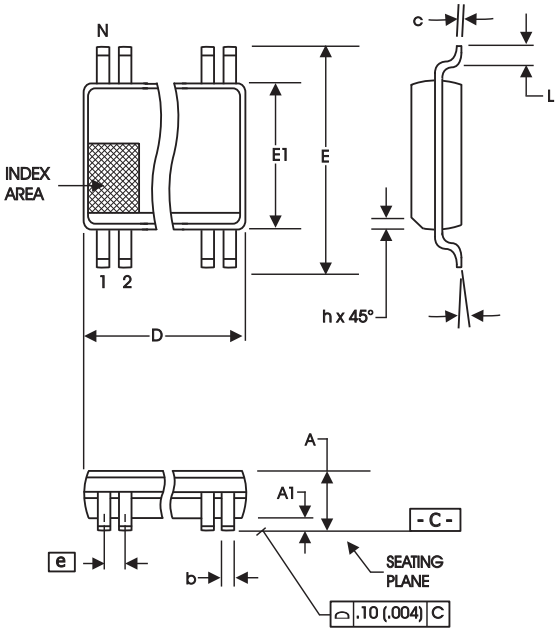
Connection to GND plane.

Connection to VDD plane.

Connection to VDDL plane.

Connection to System VCC plane

NOTE:
This PCB Layout is based on a 4 layer board with an internal Ground (common) and Vcc plane. Placement of components will depend on routing of signal trace. The 0.1uf Capacitors should be placed as close as possible to the Power pins. Placement on the backside of the board is also possible. The Ferrite Beads can be replaced with 10-15ohm Resistors. For best results, use a Fixed Voltage Regulator between the main (board) Vcc and the different Vdd planes.



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS9147F-03

Example:

ICS XXXX F - PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
F=SSOP

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS = Standard Device

ICS reserves the right to make changes in the device data identified in this publication without further notice. ICS advises its customers to obtain the latest version of all device data to verify that any information being relied upon by the customer is current and accurate.