Low Skew, 1-to-16 Differential-to-LVDS, Clock Distribution Chip

ICS8516I

DATA SHEET

General Description

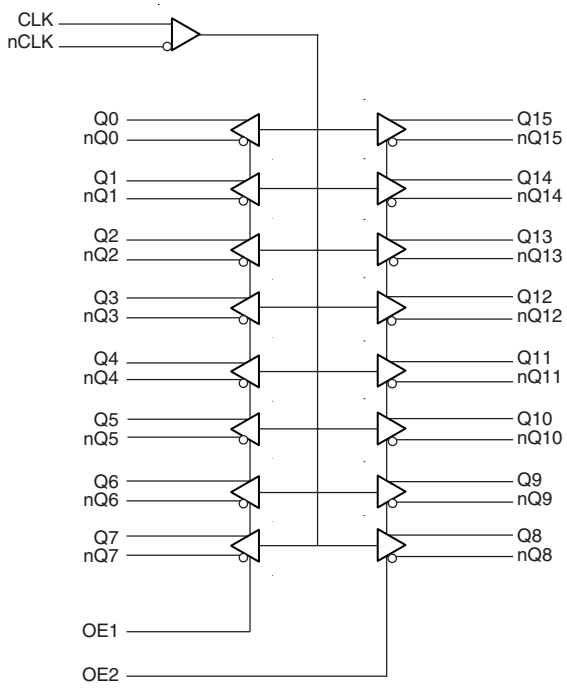
The ICS8516I is a low skew, high performance 1-to-16 Differential-to-LVDS Clock Distribution Chip and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS8516I CLK, nCLK pair can accept any differential input levels and translates them to 3.3V LVDS output levels. Utilizing Low Voltage Differential Signaling (LVDS), the ICS8516I provides a low power, low noise, point-to-point solution for distributing clock signals over controlled impedances of 100Ω.

Dual output enable inputs allow the ICS8516I to be used in a 1-to-16 or 1-to-8 input/output mode. Guaranteed output and part-to-part skew specifications make the ICS8516I ideal for those applications demanding well defined performance and repeatability.

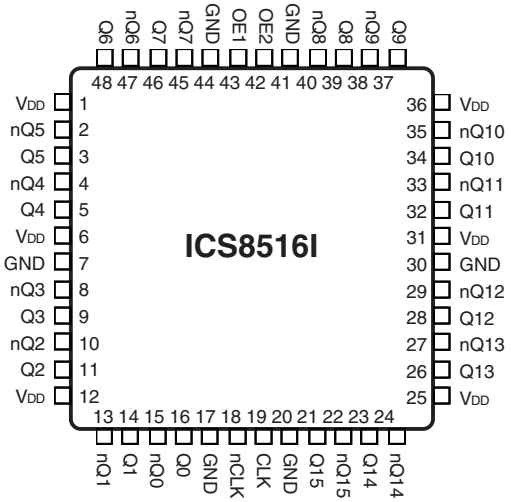
Features

- Sixteen Differential LVDS outputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Maximum output frequency: 700MHz
- Translates any differential input signal (LVPECL, LVHSTL, SSTL, DCM) to LVDS levels without external bias networks
- Translates any single-ended input signal to LVDS with resistor bias on nCLK input
- Multiple output enable inputs for disabling unused outputs in reduced fanout applications
- LVDS compatible
- Output skew: 65ps (maximum)
- Part-to-part skew: 550ps (maximum)
- Propagation delay: 2.4ns (maximum)
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



48-Lead LQFP
7mm x 7mm x 1.4mm body package
Y Package
Top View

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TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 6, 12, 25, 31, 36	V_{DD}	Power		Positive supply pins.
2, 3	nQ5, Q5	Output		Differential output pair. LVDS interface levels.
4, 5	nQ4, Q4	Output		Differential output pair. LVDS interface levels.
7, 17, 20, 30, 41, 44	GND	Power		Power supply ground.
8, 9	nQ3, Q3	Output		Differential output pair. LVDS interface levels.
10, 11	nQ2, Q2	Output		Differential output pair. LVDS interface levels.
13, 14	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
15, 16	nQ0, Q0	Output		Differential output pair. LVDS interface levels.
18	nCLK	Input	Pullup	Inverting differential clock input.
19	CLK	Input	Pulldown	Non-inverting differential clock input.
21, 22	Q15, nQ15	Output		Differential output pair. LVDS interface levels.
23, 24	Q14, nQ14	Output		Differential output pair. LVDS interface levels.
26, 27	Q13, nQ13	Output		Differential output pair. LVDS interface levels.
28, 29	Q12, nQ12	Output		Differential output pair. LVDS interface levels.
32, 33	Q11, nQ11	Output		Differential output pair. LVDS interface levels.
34, 35	Q10, nQ10	Output		Differential output pair. LVDS interface levels.
37, 38	Q9, nQ9	Output		Differential output pair. LVDS interface levels.
39, 40	Q8, nQ8	Output		Differential output pair. LVDS interface levels.
42, 43	OE2, OE1	Input	Pullup	Output enable. OE2 controls outputs Q8, nQ8 thru Q15, nQ15; OE1 controls outputs Q0, nQ0 thru Q7, nQ7. LVCMOS/LVTTL interface levels.
45, 46	nQ7, Q7	Output		Differential output pair. LVDS interface levels.
47, 48	nQ6, Q6	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

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TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
C_{PD}	Power Dissipation Capacitance (per output)			4		pF

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs		Outputs			
OE1	OE2	Q0:Q7	nQ0:nQ7	Q8:Q15	nQ8:nQ15
0	0	Hi Z	Hi Z	Hi Z	Hi Z
1	0	ACTIVE	ACTIVE	Hi Z	Hi Z
0	1	Hi Z	Hi Z	ACTIVE	ACTIVE
1	1	ACTIVE	ACTIVE	ACTIVE	ACTIVE

In the active mode, the state of the outputs are a function of the CLK and nCLK inputs as described in Table 3B.

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0:Q15	nQ0:nQ15		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single Ended Levels".

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Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Static Power Supply Current	R_L = 100Ω			185	mA
		No Load			80	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	OE1, OE2		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	OE1, OE2		-0.3		0.8	V
I_{IH}	Input High Current	OE1, OE2	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	OE1, OE2	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	V_{IN} = V_{DD} = 3.465V			150	µA
		nCLK	V_{IN} = V_{DD} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined ast V_{IH}.

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TABLE 4D. LVDS DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		250	400	600	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125	1.4	1.6	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV
I_{OZ}	High Impedance Leakage Current		-10		+10	µA
I_{OFF}	Power Off Leakage		-1		+1	µA
I_{OSD}	Differential Output Short Circuit Current				-5.5	mA
I_{OS}/I_{OSB}	Output Short Circuit Current				-12	mA

TABLE 5. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				700	MHz
t_{PD}	Propagation Delay; NOTE 1		1.6	2.0	2.4	ns
*t*sk(o)	Output Skew; NOTE 2, 4				65	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				550	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	Integration Range: 12kHz - 20MHz		148		fs
t_R/t_F	Output Rise/Fall Time	20% to 80%	50		600	ps
odc	Output Duty Cycle	$f \leq$ 600MHz	45		55	%
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 5				5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 5				5	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditons."

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

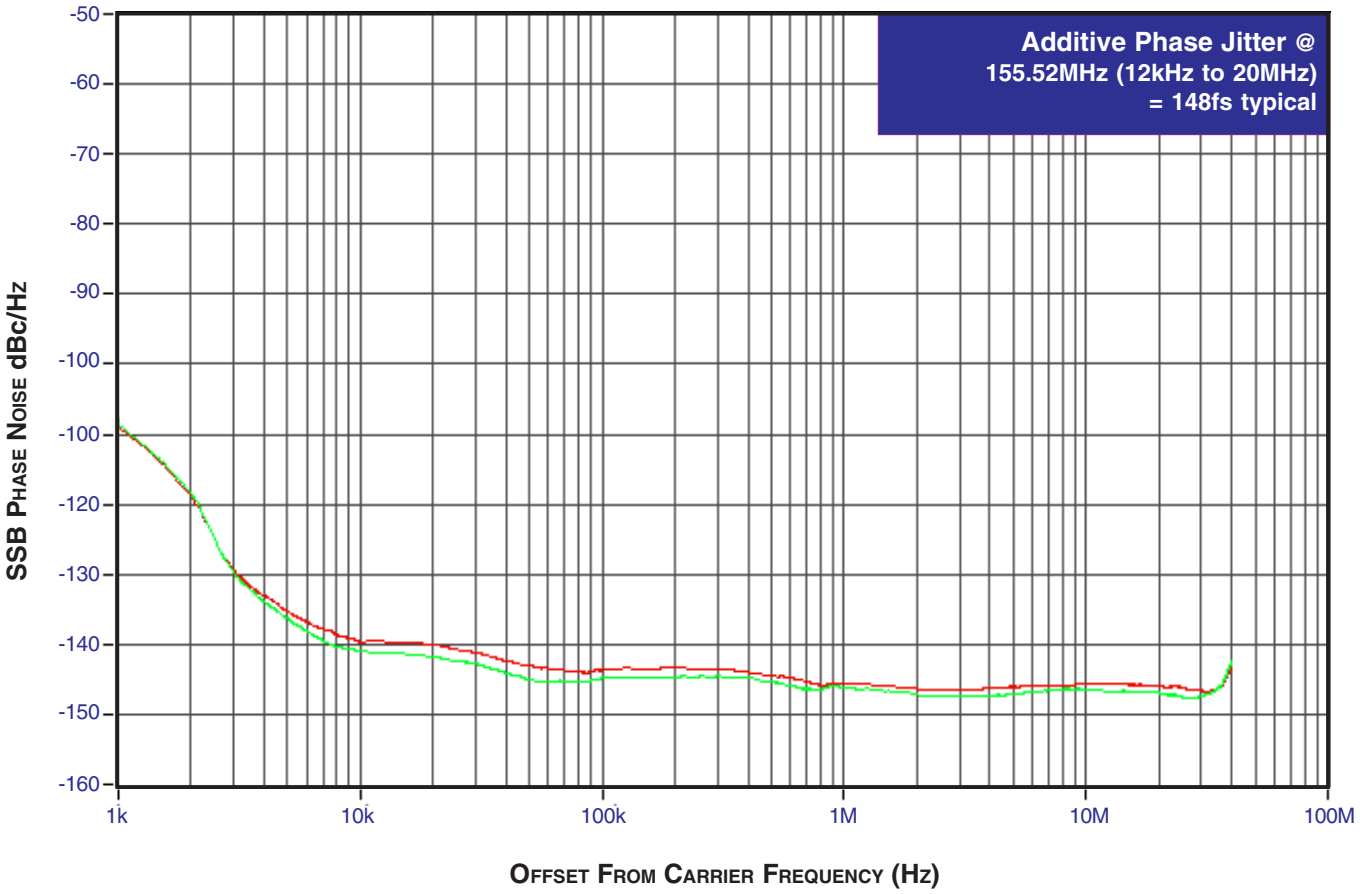
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

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Additive Phase Jitter

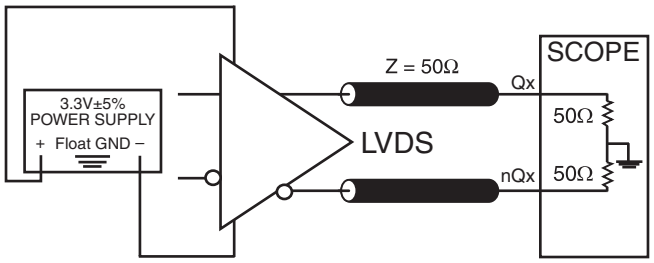
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



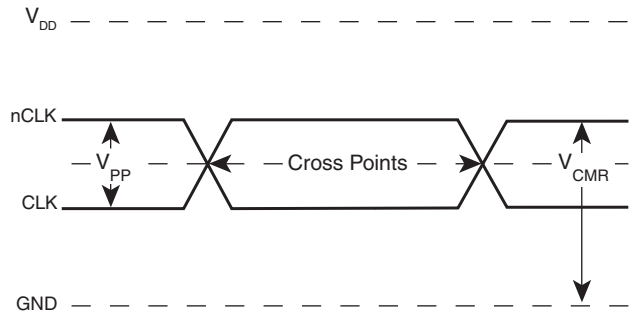
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

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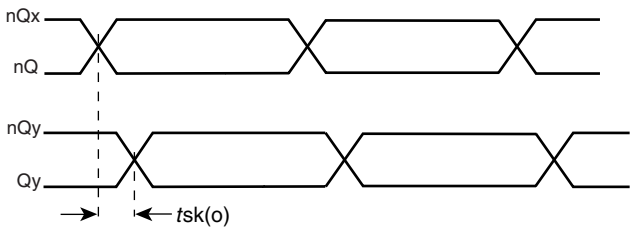
PARAMETER MEASUREMENT INFORMATION



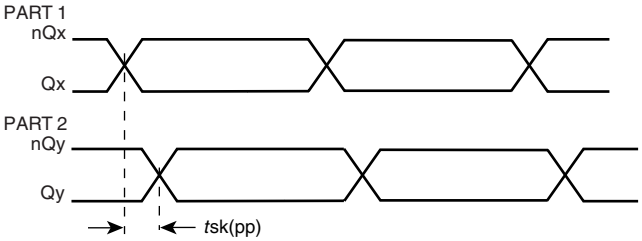
3.3V OUTPUT LOAD AC TEST CIRCUIT



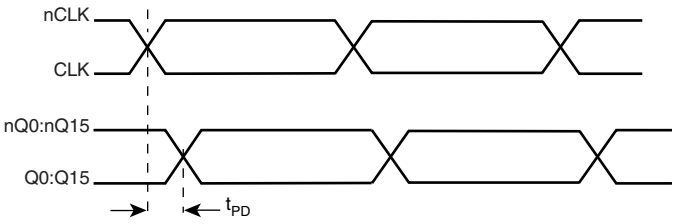
DIFFERENTIAL INPUT LEVEL



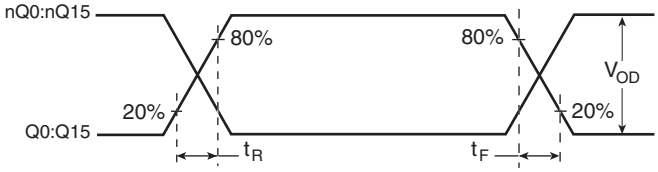
OUTPUT SKEW



PART-TO-PART SKEW



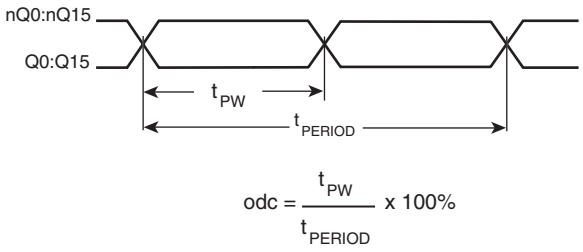
PROPAGATION DELAY



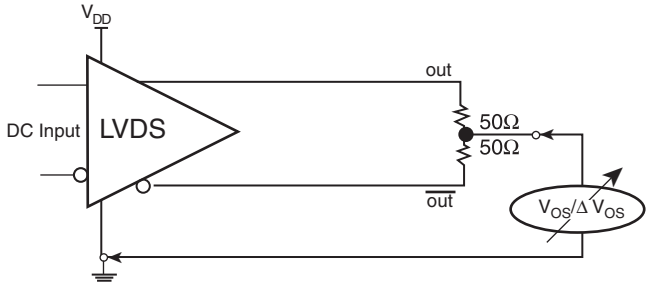
OUTPUT RISE/FALL TIME

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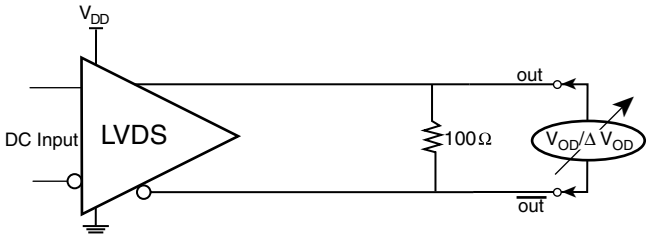
PARAMETER MEASUREMENT INFORMATION, CONTINUED



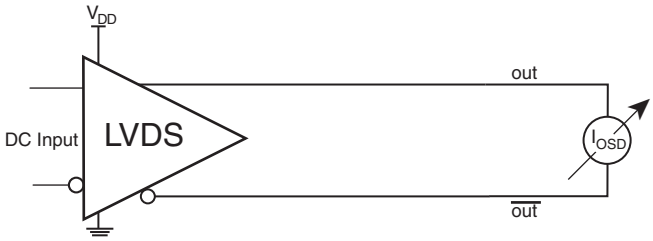
OUTPUT DUTY CYCLE/PULSE WIDTH PERIOD



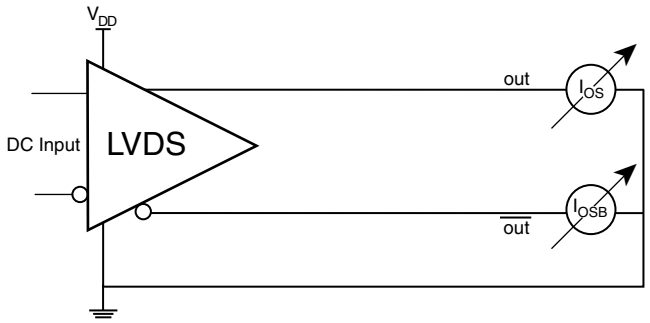
OFFSET VOLTAGE



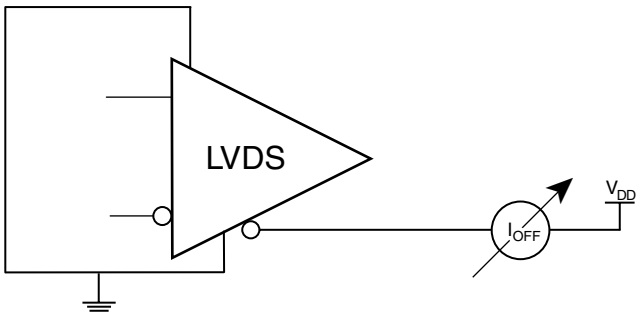
DIFFERENTIAL OUTPUT VOLTAGE



DIFFERENTIAL OUTPUT SHORT CIRCUIT CURRENT



OUTPUT SHORT CIRCUIT CURRENT



POWER OFF LEAKAGE

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APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD}= 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

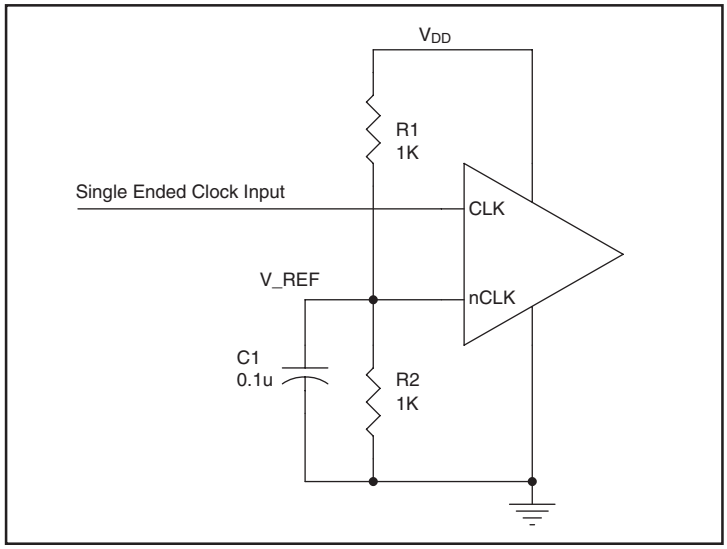


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK/nCLK INPUTS

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS CONTROL PINS

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVDS OUTPUTS

All unused LVDS outputs should be terminated with 100Ω resistor between the differential pair.

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Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termina-tion requirements. For example in Figure 2A, the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

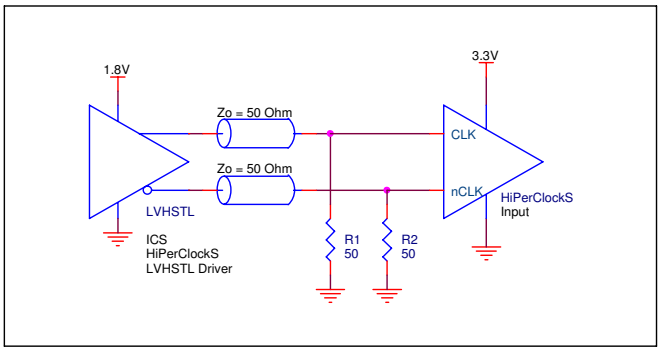


Figure 2A. HiPerClockS CLK/nCLK Input Driven by IDT HiPerClockS LVHSTL Driver

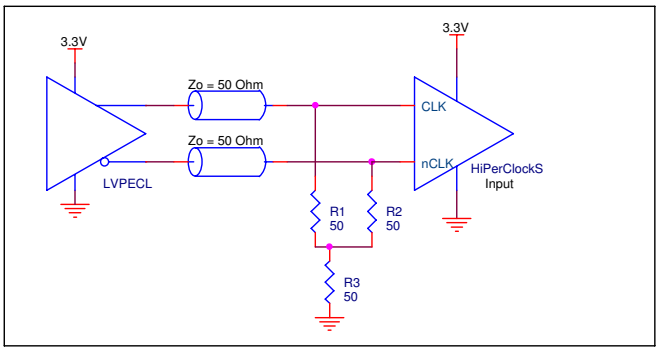


Figure 2B. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

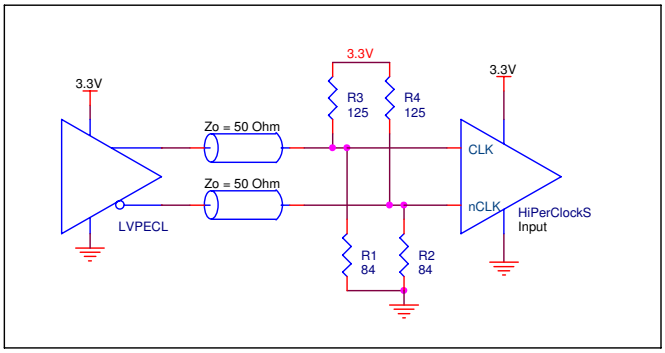


Figure 2C. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

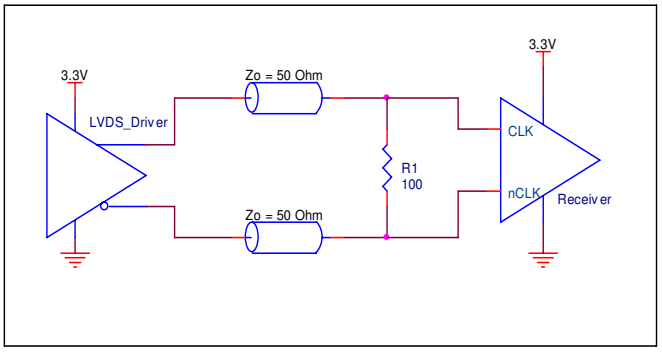


Figure 2D. HiPerClockS CLK/nCLK Input Driven by 3.3V LVDS Driver

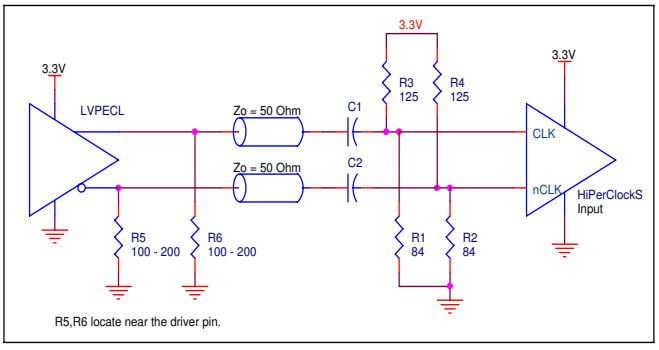


Figure 2E. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple

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SCHEMATIC EXAMPLE

Figure 3 shows a schematic example of ICS8516I. In this example, the input is driven by an LVDS driver. For LVDS buffer, it is recommended to terminate the unused outputs for better signal integrity. The decoupling capacitors should be physically located near the power pin.

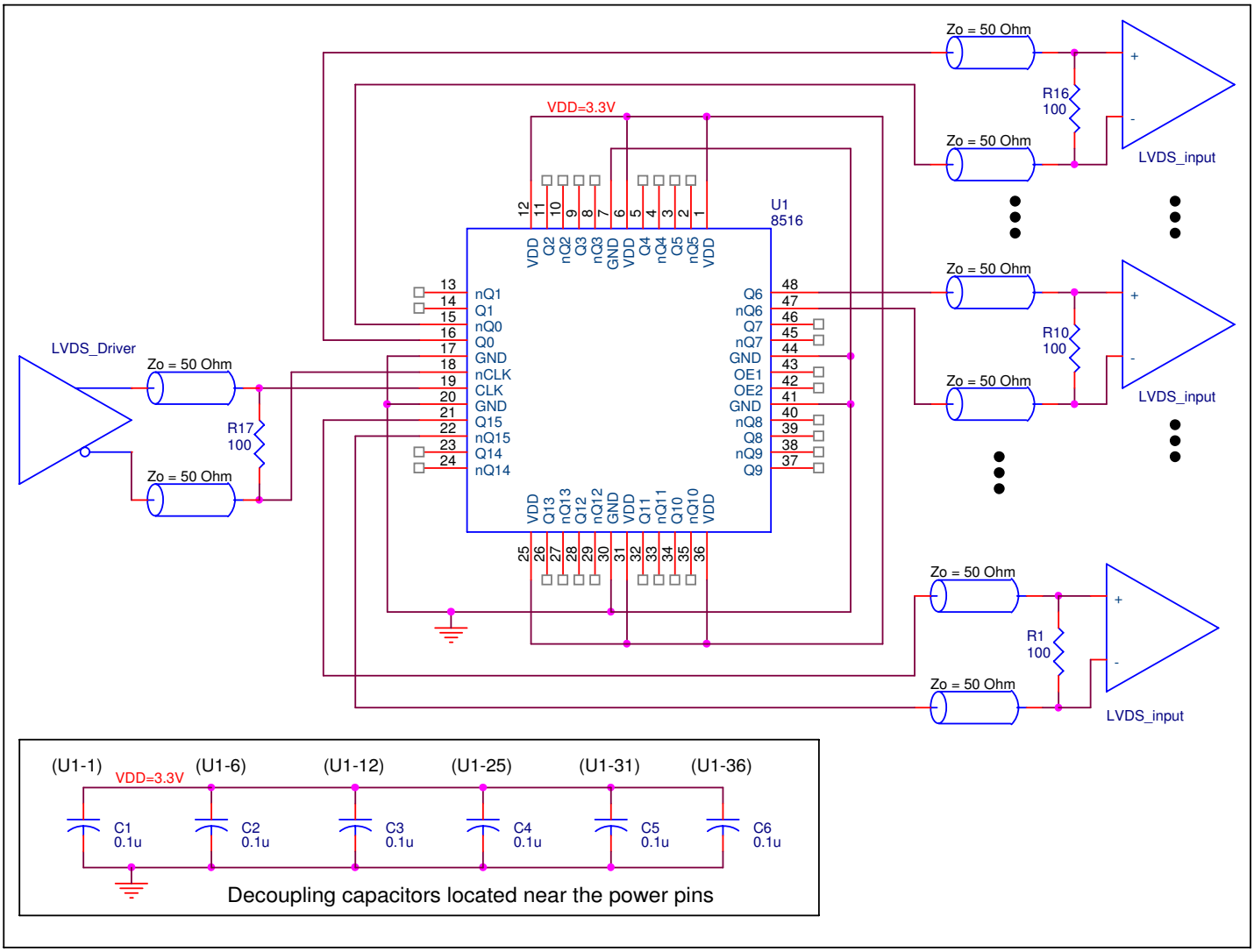


FIGURE 3. ICS8516I LVDS BUFFER SCHEMATIC EXAMPLE

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LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

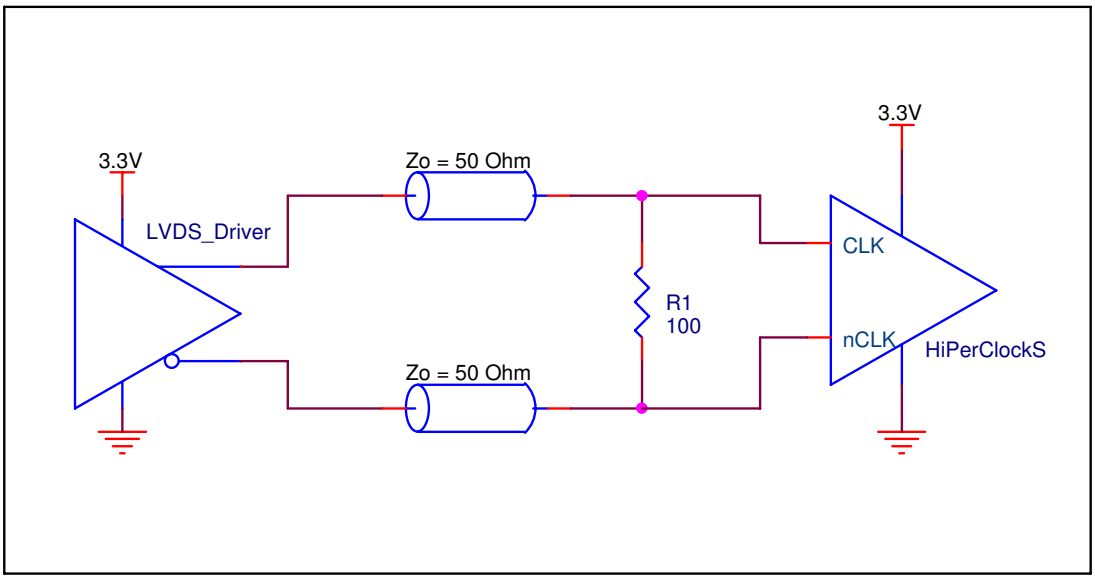


Figure 4. Typical LVDS Driver Termination

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POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8516I.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS8516I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power_$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 185mA = **641mW**

2. Junction Temperature.
Junction temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow of and a multi-layer board, the appropriate value is 47.9°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.641W * 47.9°C/W = 115.7°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 48-PIN LFQP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

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RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 48 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8516I is: 1821

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Package Outline - Y Suffix for 48 Lead LQFP

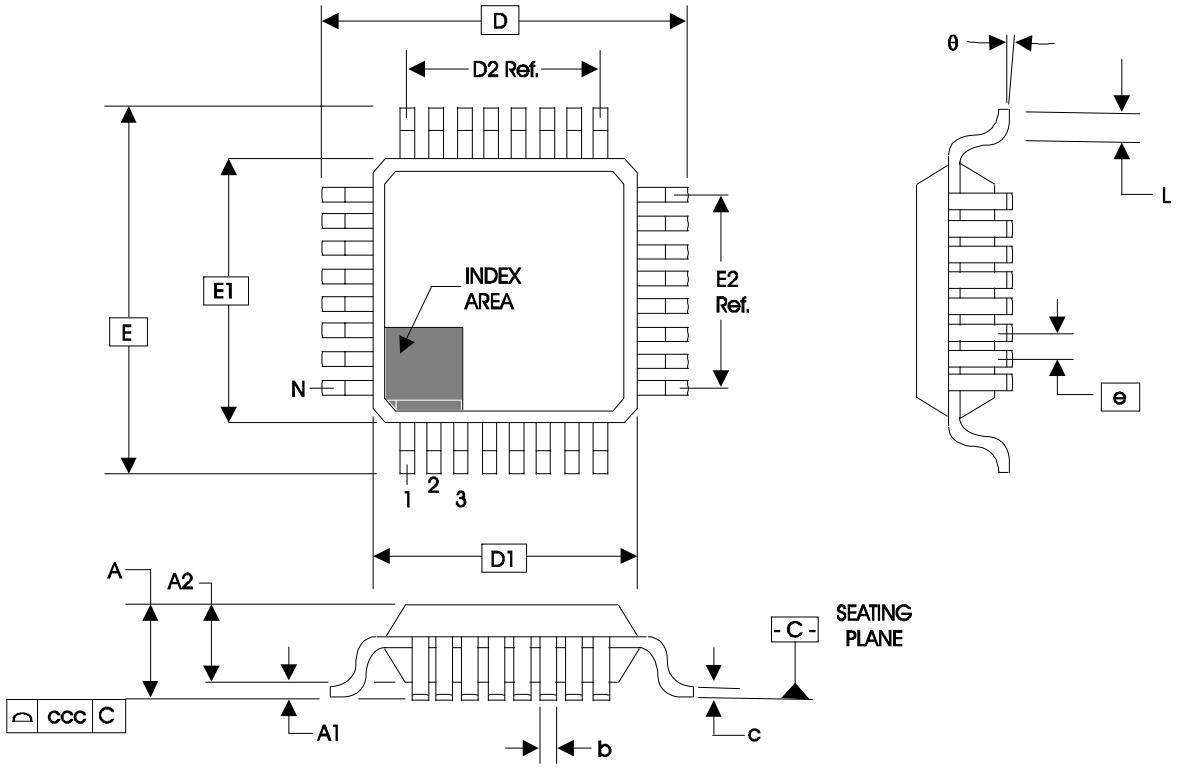


Table 8. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N		48	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

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TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8516FYI	ICS8516FYI	48 Lead LQFP	tray	-40°C to 85°C
8516FYIT	ICS8516FYI	48 Lead LQFP	1000 tape & reel	-40°C to 85°C
8516FYILF	ICS8516FYILF	48 Lead "Lead-Free" LQFP	tray	-40°C to 85°C
8516FYILFT	ICS8516FYILF	48 Lead "Lead-Free" LQFP	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T8	12	Ordering Information Table - added Lead-Free part numbers.	7/30/04
B	T5	1 5 6 9 13	Features section - added Lead-free bullet. AC Characteristics - added additive phase jitter spec. Added Additive Phase Jitter Plot. Added Recommendations for Unused Input & Output Pins. Added Power Considerations.	1/12/09
B		13	Replaced Junction Temperature First Paragraph. Updated Headers and Footers to new format.	9/10/09

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