FEMTOCLOCK™ CRYSTAL/LVCMOS-TO-LVDS/LVCMOS FREQUENCY SYNTHESIZER

ICS8440259D-45

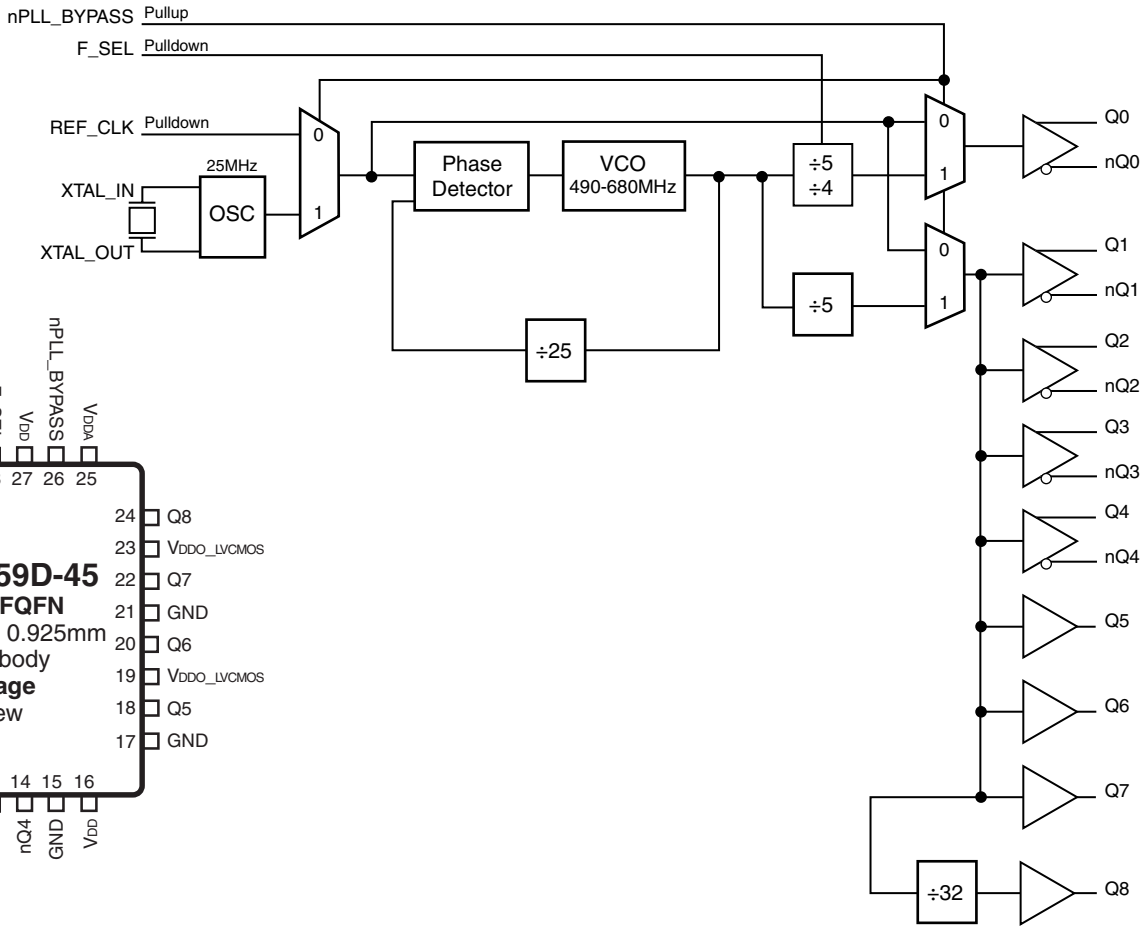
General Description

The ICS8440259D-45 is a 9 output synthesizer optimized to generate Gigabit and 10 Gigabit Ethernet clocks and is a member of the HiPerClockS™ family of high performance clock solutions from IDT. Using a 25MHz, 18pF parallel resonant crystal, the device will generate both 156.25MHz, 125MHz and 3.90625MHz clocks with mixed LVDS and LVCMOS/LVTTL output levels. The ICS8440259D-45 uses IDT's 3rd generation low phase noise VCO technology and can achieve <1ps typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS8440259D-45 is packaged in a small, 5mm x 5mm VFQFN package that is optimum for applications with space limitations.

Features

- One differential LVDS output at 156.25MHz or 125MHz
  Four differential LVDS outputs at 125MHz
  Three LVCMOS/LVTTL single-ended outputs at 125MHz
  One LVCMOS/LVTTL single-ended output at 3.90625MHz
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input and PLL bypass from a single select pin
- VCO range: 510MHz - 650MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.34ps (typical), LVDS output
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.31ps (typical), LVDS output
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment

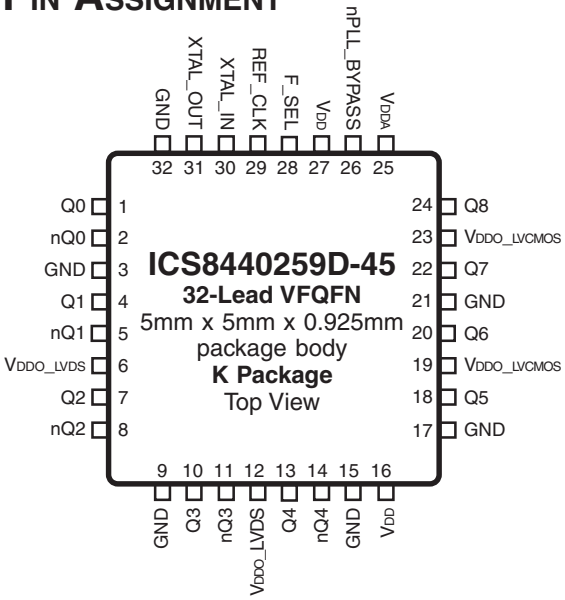


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential clock outputs. LVDS interface levels.
3, 9, 15, 17, 21, 32	GND	Power		Power supply ground.
4, 5	Q1, nQ1	Output		Differential clock outputs. LVDS interface levels.
6, 12	V_{DDO_LVDS}	Power		Output supply pins for Qx/nQx LVDS outputs.
7, 8	Q2, nQ2	Output		Differential clock outputs. LVDS interface levels.
10, 11	Q3, nQ3	Output		Differential clock outputs. LVDS interface levels.
13, 14	Q4, nQ4	Output		Differential clock outputs. LVDS interface levels.
16, 27	V_{DD}	Power		Core supply pins.
18, 20, 22, 24	Q5, Q6, Q7, Q8	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
19, 23	V_{DDO_LVCMOS}	Power		Output supply pins for Q5:Q8 LVCMOS outputs.
25	V_{DDA}	Power		Analog supply pin.
26	nPLL_BYPASS	Input	Pullup	Input select and PLL bypass control pin. See Table 3B. LVCMOS/LVTTL interface levels.
28	F_SEL	Input	Pulldown	Frequency select pin. See Table 3A. LVCMOS/LVTTL interface levels.
29	REF_CLK	Input	Pulldown	Single-ended LVCMOS/LVTTL reference clock input.
30, 31	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
C_{PD}	Power Dissipation Capacitance		$V_{DD,}V_{DDO_LVCMOS}$ = 3.465V		15		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	Q5:Q8			25		Ω

TABLE 3A. FREQUENCY SELECT FUNCTION TABLE

Input		Outputs
F_SEL	Output Divider	Q0/nQ0 Frequency
0	÷5	125MHz (default)
1	÷4	156.25MHz

TABLE 3B. PLL BYPASS AND INPUT SELECT FUNCTION TABLE

Inputs		
nPLL_BYPASS	PLL Bypass	Input Selected
0	PLL Bypassed	REF_CLK
1	PLL Enabled	XTAL_IN/XTAL_OUT (default)

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVCMOS)	-0.5V to V_{DDO_LVCMOS} + 0.5V
Outputs, I_O (LVDS)	
Continuous Current	10mA
Surge Current	15mA
Operating Temperature Range, T_A	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA}	37°C/W (0 mps)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO_LVCMOS} = V_{DDO_LVDS} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.35	3.3	V_{DD}	V
V_{DDO_LVCMOS}, V_{DDO_LVDS}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				118	mA
I_{DDA}	Analog Supply Current				35	mA
I_{DDO_LVCMOS}	LVCMOS Output Supply Current				10	mA
I_{DDO_LVDS}	LVDS Output Supply Current				160	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	REF_CLK (PD)	$V_{DD} = V_{IN} = 3.465V$			150	µA
		nPLL_BYPASS (PU)	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	REF_CLK (PD)	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
		nPLL_BYPASS (PU)	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage; NOTE 1	Q5:Q8	I_{OH} = -12mA	2.6			V
V_{OL}	Output Low Voltage; NOTE 1	Q5:Q8	I_{OL} = 12mA			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO_LVCMOS}/2. See Parameter Measurement Information, Output Load Test Circuit diagram.

TABLE 4C. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDO_LVDS} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		300	400	545	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.25	1.35	1.5	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

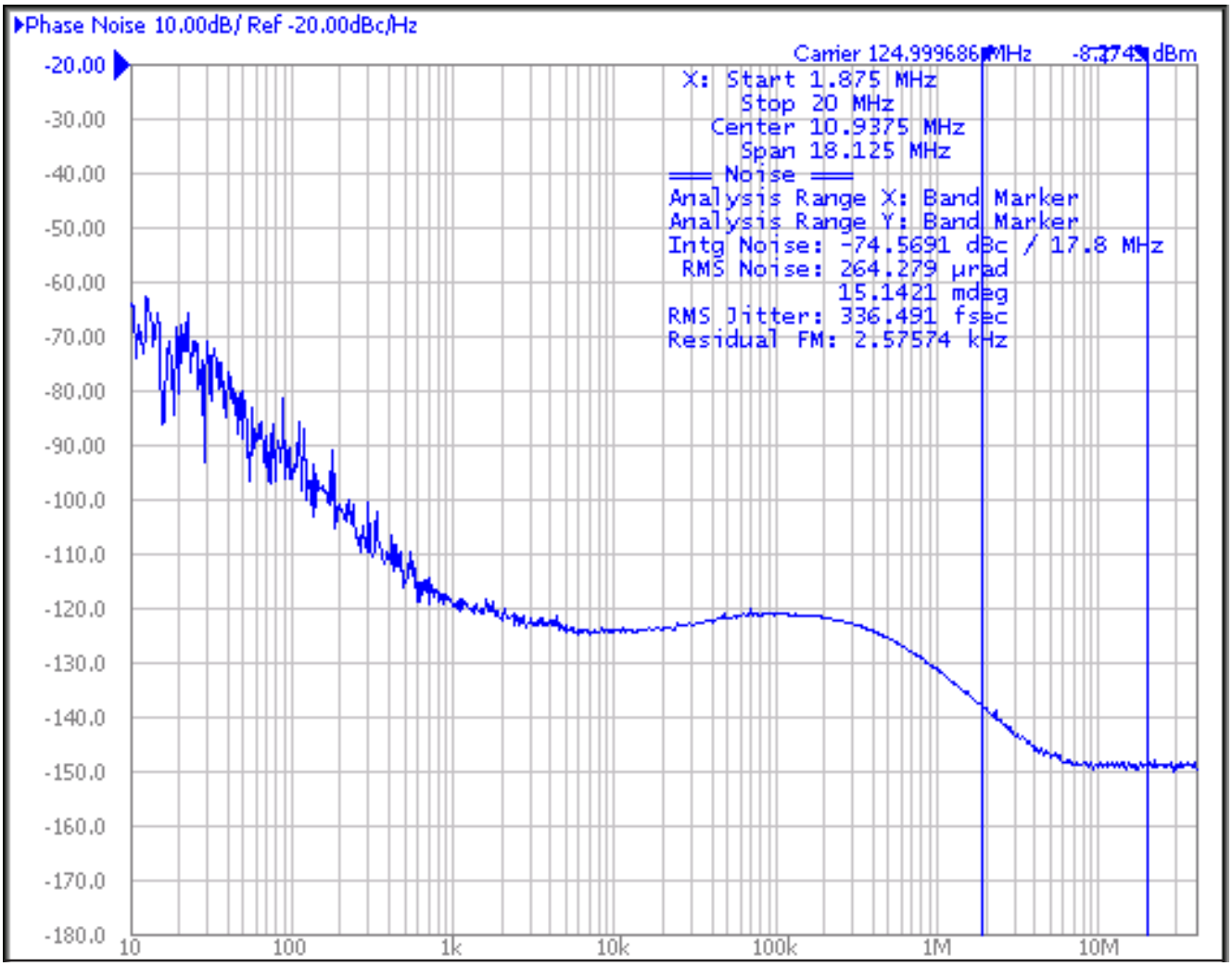
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDO_LVCMOS} = V_{DDO_LVDS} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Q0/nQ0:Q4/nQ4	F_SEL = 0 (default)		125		MHz
		Q5:Q7	F_SEL = 0 (default)		125		MHz
		Q8	F_SEL = 0 (default)		3.90625		MHz
		Q0/nQ0	F_SEL = 1		156.25		MHz
		Q[1:4]/nQ[1:4]	F_SEL = 1		125		MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1	Q[0:4]/nQ[0:4]	125MHz, (1.875MHz - 20MHz)		0.34		ps
		Q0/nQ0	156.25MHz, (1.875MHz - 20MHz)		0.31		ps
		Q5:Q7	125MHz, (1.875MHz - 20MHz)		0.48		ps
t_R / t_F	Output Rise/Fall Time	Q[0:4]/nQ[0:4] (NOTE 2)	PLL Mode, 125MHz, 30% to 70%	1.00E-10		1.02E-09	s
		Q[0:4]/nQ[0:4]	PLL Mode, 125MHz, 20% to 80%	1.50E-10		5.50E-10	s
		Q0/nQ0	PLL Mode, 156.25MHz, 20% to 80%	2.50E-10		3.75E-10	s
		Q5:Q7	PLL Mode, 125MHz, 20% to 80%	4.00E-10		1.15E-09	s
		Q8 (NOTE 2)	3.90625MHz, 20% to 80%	6.50E-10		1.35E-09	s
odc	Output Duty Cycle, PLL Mode	Q[0:4]/nQ[0:4]	125MHz	47		53	%
		Q0/nQ0	156.25MHz	48		52	%
		Q5:Q7	125MHz	45		55	%
		Q8	3.90625MHz	49		51	%
odc	Output Duty Cycle, BYPASS Mode	Q[0:4]/nQ[0:4]	125MHz	45		55	%
		Q0/nQ0	156.25MHz	45		55	%
		Q5:Q7	125MHz	45		55	%
		Q8	3.90625MHz	49		51	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Please refer to the Phase Noise Plots.
NOTE 2: Output loaded with 100Ω differential and 15pF loads.

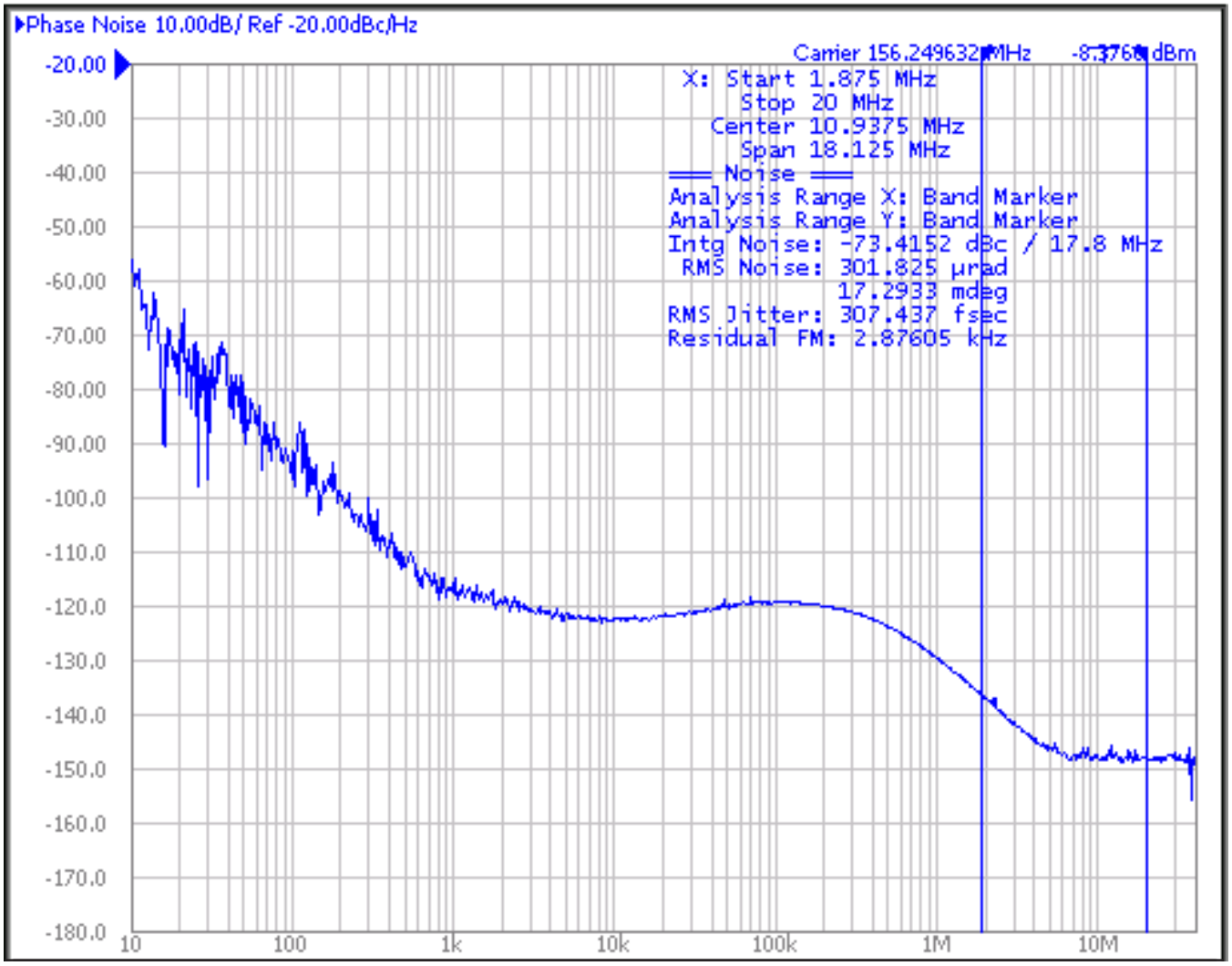
TYPICAL PHASE NOISE AT 125MHZ (LVDS @ 3.3V)



NOISE POWER $\frac{dBc}{Hz}$

OFFSET FREQUENCY (HZ)

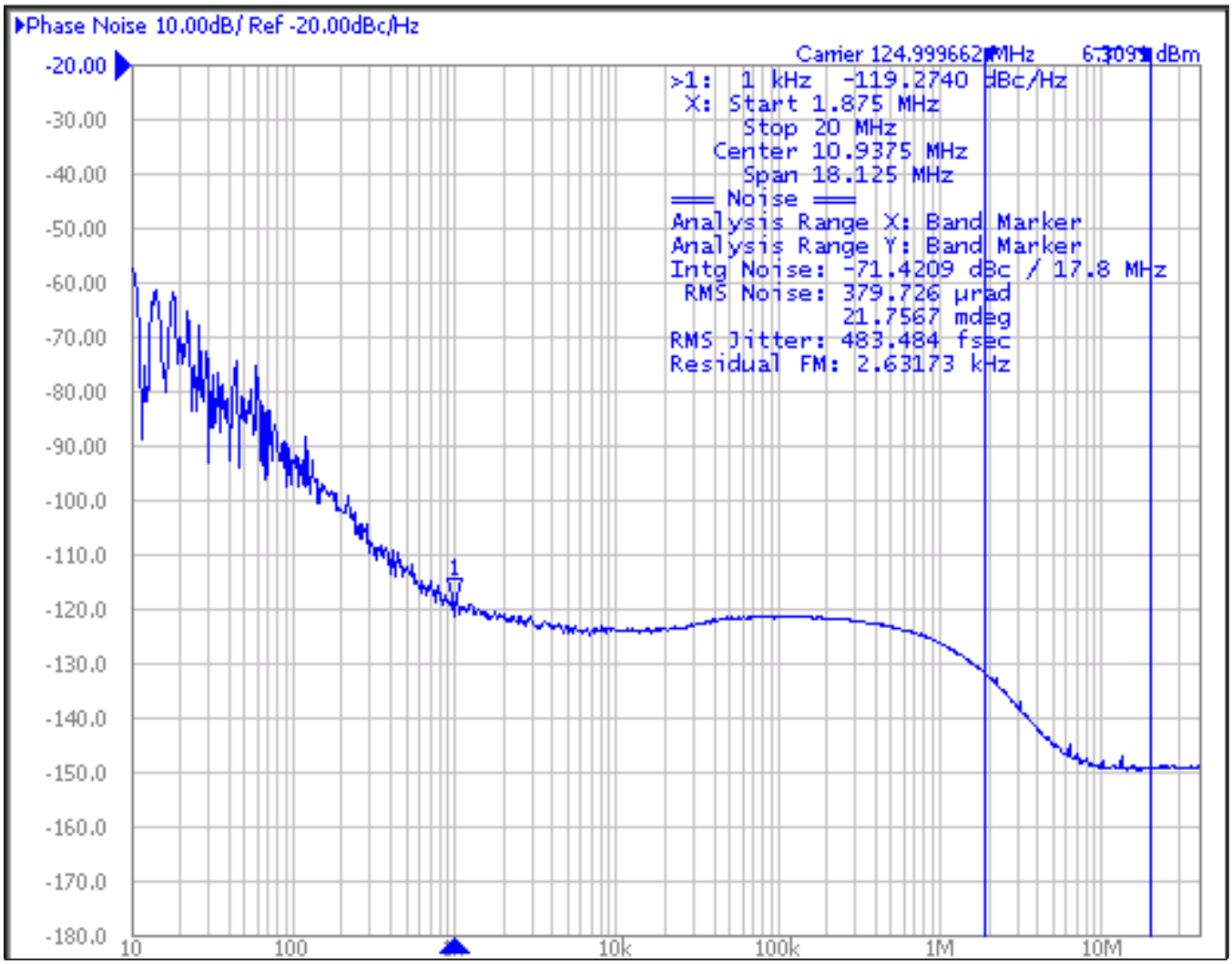
TYPICAL PHASE NOISE AT 156.25MHZ (LVDS @ 3.3V)



NOISE POWER dBc/Hz

OFFSET FREQUENCY (HZ)

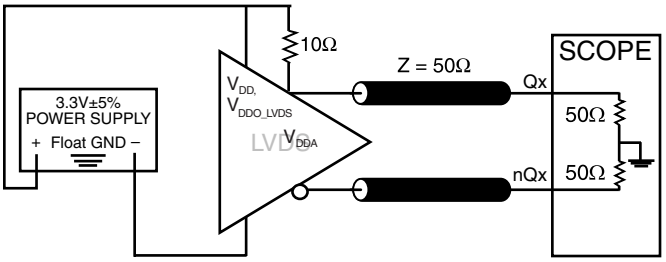
TYPICAL PHASE NOISE AT 125MHZ (LVCMOS @ 3.3V)



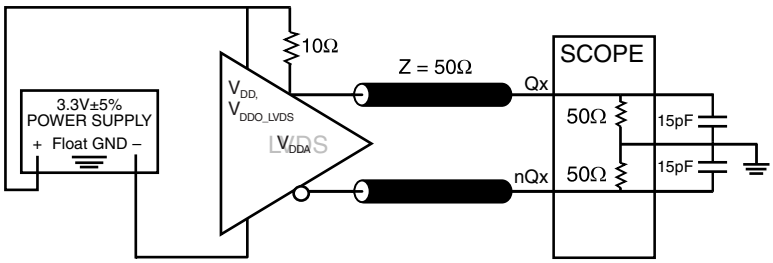
NOISE POWER $\frac{dBc}{Hz}$

OFFSET FREQUENCY (HZ)

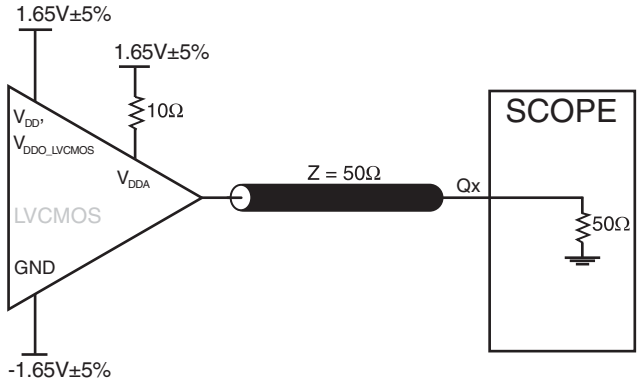
PARAMETER MEASUREMENT INFORMATION



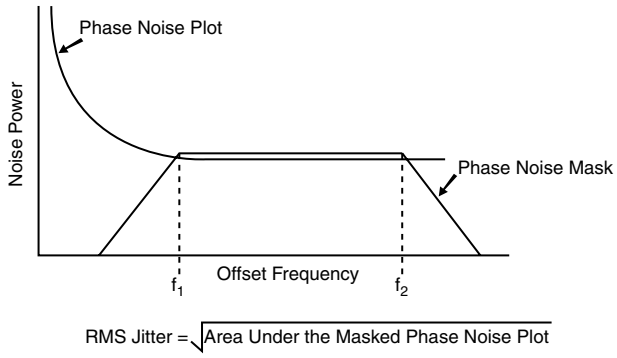
3.3V LVDS OUTPUT LOAD AC TEST CIRCUIT



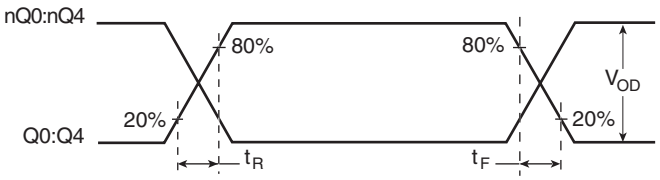
3.3V LVDS OUTPUT LOAD AC TEST CIRCUIT WITH 18pF



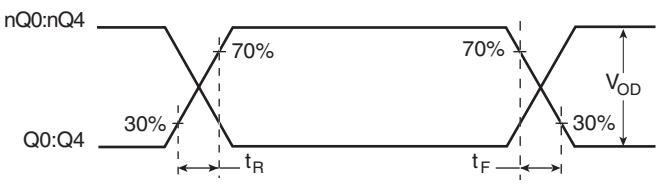
3.3V LVCMOS OUTPUT LOAD AC TEST CIRCUIT



RMS PHASE JITTER

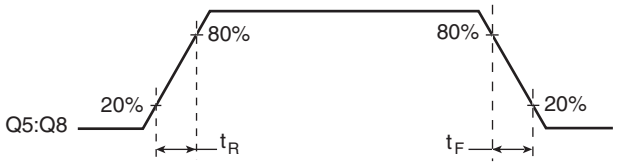


LVDS OUTPUT RISE/FALL TIME

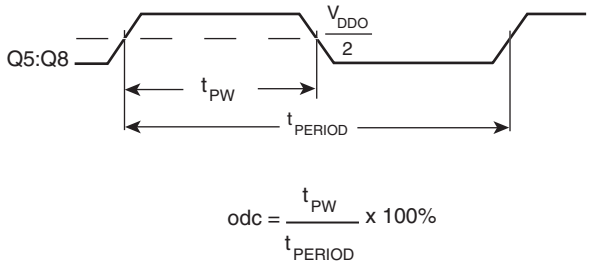


LVDS OUTPUT RISE/FALL TIME

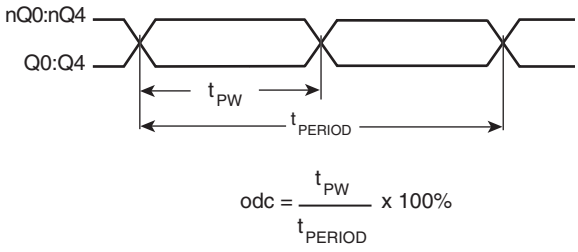
PARAMETER MEASUREMENT INFORMATION, CONTINUED



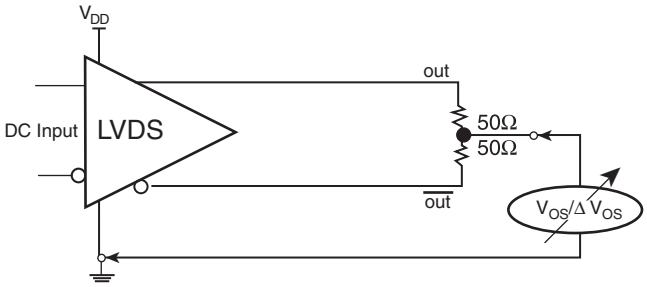
LVCMOS OUTPUT RISE/FALL TIME



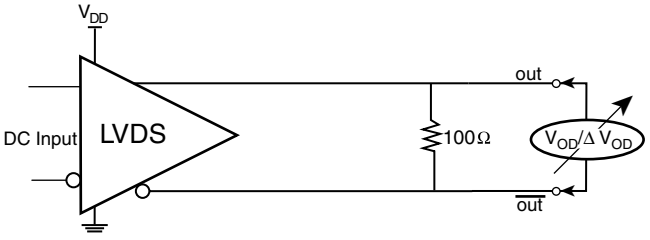
LVCMOS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



LVDS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS8440259D-45 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, V_{DDO_LVDS} and V_{DDO_LVCMOS} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

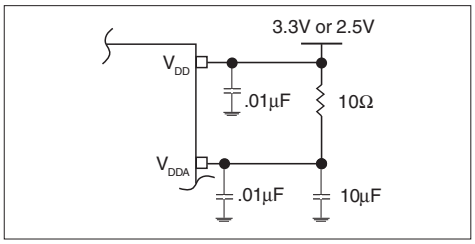


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK INPUT

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS CONTROL PINS

All control pins have internal pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUTS

All unused LVCMOS output can be left floating. There should be no trace attached.

LVDS OUTPUTS

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Crystal Input Interface

The ICS8440259D-45 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

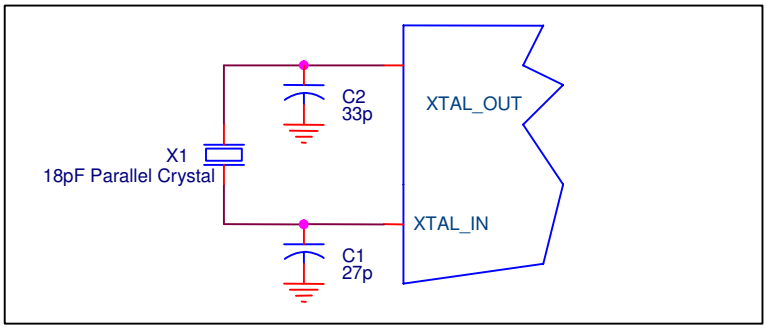


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC couple capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

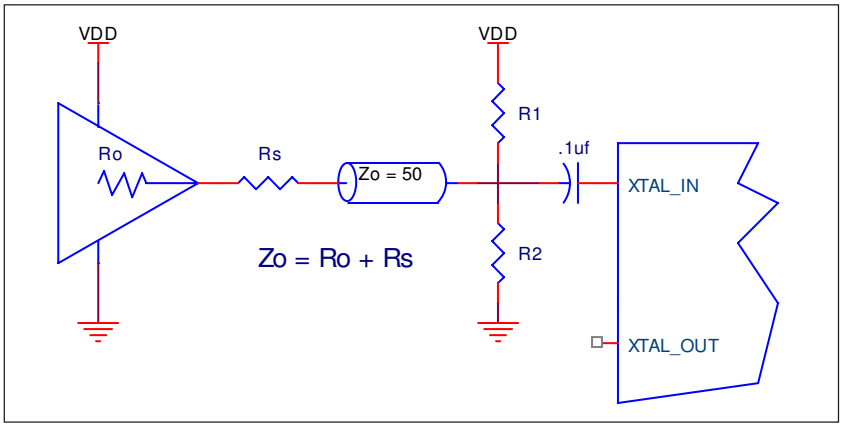


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

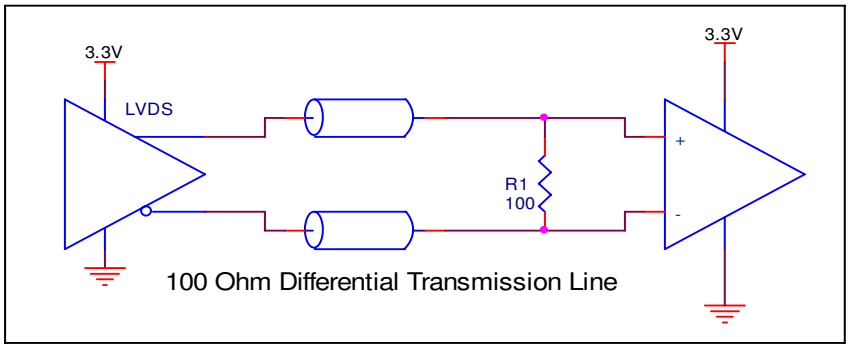


Figure 4. Typical LVDS Driver Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

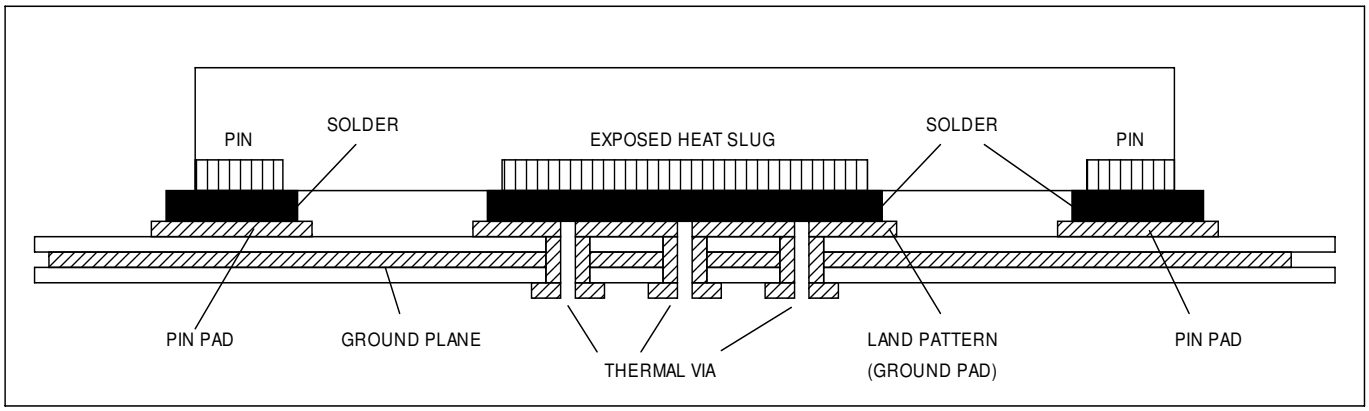


Figure 5. P.C.Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8440259D-45.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS840259D-45 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

Core and LVDS Output Power Dissipation

- Power (core, LVDS) = V_{DD_MAX} * (I_{DD} + I_{DDO_LVDS} + I_{DDA}) = 3.465V * (118mA + 160mA + 35mA) = **1084.545mW**

LVCMOS Output Power Dissipation

- Power (LVCMOS, no-load) = V_{DD_MAX} * I_{DDO_LVCMOS} = 3.465V * 10mA = **34.65mW**
- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to V_{DDO}/2
  Output Current I_{OUT} = V_{DDO_MAX} / [2 * (50Ω + R_{OUT})] = 3.465V / [2 * (50Ω + 25Ω)] = **23.1mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (R_{OUT}) = R_{OUT} * (I_{OUT})^2 = 25Ω * (23.1mA)^2 = **13.3mW per output**
- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT}) = 13.3mW * 4 = **53.2mW**
- Dynamic Power Dissipation at 125MHz
  Power (125MHz) = C_{PD} * Frequency * (V_{DDO})^2 = 15pF * 125MHz * (3.465V)^2 = **22.5mW per output**
  Total Power (125MHz) = **22.5mW * 3 = 67.5mW**
- Dynamic Power Dissipation at 3.9MHz
  Power (3.9MHz) = C_{PD} * frequency * (V_{DDO})^2 = 15pF * 3.90625MHz * (3.465V)^2 = **0.7mW per output**

Total Power Dissipation

- **Total Power**
  = Power (core, LVDS) + Power (LVCMOS-no load) + Total Power (R_{OUT}) + Total Power (125MHz) + Total Power (3.9MHz)
  = 1084.545mW + 34.65mW + 53.2mW + 67.5mW + 0.7mW
  = 1240.595mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 7.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 1.241W * 37°C/W = 115.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 32-LEAD VFQFN, FORCED CONVECTION

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

RELIABILITY INFORMATION

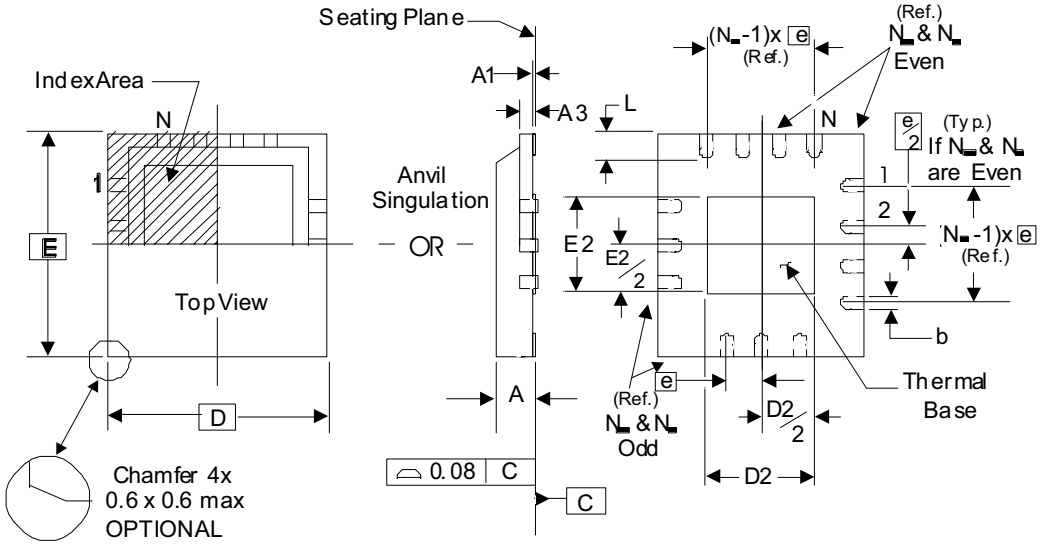
TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD VFQFN

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

TRANSISTOR COUNT

The transistor count for ICS8440259D-45 is: 2975

PACKAGE OUTLINE - K SUFFIX FOR 32 LEAD VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page.

TABLE 9. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	VHHD-2		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	0.80	--	1.00
A1	0	--	0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D			8
N_E			8
D		5.00 BASIC	
D2	1.25	2.25	3.25
E		5.00 BASIC	
E2	1.25	2.25	3.25
e		0.50 BASIC	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8440259DK-45LF	ICS0259D45L	32 Lead "Lead-Free" VFQFN	Tray	0°C to 70°C
8440259DK-45LFT	ICS0259D45L	32 Lead "Lead-Free" VFQFN	1000 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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