Integrated Circuit Systems, Inc.

ICS83026I

LOW SKEW, 1-TO-2 DIFFERENTIAL-TO-LVCMOS/LVTTL FANOUT BUFFER

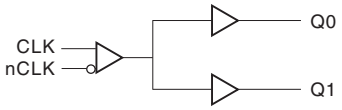
GENERAL DESCRIPTION

The ICS83026I is a low skew, 1-to-2 Differential-to-LVCMOS/LVTTL Fanout Buffer and a member of the HiPerClockS™family of High Performance Clock Solutions from ICS.The differential input can accept most differential signal types (LVDS, LVHSTL, LVPECL, SSTL, and HCSL) and translate to two single-ended LVCMOS/LVTTL outputs with a maximum output skew of 20ps. The small 8-lead SOIC footprint makes this device ideal for use in applications with limited board space.

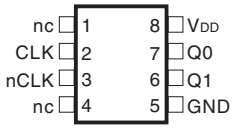
FEATURES

- 2 LVCMOS / LVTTL outputs
- Differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency: 350MHz (typical)
- Output skew: 20ps (maximum)
- Part-to-part skew: 600ps (maximum)
- Small 8 lead SOIC package saves board space
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Lead-Free package available
- Pin-to-pin compatible with MC100EPT26

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS83026I
8-Lead SOIC
3.8mm x 4.8mm, x 1.47mm package body
M Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 4	nc	Unused		No connect.
2	CLK	Input	Pulldown	Non-inverting differential clock input.
3	nCLK	Input	Pullup	Inverting differential clock input.
5	GND	Power		Power supply ground.
6	Q1	Output		Single clock output. LVCMOS / LVTTL interface levels.
7	Q0	Output		Single clock output. LVCMOS / LVTTL interface levels.
8	V_{DD}	Power		Positive supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD} = 3.6V		23		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
R_{OUT}	Output Impedance		5	7	12	Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	112.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±0.3V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Power Supply Current				35	mA

TABLE 3B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±0.3V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		2.6			V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DD}/2$. See Parameter Measurement Information, 3.3V Output Load Test Circuit.

TABLE 3C. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±0.3V, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK	$V_{IN} = V_{DD} = 3.6V$			5	µA
		CLK	$V_{IN} = V_{DD} = 3.6V$			150	µA
I_{IL}	Input Low Current	nCLK	$V_{IN} = 0V, V_{DD} = 3.6V$	-150			µA
		CLK	$V_{IN} = 0V, V_{DD} = 3.6V$	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

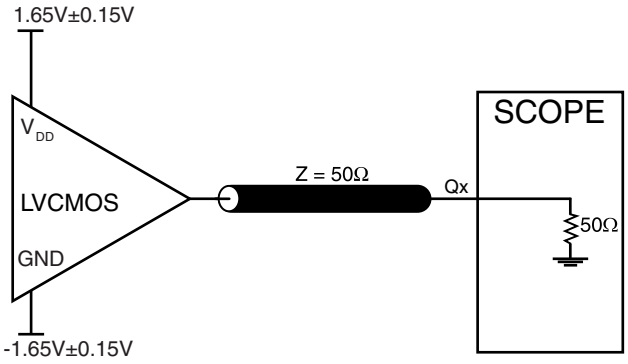
NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4. AC CHARACTERISTICS, V_{DD} = 3.3V±0.3V, T_A = -40°C TO 85°C

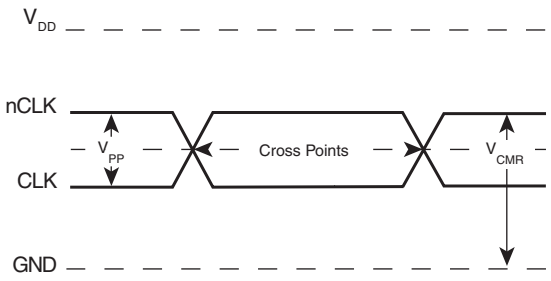
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			350		MHz
t_{PD}	Propagation Delay, NOTE 1	$f \leq$ 350MHz	1.7	2.1	2.5	ns
*t*sk(o)	Output Skew; NOTE 2, 4			5	20	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				600	ps
t_R / t_F	Output Rise/Fall Time	0.8V to 2V	150	300	450	ps
odc	Output Duty Cycle		40	50	60	%

All parameters measured at f_{MAX} unless noted otherwise. See Parameter Measurement Information.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DD}/2$.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DD}/2$.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DD}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

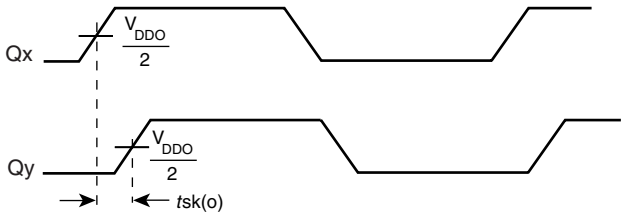
PARAMETER MEASUREMENT INFORMATION



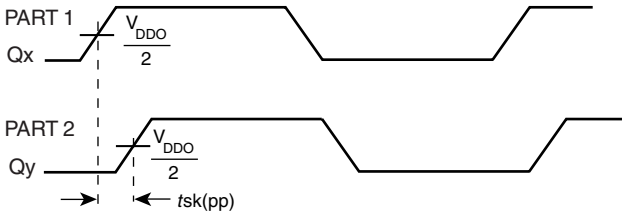
3.3VCORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



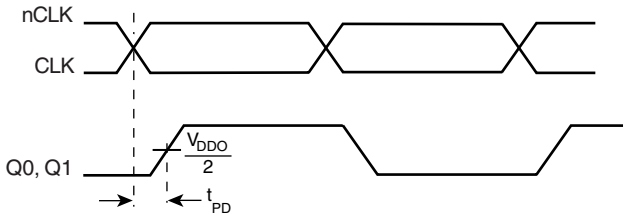
DIFFERENTIAL INPUT LEVEL



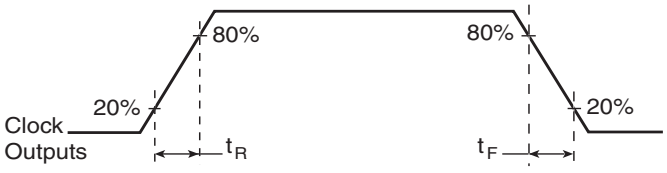
OUTPUT SKEW



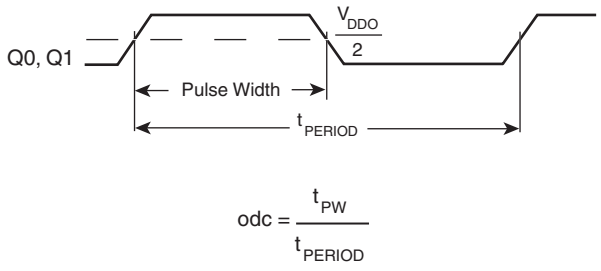
PART-TO-PART SKEW



PROPAGATION DELAY



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

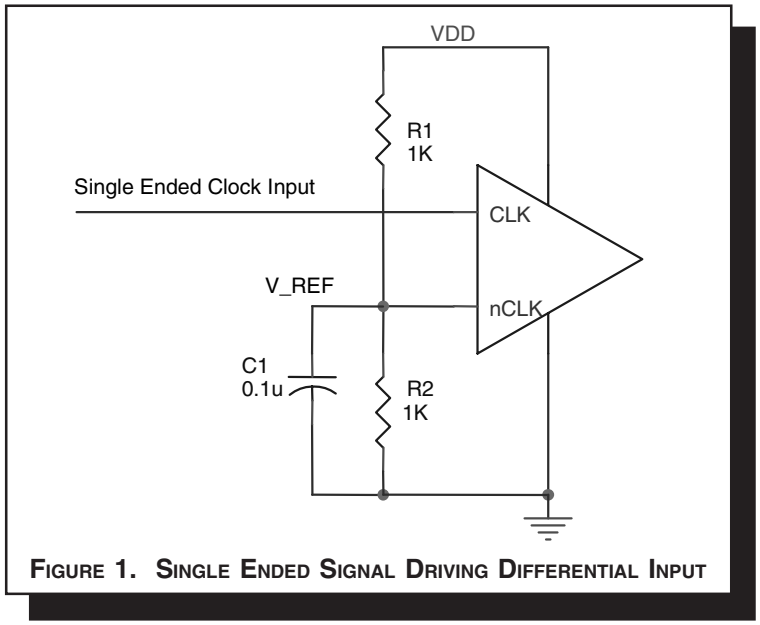


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

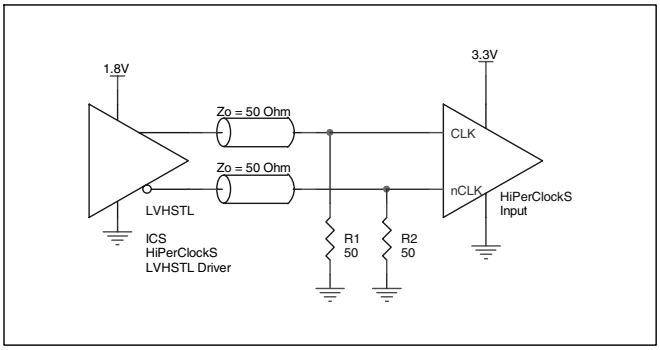


FIGURE 2A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

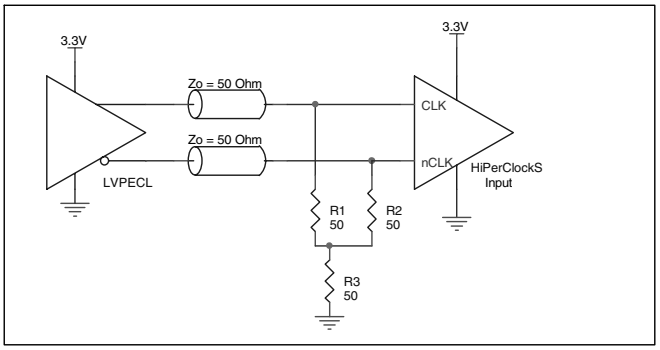


FIGURE 2B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

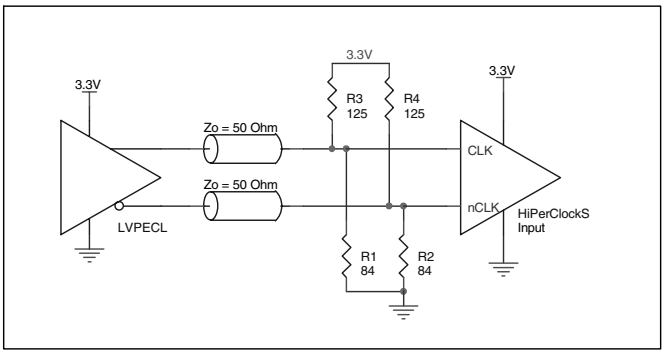


FIGURE 2C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

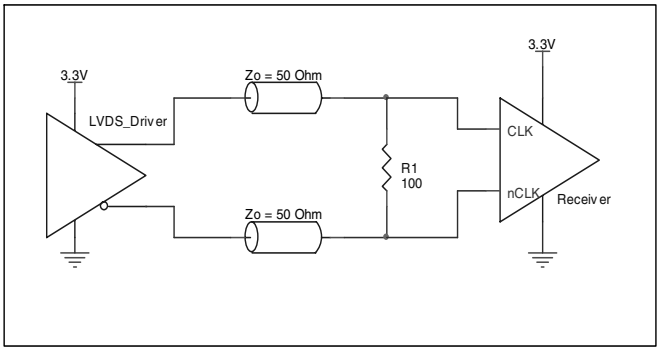


FIGURE 2D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

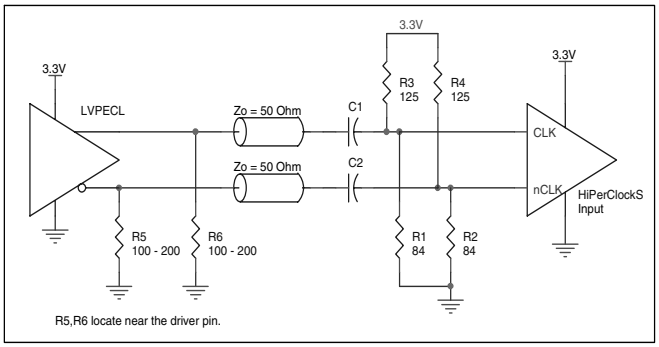


FIGURE 2E. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

RELIABILITY INFORMATION

TABLE 5. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS83026I is: 416

PACKAGE OUTLINE - SUFFIX M FOR 8 LEAD SOIC

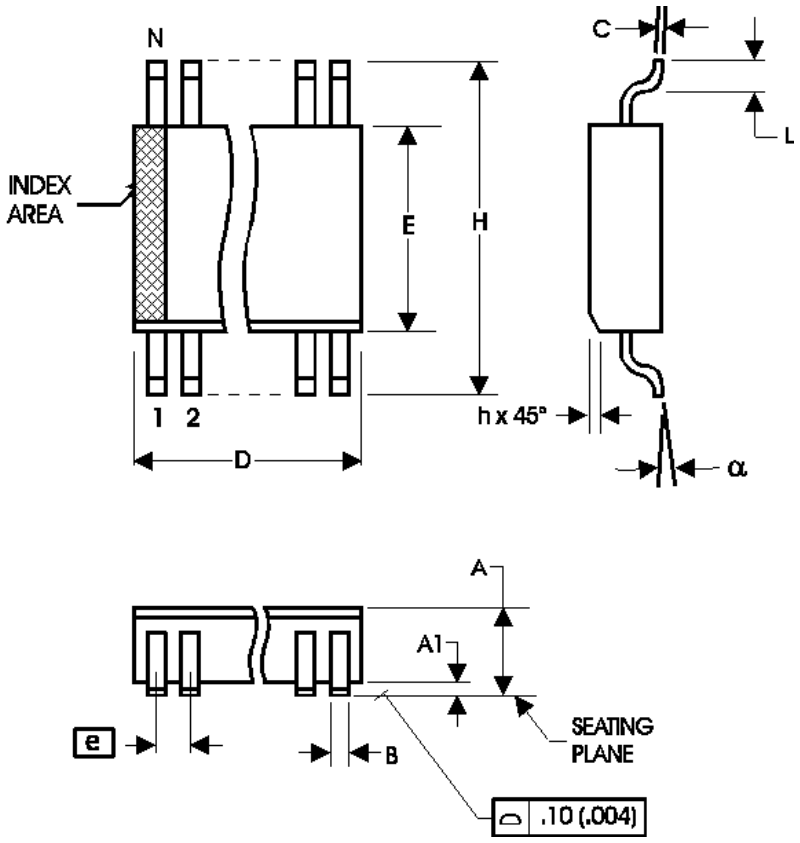


TABLE 6. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS83026AMI	83026AMI	8 Lead SOIC	96 per tube	-40°C to 85°C
ICS83026AMIT	83026AMI	8 Lead SOIC on Tape and Reel	2500	-40°C to 85°C
ICS83026AMILF	83026AIL	8 Lead "Lead-Free" SOIC	96 per tube	-40°C to 85°C
ICS83026AMILFT	83026AIL	8 Lead "Lead-Free" SOIC on Tape and Reel	2500	-40°C to 85°C

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REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A		1	Revised General Description.	8/9/02
B		1	Added Lead-Free bullet to Features section.	11/9/04
	T2	2	Pin Characteristics Table - changed C_{IN} from 4pF max. to 4pF typical and added 5Ω min. & 12Ω max. to R_{OUT} row.	
		6-7	Added Application Information section.	
	T7	11	Added Lead-Free P/N to Ordering Information table.	