FEMTOCLOCKS™ VCXO-PLL FREQUENCY GENERATOR FOR WIRELESS INFRASTRUCTURE EQUIPMENT

ICS813078I

General Description

The ICS813078I is a member of the HiperClocks family of high performance clock solutions from IDT. The ICS813078I a PLL based synchronous clock solution that is optimized for wireless infrastructure equipment where frequency translation and jitter attenuation is needed.

The device contains two internal PLL stages that are cascaded in series. The first PLL stage attenuates the reference clock jitter by using an internal or external VCXO circuit. The internal VCXO requires the connection of an external inexpensive pullable crystal (XTAL) to the ICS813078I. This first PLL stage (VCXO PLL) uses external passive loop filter components which are used to optimize the PLL loop bandwidth and damping characteristics for the given application. The output of the first stage VCXO PLL is a stable and jitter-tolerant 30.72MHz reference input for the second PLL stage. The second PLL stage provides frequency translation by multiplying the output of the first stage up to 491.52MHz or 614.4MHz. The low phase noise characteristics of the VCXO-PLL clock signal is maintained by the internal FemtoClock™PLL, which requires no external components or complex programming. Two independently configurable frequency dividers translate the internal VCO signal to the desired output frequencies. All frequency translation ratios are set by device configuration pins.

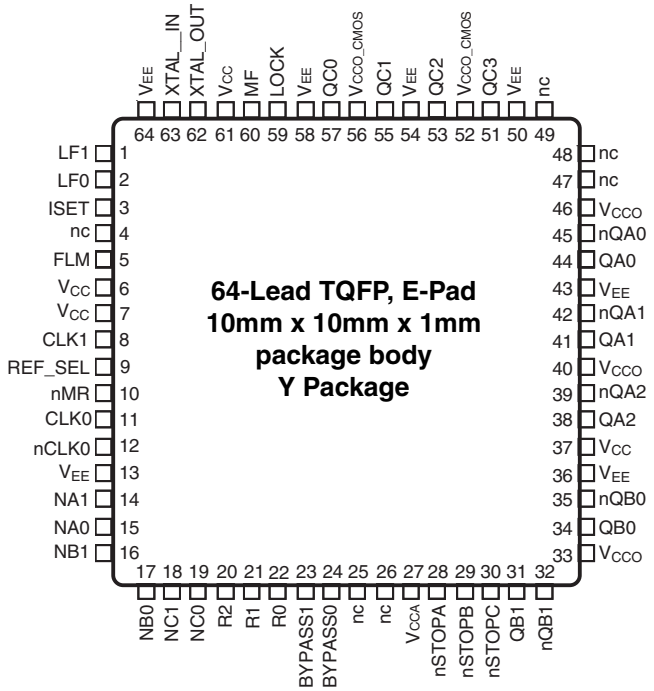
Supported input reference clock frequencies:
10MHz, 12.8MHz, 15MHz, 15.36MHz, 20MHz, 30.72MHz, 61.44MHz, and 122.88MHz

Supported output clock frequencies:
30.72MHz, 38.4MHz, 61.44MHz, 76.8MHz, 122.88MHz, 153.6MHz, 245.76MHz, 491.52MHz, and 614.4MHz

Features

- Nine outputs, organized in three independent output banks with differential LVPECL and single-ended outputs
- One differential input clock can accept the following differential input levels: LVDS, LVPECL, LVHSTL
- One single-ended clock input
- Frequency generation optimized for wireless infrastructure
- Attenuates the phase jitter of the input clock signal by using low-cost pullable fundamental mode crystal (XTAL)
- Internal Femtoclock frequency multiplier stage eliminates the need for an expensive external high frequency VCXO
- LVCMOS levels for all control I/O
- RMS phase jitter @ 122.88MHz, using a 30.72MHz crystal (12kHz to 20MHz): 1.1ps rms (typical)
- RMS phase jitter @ 61.44MHz, using a 30.72MHz crystal (12kHz to 20MHz): 0.97ps rms (typical)
- VCXO PLL bandwidth can be optimized for jitter attenuation and reference frequency tracking using external loop filter components
- PLL fast-lock control
- PLL lock detect output
- Absolute pull range is +/-50 ppm
- Full 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Pin Assignment



Block Diagram

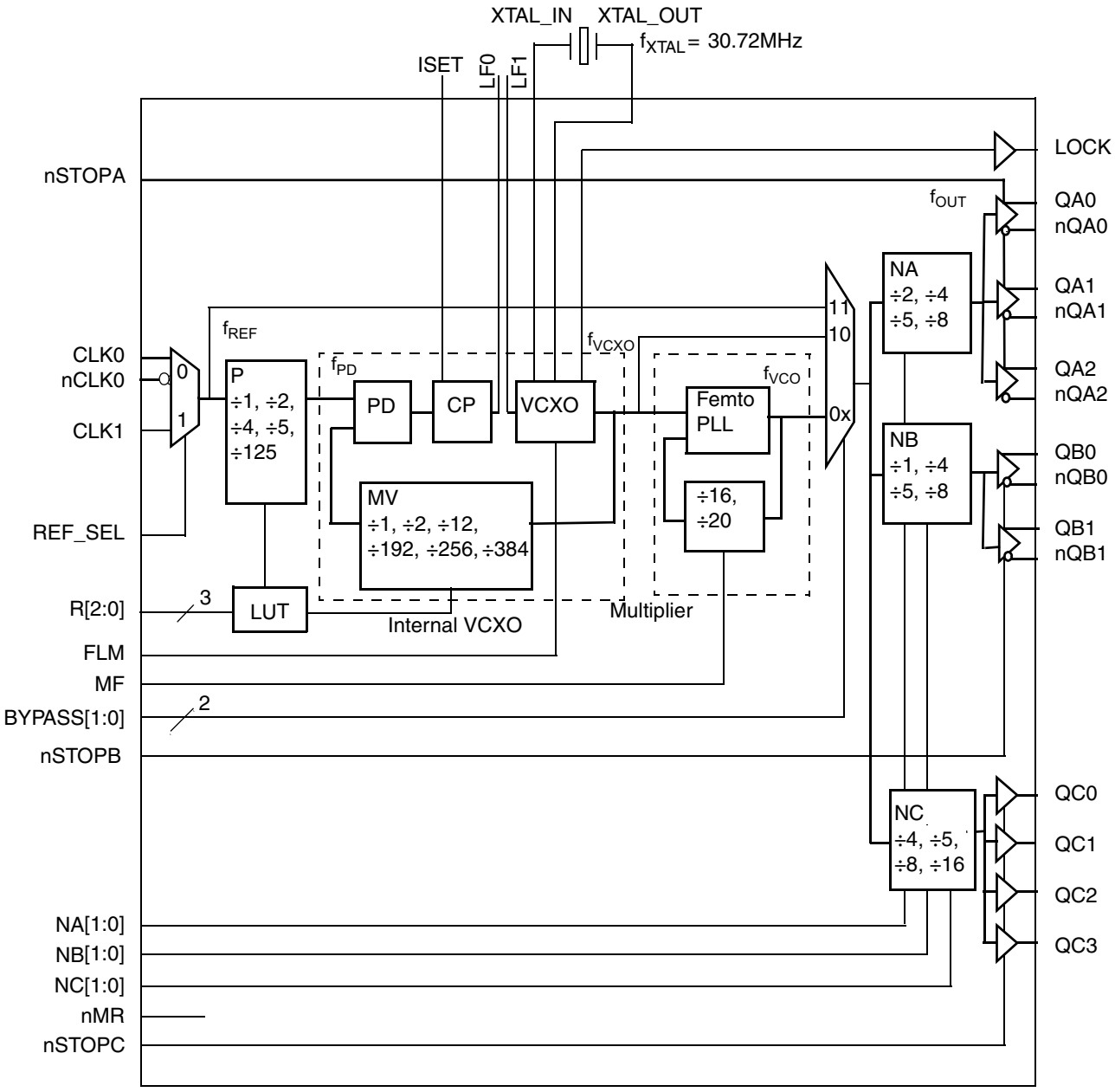


Table 1. Pin Descriptions

Number	Name	Type		Description
1	LF1	Analog Input		Input from external loop filter. VCXO control voltage input.
2	LF0	Analog Output		Output to external loop filter. Charge pump output.
3	ISET	Analog		Charge pump current-settings pin.
4, 25, 26, 47, 48, 49	nc	Unused		No connect.
5	FLM	Input	Pulldown	VCXO-PLL fast lock mode. See Table 3H. LVCMOS/LVTTL interface levels.
6, 7, 37, 61	V_{CC}	Power		Power supply pins for LVPECL outputs.
8	CLK1	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
9	REF_SEL	Input	Pulldown	Selects the input reference clock. See Table 3F. LVCMOS/LVTTL interface levels.
10	nMR	Input	Pullup	Master reset. See Table 3I. LVCMOS/LVTTL interface levels.
11	CLK0	Input	Pulldown	Non-inverting differential clock input.
12	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input.
13, 36, 43, 50, 54, 58, 64	V_{EE}	Power		Negative supply pins.
14. 15	NA1, NA0	Input	Pulldown	Femto-PLL output-divider for QAn/nQAn outputs. See Table 3B. LVCMOS/LVTTL interface levels.
16, 17	NB1, NB0	Input	Pulldown	Femto-PLL output-divider for QBn/nQBn outputs. See Table 3C. LVCMOS/LVTTL interface levels.
18, 19	NC1, NC0	Input	Pulldown	Femto-PLL output-divider for QCn outputs. See Table 3D. LVCMOS/LVTTL interface levels.
20, 21, 22	R2, R1, R0	Input	Pulldown	VCXO-PLL pre-divider and VCXO multiplier selection. See Table 3A. LVCMOS/LVTTL interface levels.
23, 24	BYPASS1, BYPASS0	Input	Pullup	PLL mode selections. See Table 3G. LVCMOS/LVTTL interface levels.
27	V_{CCA}	Power		Analog supply pin.
28	nSTOPA	Input	Pullup	Output clock stop for Bank A. See Table 3J. LVCMOS/LVTTL interface levels.
29	nSTOPB	Input	Pullup	Output clock stop for Bank B. See Table 3K. LVCMOS/LVTTL interface levels.
30	nSTOPC	Input	Pullup	Output clock stop for Bank C. See Table 3L. LVCMOS/LVTTL interface levels.
31, 32	QB1, nQB1	Output		Bank B output pair. LVPECL interface levels.
33, 40, 46	V_{CCO}	Power		Output supply pins for LVPECL outputs.
34, 35	QB0, nQB0	Output		Bank B output pair. LVPECL interface levels.
38, 39	QA2, nQA2	Output		Differential Bank A output pair. LVPECL interface levels.
41, 42	QA1, nQA1	Output		Differential Bank A output pair. LVPECL interface levels.
44, 45	QA0, nQA0	Output		Differential Bank A output pair. LVPECL interface levels.

continued on next page.

Number	Name	Type		Description
51, 53, 55, 57	QC3, QC2, QC1, QC0	Output		Single-ended Bank C outputs. LVCMOS/LVTTL interface levels.
52, 56	V_{CCO_CMOS}	Power		Output supply pins for LVCMOS outputs.
59	LOCK	Output		VCXO lock state. LVCMOS/LVTTL interface levels. See Table 3M.
60	MF	Input	Pulldown	FemtoClock-PLL feedback divider selection. See Table 3E. LVCMOS/LVTTL interface levels.
62, 63	XTAL_OUT, XTAL_IN	Input		Internal VCXO crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
C_{PD}	Power Dissipation Capacitance (per output)		V_{CC} = V_{CCO_CMOS} = 3.465V		10		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	QC[3:0]			15		Ω

Device Configuration

The ICS813078I is a two stage device, a VCXO-PLL stage followed by a low phase noise FemtoClock PLL multiplier stage. The VCXO-PLL stage uses a pullable crystal to lock to the reference clock. The low phase noise FemtoClock multiplies the VCXO-PLL output clock up to 491.52MHz or 614.4MHz and three independent output dividers scale the frequency down to the desired output frequencies. With a given input and VCXO frequency, the output frequency is a function of the P, MF, MV and the NA, NB and NC dividers. The P and MV are controlled by the R[2:0] control pins through the internal lookup table (LUT).

The VCXO-PLL pre-divider (P) down-scales the input reference frequency f_{REF} and enables the use of the ICS813078I at a variety of input frequencies. P and MV must be set to match the VCXO frequency: $f_{REF} \div P = f_{VCXO} \div MV$. For example, at the nominal VCXO frequency of 30.72MHz and if MV equals one, the input frequency must be an integer multiple of 30.72MHz (for MV = 2, the input frequency must be an integer multiple of 15.36MHz). The FemtoClock PLL stage multiplies the VCXO frequency (30.72MHz) to 614.4MHz or 491.52MHz by a multiplier MF of 20 or 16. The output frequency equals $[(f_{REF} \div P) * MV * MF] \div$ NA, NB, or NC. The NA, NB and NC dividers operate independently.

Table 3A. Input Frequency Configuration Example Table (fVCXO = 30.72MHz)

fref (MHz)	Input	Internal Dividers		fXTAL (MHz)
	R[2:0]	P	MV	
30.72	000	1	1	30.72
61.44	001	2	1	30.72
122.88	010	4	1	30.72
15.36	011	1	2	30.72
10	100	125	384	30.72
12.8	101	5	12	30.72
15	110	125	256	30.72
20	111	125	192	30.72

Table 3B. PLL Output-Divider (NA) Configuration Table.

Inputs		Output-Divider NA	Operation	QAn Output Frequency (MHz)	
NA1	NA0			MF = 0	MF = 1
0 (default)	0 (default)	2	$f_{QAn} = f_{VCO} \div 2$	245.76	307.2
0	1	4	$f_{QAn} = f_{VCO} \div 4$	122.88	153.6
1	0	5	$f_{QAn} = f_{VCO} \div 5$	98.304	122.88
1	1	8	$f_{QAn} = f_{VCO} \div 8$	61.44	76.8

Table 3C. PLL Output-Divider (NB) Configuration Table.

Inputs		Output-Divider NB	Operation	QBn Output Frequency (MHz)	
NB1	NB0			MF = 0	MF = 1
0 (default)	0 (default)	1	$f_{QBn} = f_{VCO} \div 1$	491.52	614.4
0	1	4	$f_{QBn} = f_{VCO} \div 4$	122.88	153.6
1	0	5	$f_{QBn} = f_{VCO} \div 5$	98.304	122.88
1	1	8	$f_{QBn} = f_{VCO} \div 8$	61.44	76.8

Table 3D. PLL Output-Divider (NC) Configuration Table.

Inputs		Output-Divider NC	Operation	QCn Output Frequency (MHz)	
NC1	NC0			MF = 0	MF = 1
0 (default)	0 (default)	4	$f_{QCn} = f_{VCO} \div 4$	122.08	153.6
0	1	5	$f_{QCn} = f_{VCO} \div 5$	98.304	122.88
1	0	8	$f_{QCn} = f_{VCO} \div 8$	61.44	76.8
1	1	16	$f_{QCn} = f_{VCO} \div 16$	30.72	38.4

Table 3E. Femtoclock PLL Feedback Divider (MF) Configuration Table (f_{XTAL} = 30.72MHz)

Input		
MF	Feedback Divider MF	Operation
0 (default)	16	$f_{VCO} = f_{VCXO}$ x 16 = 491.52MHz
1	20	$f_{VCO} = f_{VCXO}$ x 20 = 614.4MHz

Table 3F. Input Reference Clock Multiplexer (REF_SEL) Configuration Table

Input	
REF_SEL	**Operation**
0 (default)	Selects CLK0, nCLK0 differential input pair as reference frequency.
1	Selects CLK1 single-ended input as reference frequency.

The input reference selector should be tied to logic 0, selecting the differential clock inputs, for best signal integrity and lowest phase noise

Table 3G. PLL Bypass (BYPASS) Configuration Table

Input		
BYPASS1	**BYPASS0**	**Operation**
0	X	f_{OUT} = ((f_{REF} ÷ P) * MV * MF) ÷ NA, NB, or NC. VCXO-PLL operation, jitter attenuation and frequency multiplication enabled.
1	0	f_{OUT} = ((f_{REF} ÷ P) * MV) ÷ NA, NB, or NC. VCXO-PLL enabled, Femto-PLL bypassed. Jitter attenuation (VCXO-PLL) enabled. AC specifications do not apply.
1 (default)	1 (default)	f_{OUT} = f_{REF} ÷ NA, NB, or NC. VCXO-PLL and Femto-PLL bypassed, no jitter attenuation and frequency multiplication. AC specifications do not apply.

The BYPASS[1:0] controls should be set to logic LOW level for normal operation. BYPASS = 1x enables the PLL bypass mode for factory test. In PLL Bypass Mode, the output frequency is divided by NA, NB, or NC dividers.

Table 3H. Fast Lock Mode (FLM) Configuration Table

Input	
FLM	**Operation**
0 (default)	Normal operation.
1	Fast PLL lock operation. Use this mode only during startup to decrease PLL lock time.

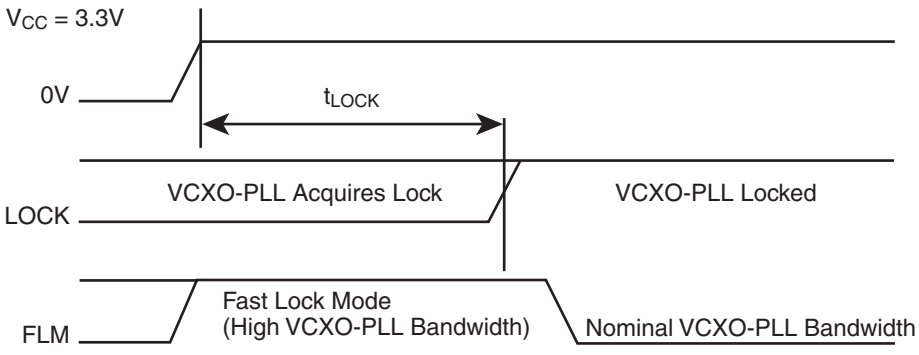


Figure 1. Recommended Start-up Timing Diagram

Table 3I. Reset (nMR) Configuration Table

Input	
nMR	**Operation**
0	The Femto-PLL is reset.
1 (default)	Normal operation.

Table 3J. Output Disable (nSTOPA) Configuration Table.

Input	
nSTOPA	**Operation**
0	QA[2:0]/nQA[2:0] outputs are stopped in logic LOW state. The assertion of nSTOPA is asynchronous to the internal clock signal and may cause an output runt pulse.
1 (default)	Normal operation and outputs enabled.

Table 3K. Output Disable (nSTOPB) Configuration Table.

Input	
nSTOPB	**Operation**
0	QB[1:0] / nQB[1:0] outputs are stopped in logic LOW state. The assertion of nSTOPB is asynchronous to the internal clock signal and may cause an output runt pulse.
1 (default)	Normal operation and outputs enabled.

Table 3L. Output Disable (nSTOPC) Configuration Table.

Input	
nSTOPC	**Operation**
0	QC[3:0] outputs are stopped in logic LOW state. The assertion of nSTOPC is asynchronous to the internal clock signal and may cause an output runt pulse.
1 (default)	Normal operation and outputs enabled.

Table 3M. PLL Lock Status Output (LOCK_DT) Configuration Table.

	Output
Conditions	**LOCK_DT**
Locked	Constantly HIGH.
Unlocked	HIGH with occasional LOW pulses.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current Outputs, V_O (LVCMOS)	 50mA 100mA -0.5V to V_{CCO_CMOS}+ 0.5V
Package Thermal Impedance, θ_{JA}	31.8°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO} = V_{CCO_CMOS} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.15	3.3	V_{CC}	V
V_{CCO}, V_{CCO_CMOS}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				260	mA
I_{CCA}	Analog Supply Current				15	mA
I_{CCO_CMOS}	Output Supply Current				6	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO_CMOS} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK1, REF_SEL, MF, FLM, NA[1:0], NB[1:0], NC[1:0], R[2:0]	$V_{CC} = V_{IN} = 3.465V$			150	µA
		nSTOP[A:C], BYPASS[1:0], nMR	$V_{CC} = V_{IN} = 3.465V$			10	µA
I_{IL}	Input Low Current	CLK1, REF_SEL, MF, FLM, NA[1:0], NB[1:0], NC[1:0], R[2:0]	V_{CC} = 3.465V, V_{IN} = 0V	-10			µA
		nSTOP[A:C], BYPASS[1:0], nMR	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage	QC0:QC3	I_{OH} = -12mA	2.6			V
V_{OL}	Output Low Voltage	QC0:QC3	I_{OL} = 12mA			0.5	V

Table 4C. Differential DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, nCLK0	$V_{CC} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	CLK0	V_{CC} = 3.465V, V_{IN} = 0V	-10			µA
		nCLK0	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4D. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} – 1.4		V_{CCO} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} – 2.0		V_{CCO} – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to V_{CCO} – 2V.

AC Electrical Characteristics

Table 5. AC Characteristics, $V_{CC} = V_{CCO} = V_{CCO_CMOS} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Reference Frequency		R=000	30.72MHz–50ppm		30.72MHz+50ppm	
			R=001	61.44MHz–50ppm		61.44MHz+50ppm	
			R=010	122.88MHz–50ppm		122.88MHz+50ppm	
			R=011	15.36MHz–50ppm		15.36MHz+50ppm	
			R=100	10MHz–50ppm		10MHz+50ppm	
			R=101	12.88MHz–50ppm		12.88MHz+50ppm	
			R=110	15MHz–50ppm		15MHz+50ppm	
			R=111	20MHz–50ppm		20MHz+50ppm	
f_{OUT}	Output Frequency		MF=0, N=1		491.52		MHz
			MF=0, N=2		245.76		MHz
			MF=0, N=4		122.88		MHz
			MF=0, N=5		98.304		MHz
			MF=0, N=8		61.44		MHz
			MF=0, N=16		30.72		MHz
			MF=1, N=1		614.4		MHz
			MF=1, N=2		307.2		MHz
			MF=1, N=4		153.6		MHz
			MF=1, N=5		122.88		MHz
			MF=1, N=8		76.8		MHz
			MF=1, N=16		38.4		MHz
f_{VCXO}	VCXO-PLL VCO Lock Range			30.72MHz–50ppm		30.72MHz+50ppm	
f_{VCO}	Femto-PLL VCO Lock Range				491.52, 614.4		MHz
tjit(Ø)	RMS Phase Jitter Integration Range: 12kHz - 20MHz; NOTE 1	QBn	491.52MHz		1.03		ps
		QAn, QBn	153.6MHz, MF=20		0.92		ps
		QAn, QBn	122.88MHz, MF=20		1.1		ps
		QAn, QBn	122.88MHz, MF=16		1.1		ps
		QAn, QBn	61.44MHz, MF=16		0.97		ps
tjit(per)	Period Jitter	QAn QBn	153.6MHz, QCn = off 122.88MHz, QCn = off			35	ps
		QAn, QBn	122.88MHz, QCn = off			30	ps
Φ_N	Single-Side Band Noise at: QAn =122.88MHz	10Hz offset	30.72MHz XTAL, f_{ref} = 30.72MHz, QBn and QCn = 122.88MHz		-41.3		dBc/Hz
		100Hz offset			-71.5		dBc/Hz
		1kHz offset			-100.7		dBc/Hz
		10kHz offset			-127.2		dBc/Hz
		100kHz offset			-128.2		dBc/Hz
		1MHz offset			-131.4		dBc/Hz

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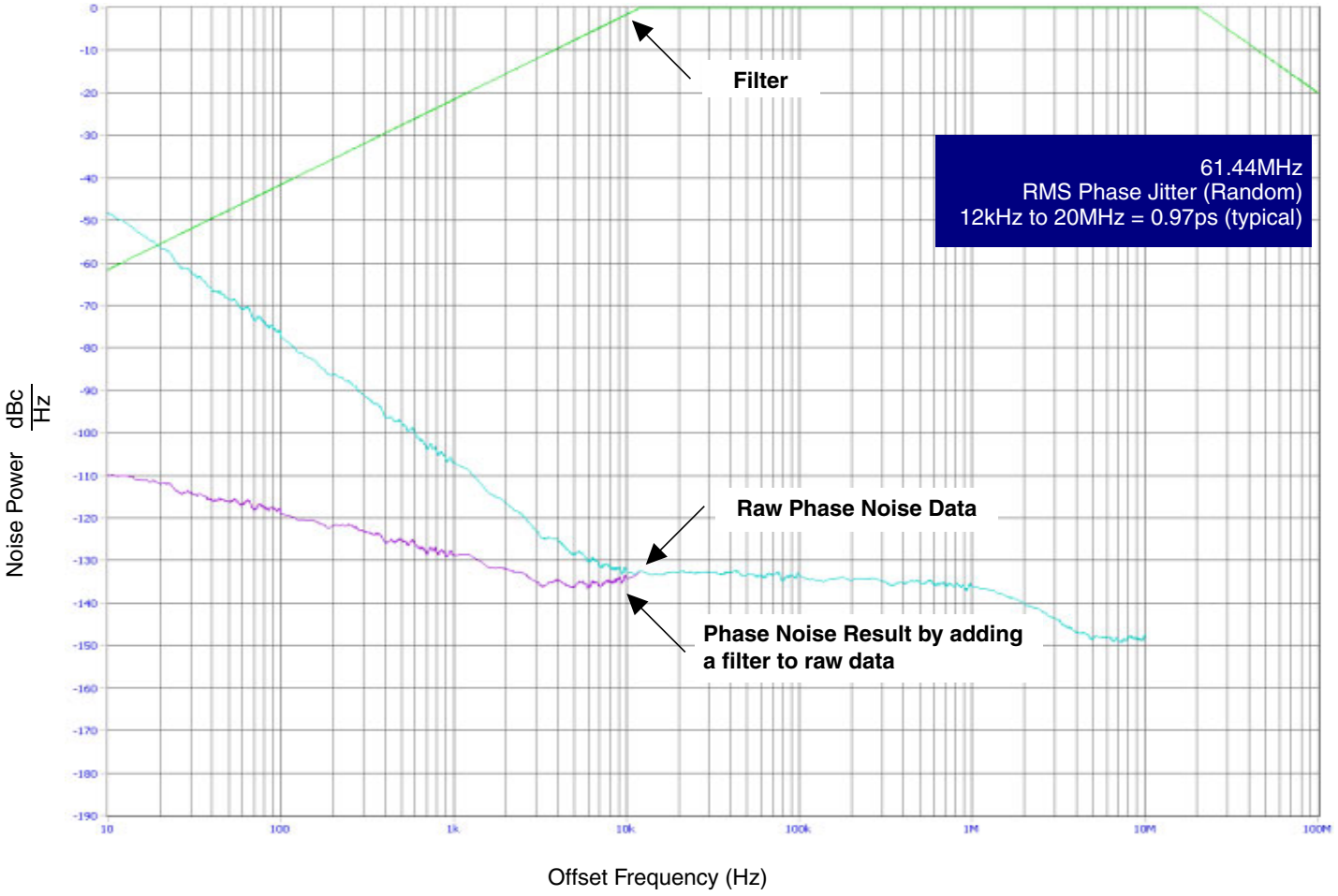
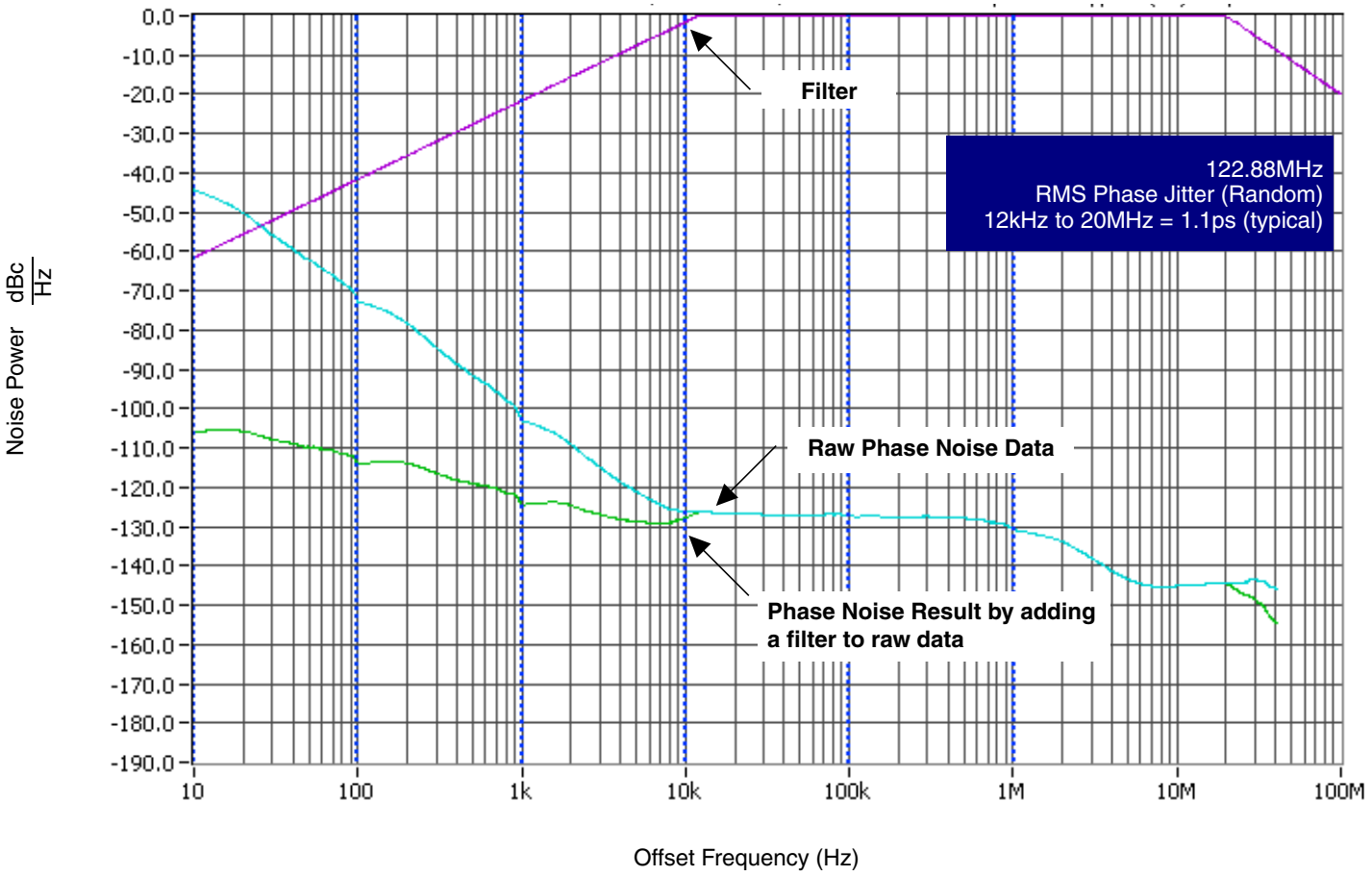
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
Φ_N	Single-Side Band Noise at: QAn = 61.44MHz	10Hz offset	30.72MHz XTAL, f_{ref} = 30.72MHz, QBn and QCn = 61.44MHz		-44.6		dBc/Hz
		100Hz offset			-77.2		dBc/Hz
		1kHz offset			-106.4		dBc/Hz
		10kHz offset			-132.8		dBc/Hz
		100kHz offset			-132.9		dBc/Hz
		1MHz offset			-137.9		dBc/Hz
tsk(o)	Output Skew NOTE 2, 3	$f_{QA} = f_{QB}$	across QAn and QBn			200	ps
		$f_{QA} \neq f_{QB}$	across QAn and QBn			300	ps
tsk(b)	Bank Skew; NOTE 2, 4	QAn/nQAn				50	ps
		QBn/nQBn				50	ps
		QCn				65	ps
t_R / t_F	Output Rise/ Fall Time	QAn/nQAn	20% to 80%	100		600	ps
		QBn/nQBn	20% to 80%	100		600	ps
		QCn	20% to 80%	350		1050	ps
odc	Output Duty Cycle	QAn/nQAn		47		53	%
		QBn/nQBn	N ≠ 1	47		53	%
		QBn/nQBn	N = 1	43		57	%
		QCn		45		55	%

NOTE: T_A, Ambient Temperature applied using forced air flow.
NOTE 1: Phase jitter measured using a 30.72MHz quartz crystal.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 4: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

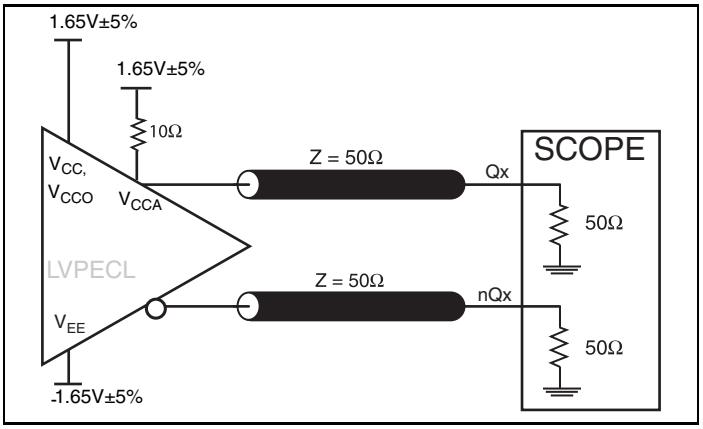
Typical Phase Noise at 61.44MHz



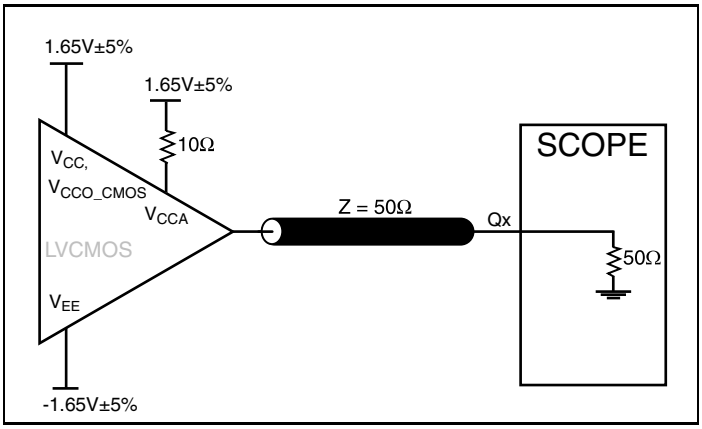
Typical Phase Noise at 122.88MHz



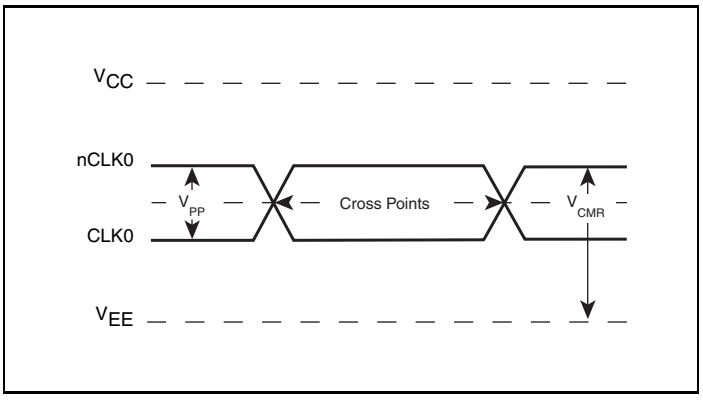
Parameter Measurement Information



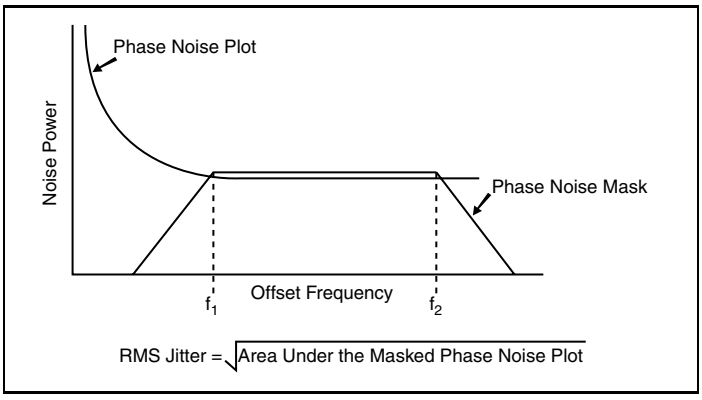
3.3V LVPECL Output Load AC Test Circuit



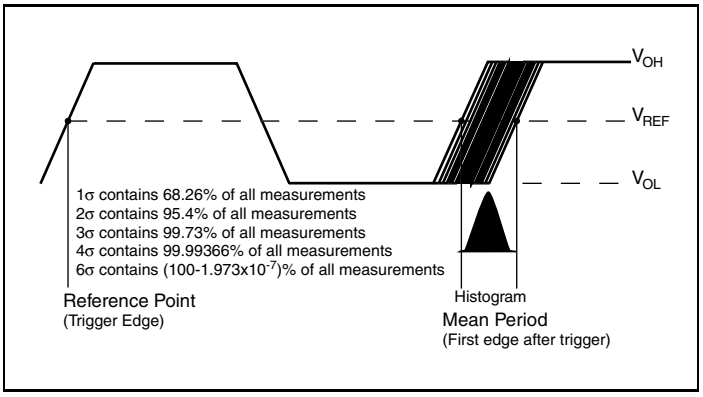
3.3V LVCMOS Output Load AC Test Circuit



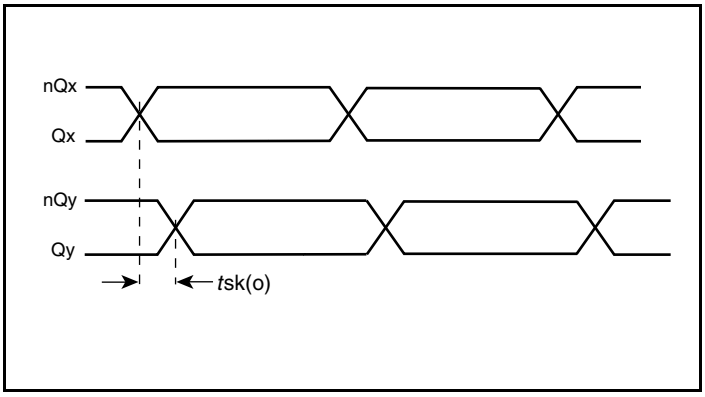
Differential Input Level



RMS Phase Jitter

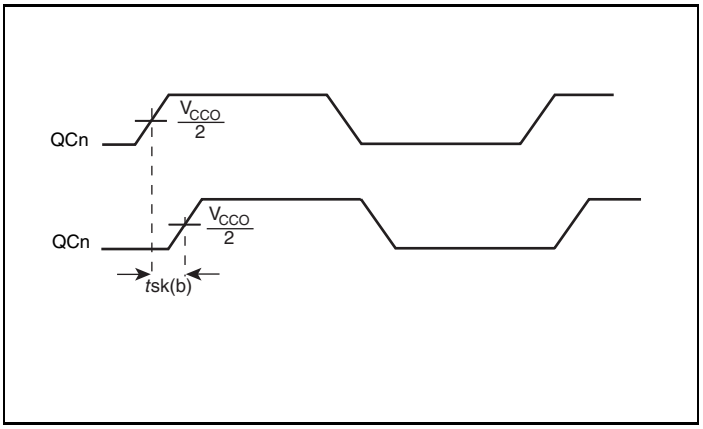


Period Jitter

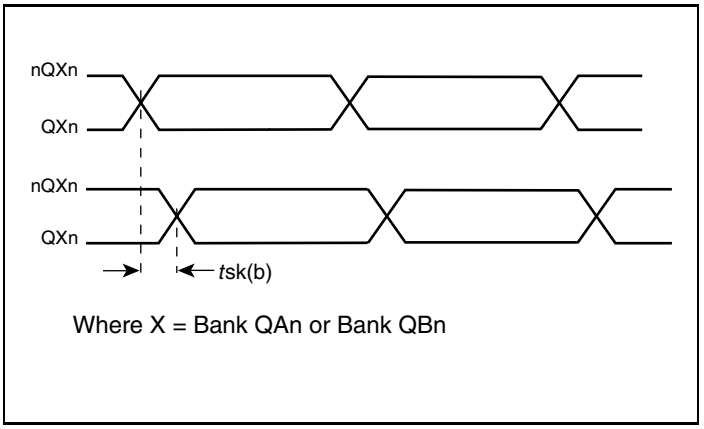


Differential Output Skew

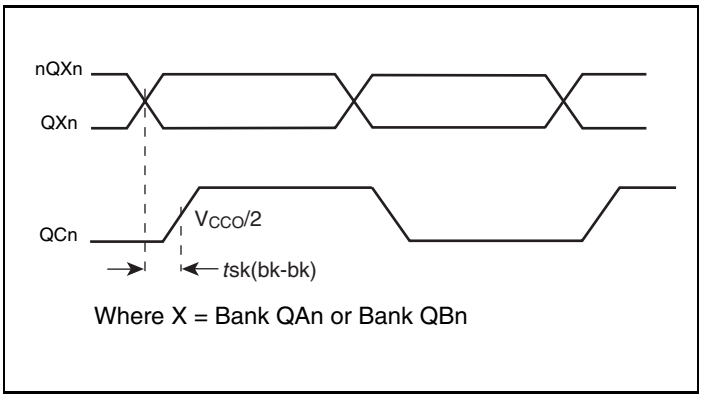
Parameter Measurement Information, continued



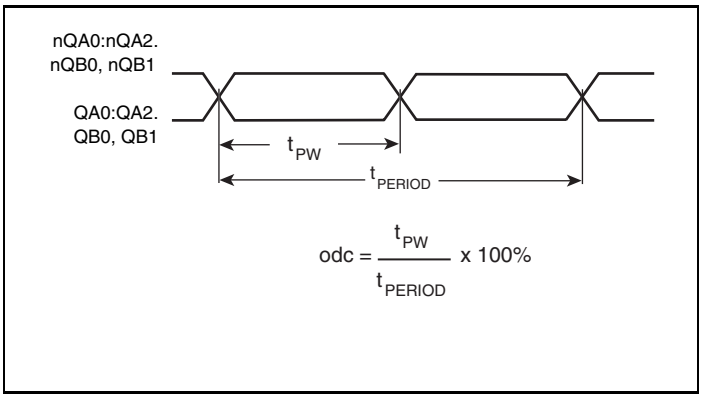
LVCMOS Bank Skew



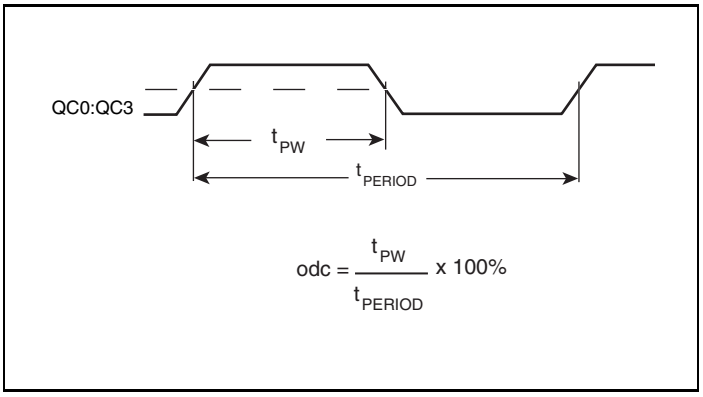
Differential Bank Skew



Output Rise/Fall Time



Differential Output Duty Cycle/Pulse Width/Period



LVCMOS Output Duty Cycle/Pulse Width/Period

Application Information

VCXO-PLL External Components

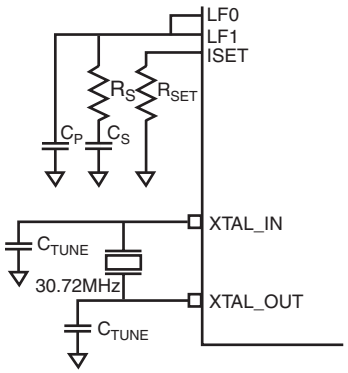
Choosing the correct external components and having a proper printed circuit board (PCB) layout is a key task for quality operation of the VCXO-PLL. In choosing a crystal, special precaution must be taken with the package and load capacitance (C_L). In addition, frequency, accuracy and temperature range must also be considered. Since the pulling range of a crystal also varies with the package, it is recommended that a metal-canned package like HC49 be used. Generally, a metal-canned package has a larger pulling range than a surface mounted device (SMD). For crystal selection information, refer to the *VCXO Crystal Selection Application Note.*

The crystal's load capacitance C_L characteristic determines its resonating frequency and is closely related to the VCXO tuning range. The total external capacitance seen by the crystal when installed on a board is the sum of the stray board capacitance, IC package lead capacitance, internal varactor capacitance and any installed tuning capacitors (C_{TUNE}).

If the crystal C_L is greater than the total external capacitance, the VCXO will oscillate at a higher frequency than the crystal specification. If the crystal C_L is lower than the total external capacitance, the VCXO will oscillate at a lower frequency than the crystal specification. In either case, the absolute tuning range is reduced. The correct value of C_L is dependant on the characteristics of the VCXO. The recommended C_L in the Crystal Parameter Table balances the tuning range by centering the tuning curve.

The *VCXO-PLL Loop Bandwidth Selection Table* shows R_S, C_S and C_P values for recommended high, mid and low loop bandwidth configurations. The device has been characterized using these parameters. For other configurations, refer to the *Loop Filter Component Selection for VCXO Based PLLs Application Note.*

The crystal and external loop filter components should be kept as close as possible to the device. Loop filter and crystal traces should be kept short and separated from each other. Other signal traces should be kept separate and not run underneath the device, loop filter or crystal components.



VCXO Characteristics Table

Symbol	Parameter	Typical	Units
k_{VCXO}	VCXO Gain	9.3	kHz/V
C_{V_LOW}	Low Varactor Capacitance	14.7	pF
C_{V_HIGH}	High Varactor Capacitance	7.5	pF

VCXO-PLL Loop Bandwidth Selection Table

Bandwidth	Crystal Frequency (MHz)	MV	R_S (kΩ)	C_S (µF)	C_P (µF)	R_{SET} (kΩ)
8.5Hz (Low)	30.72	384	20	10	0.1	10
85Hz (Mid)	30.72	192	20	10	0.01	2.0
22.2kHz (High)	30.72	1	30	0.01	0.00001	2.2

Crystal Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
	Mode of Oscillation			Fundamental		
f_N	Frequency			30.72		MHz
f_T	Frequency Tolerance				±20	ppm
f_S	Frequency Stability				±20	ppm
	Operating Temperature Range		-40		+85	^{0}C
C_L	Load Capacitance			10		pF
C_O	Shunt Capacitance			4		pF
C_O / C_1	Pullability Ratio			220	240	
ESR	Equivalent Series Resistance				20	Ω
	Drive Level				1	mW
	Aging @ 25 ^{0}C				±3 per year	ppm

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

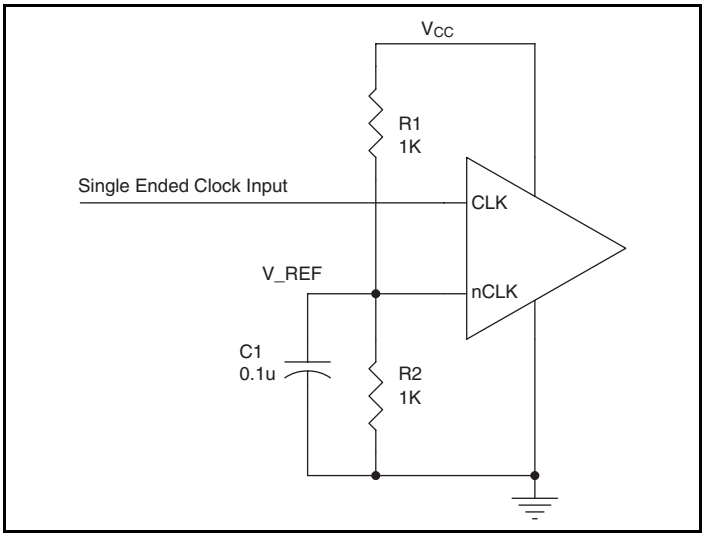


Figure 2. Single-Ended Signal Driving Differential Input

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS813078I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, V_{CCO} and V_{CCO_CMOS} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 3* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

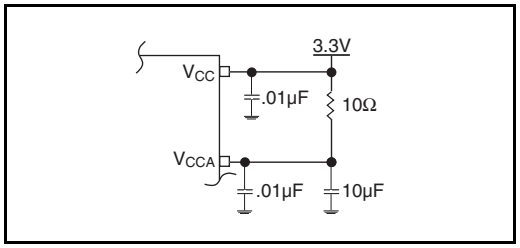


Figure 3. Power Supply Filtering

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 4A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

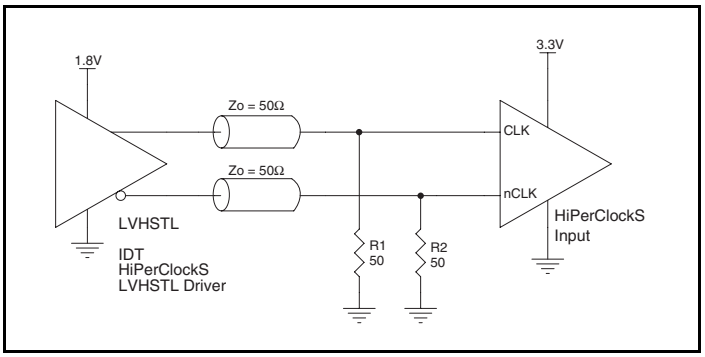


Figure 4A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

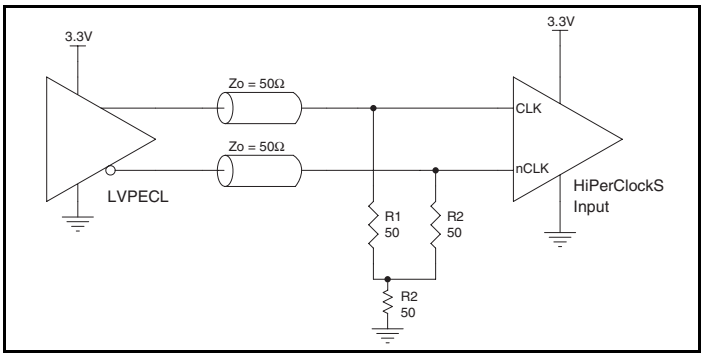


Figure 4B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

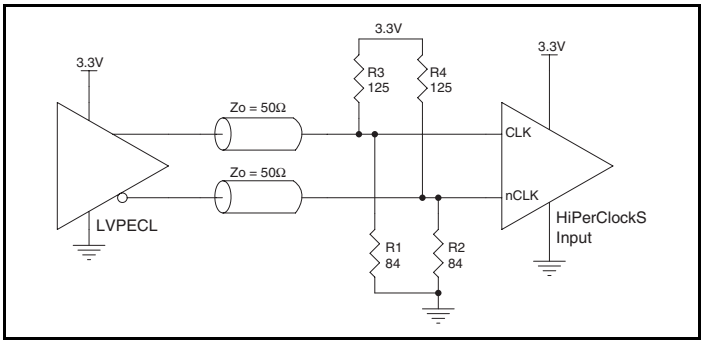


Figure 4C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

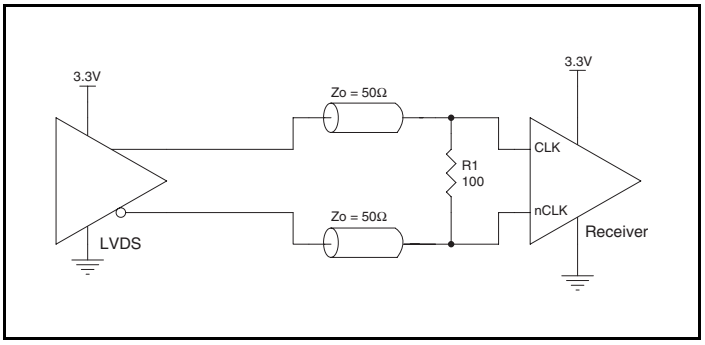


Figure 4D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

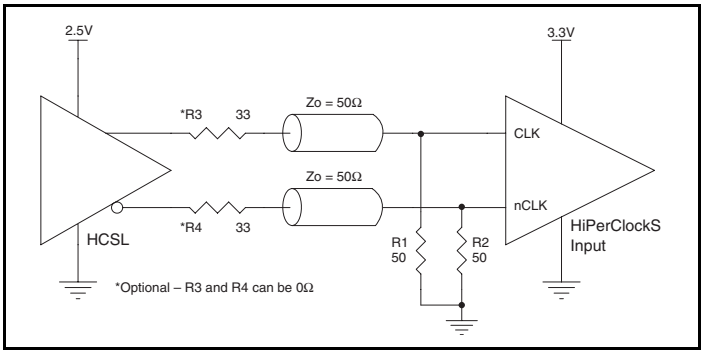


Figure 4E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

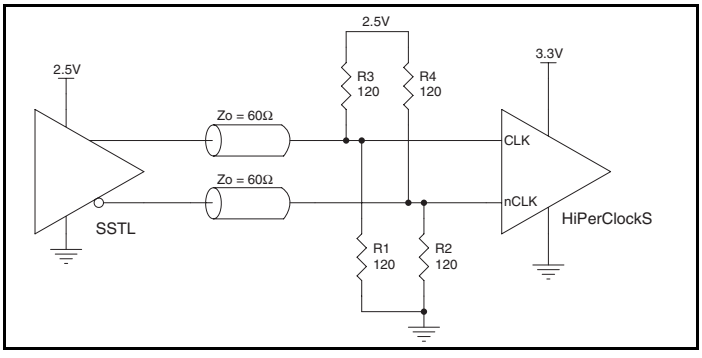


Figure 4F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

CLK Input

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50W transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

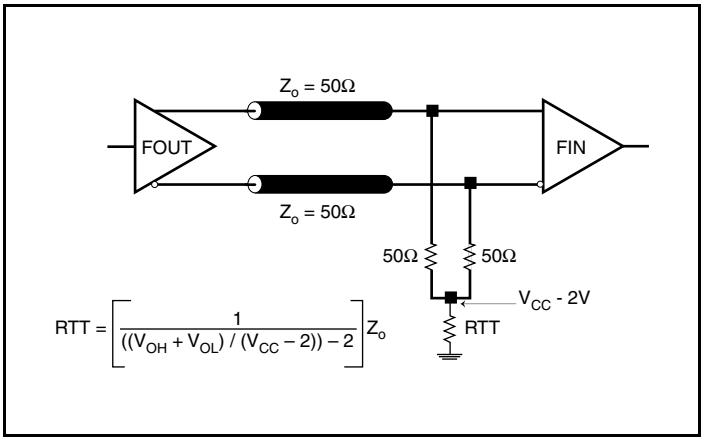


Figure 5A. 3.3V LVPECL Output Termination

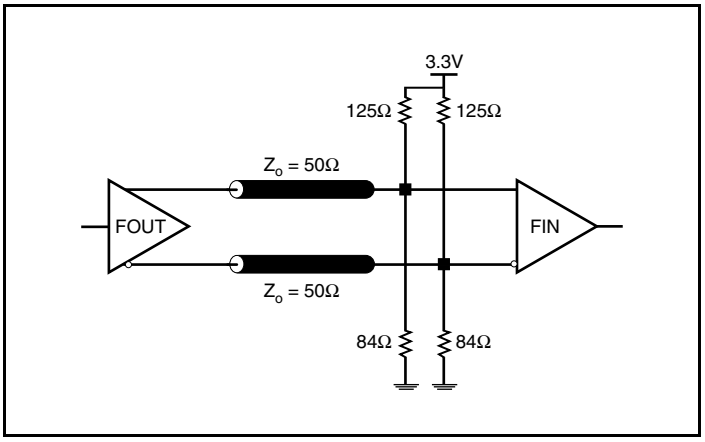


Figure 5B. 3.3V LVPECL Output Termination

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

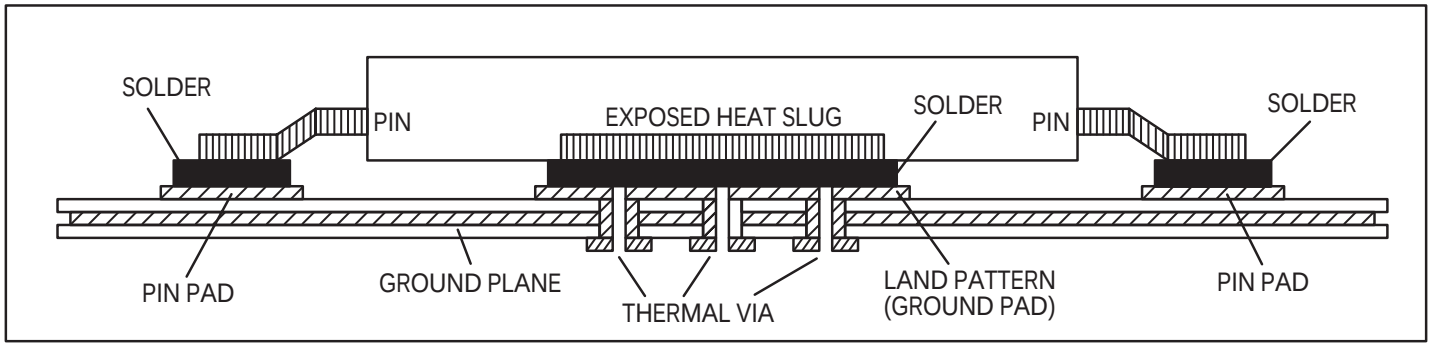


Figure 6. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS813078I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS813078I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

Core and LVPECL Output Power Dissipation

- Power (core)$_{_MAX}$ = V_{CC_MAX} *I_{EE_MAX} = 3.465V * 260mA = **900.9mW**

Power (output)$_{_MAX}$ = **30mW/Loaded Output Pair**
If all outputs are loaded, the total power is 5 * 30mW = **150mW**

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to V_{CCO}/2
  Output Current I_{OUT} = V_{CCO_MAX} / [2 * (50Ω + R_{OUT})] = 3.465V / [2 * (50Ω + 15Ω)] = **26.7mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (R_{OUT}) = R_{OUT} * (I_{OUT})^2 = 15Ω * (26.7mA)^2 = **10.7mW per output**
- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT}) = 10.7mW * 4 = **42.8mW**
- Dynamic Power Dissipation at 153.6MHz
  Power (25MHz) = C_{PD} * Frequency * (V_{CCO})^2 = 10pF * 153.6MHz * (3.465V)^2 = **18mW per output**
  Total Power (153.6MHz) = **18mW * 4 = 72mW**

Total Power Dissipation

- **Total Power**
  = Power (core) + Power (LVPECL output) + Total Power (R_{OUT}) + Total Power (153.6MHz)
  = 900.9mW + 150mW + 42.8mW + 72mW
  = 1165.7mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 31.8°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.166W * 31.8°C/W = 122.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 64 Lead TQFP, E-Pad Forced Convection

θ_{JA} **Vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	31.8°C/W	25.8°C/W	24.2°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 64 Lead TQFP, E-Pad

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	31.8°C/W	25.8°C/W	24.2°C/W

Transistor Count

The transistor count for ICS813078I is: 6235

Package Outline and Package Dimensions

Package Outline - Y Suffix for 64 Lead TQFP, E-Pad

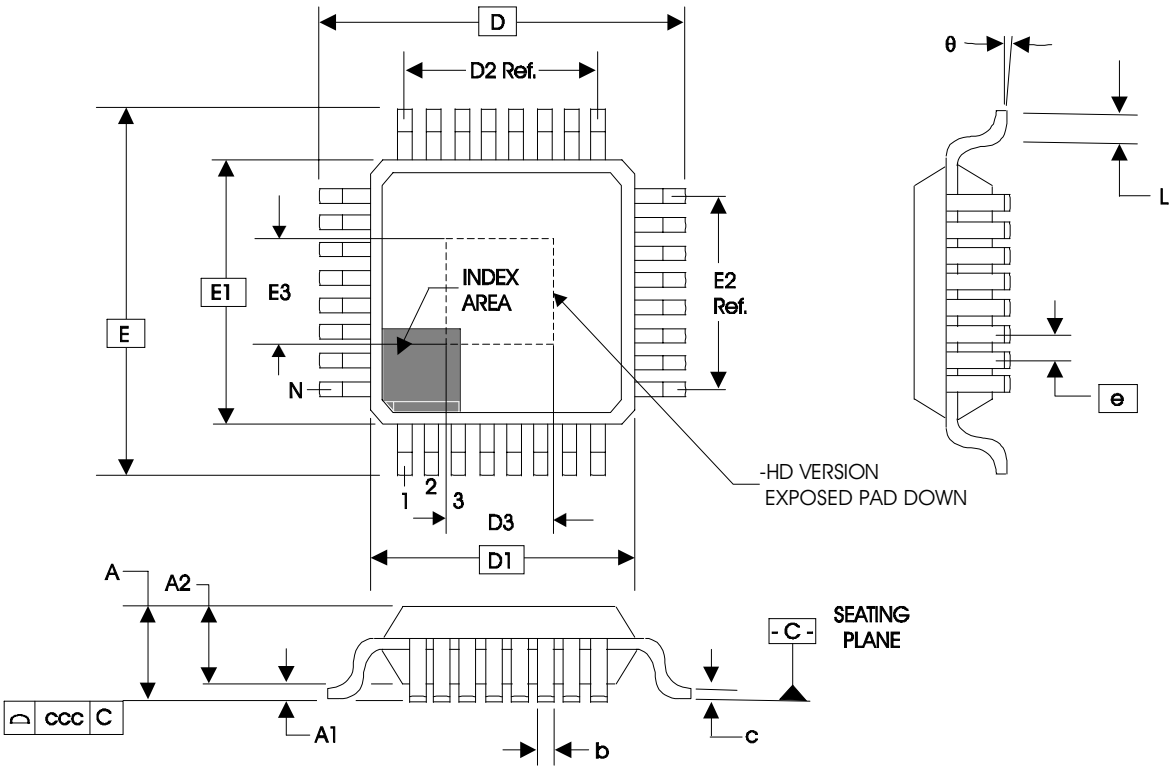


Table 8. Package Dimensions for 64 Lead TQFP, E-Pad

JEDEC Variation: ACD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		64	
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09		0.20
D & E		12.00 Basic	
D1 & E1		10.00 Basic	
D2 & E2		7.50 Ref.	
D3 & E3	4.5	5.0	5.5
e		0.50 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.08

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
813078BYILF	ICS813078BYILF	“Lead-Free” 64 Lead TQFP, E-Pad	Tray	-40°C to +85°C
813078BYILFT	ICS813078BYILF	“Lead-Free” 64 Lead TQFP, E-Pad	500 Tape & Reel	-40°C to +85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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