# ICS651-03

## VOIP Clock Source

## Description

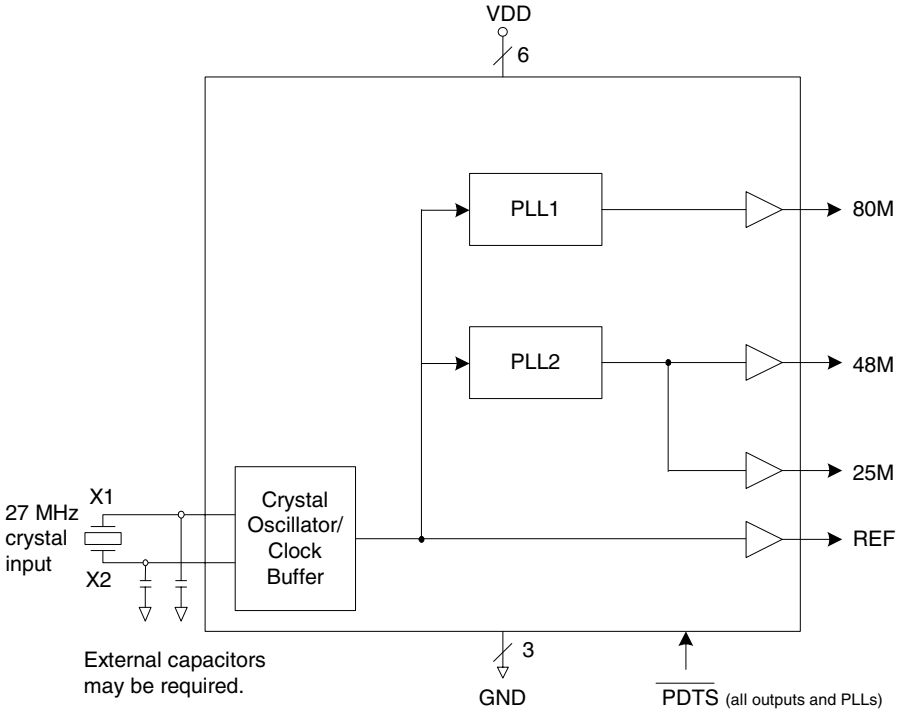
The ICS651-03 is a low cost frequency generator designed to support voice-over-internet protocol (VOIP) applications. Using analog/digital Phase-Locked Loop (PLL) techniques, the device uses a standard fundamental mode, inexpensive crystal input to produce four output clocks supporting DSP, video encoder, and memory functions. To form a complete VOIP clocking solution use the ICS651-02 companion device.

The device also has a power down feature that tri-states the clock outputs and turns off the PLL when the $\overline{\text{PDTS}}$ pin is taken low.

## Features

- Packaged in 16-pin TSSOP
- Replaces multiple crystals and oscillators
- Input crystal or clock frequency of 27 MHz
- Fixed reference output frequency of 80 MHz
- Fixed output frequency of 48 MHz
- Fixed output frequency of 25 MHz
- Reference output frequency of 27 MHz
- Duty cycle of 40/60
- Operating voltage of 3.3 V
- Advanced, low power CMOS process

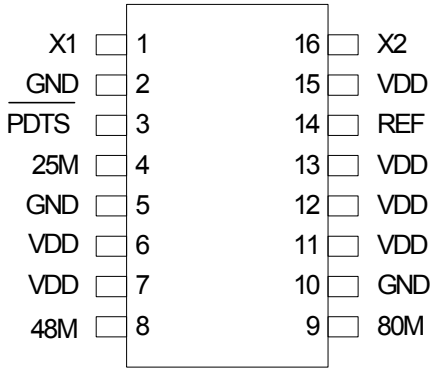
## Block Diagram






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## Pin Assignment




16-pin (173 mil) TSSOP

## Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1 | X1 | Input | Crystal connection. Connect to 27 MHz crystal input. |
| 2 | GND | Power | Connect to ground. |
| 3 | $\overline{\text{PDTS}}$ | Input | Powers down entire chip and tri-states outputs when low. Internal pull-up resistor. |
| 4 | 25M | Output | 25 MHz clock output. Weak internal pull-down when tri-state. |
| 5 | GND | Power | Connect to ground. |
| 6 | VDD | Power | Connect to +3.3 V. |
| 7 | VDD | Power | Connect to +3.3 V. |
| 8 | 48M | Output | 48 MHz clock output. Weak internal pull down when tri-state. |
| 9 | 80M | Output | 80 MHz clock output. Weak internal pull down when tri-state. |
| 10 | GND | Power | Connect to ground. |
| 11 | VDD | Power | Connect to +3.3 V. |
| 12 | VDD | Power | Connect to +3.3 V. |
| 13 | VDD | Power | Connect to +3.3 V. |
| 14 | REF | Output | Reference 27 MHz output. Weak internal pull-down when tri-state. |
| 15 | VDD | Power | Connect to +3.3 V. |
| 16 | X2 | Output | Crystal connection. Connect to 27 MHz crystal input. |

# External Components

## Decoupling Capacitor

As with any high performance mixed-signal IC, the ICS651-03 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between each VDD and the PCB ground plane.

## Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

## Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal ($C_L$ -6 pF)*2. In this equation, $C_L$= crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF [(16-6) x 2] = 20.

## PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitors should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pins should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) Place the 33Ω series termination resistor (if needed) close to the clock output to minimize EMI.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS651-03. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.



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## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS651-03. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|---|---|
| Supply Voltage, VDD | -0.5 V to 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | 0 to +70°C |
| Storage Temperature | -65 to +150°C |
| Junction Temperature | 175°C |
| Soldering Temperature | 260°C |

## Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Ambient Operating Temperature | 0 | | +70 | °C |
| Power Supply Voltage (measured in respect to GND) | +3.135 | +3.3 | +3.465 | V |

## DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3V ±5%**, Ambient Temperature 0 to +70°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | | 3.135 | 3.3 | 3.465 | V |
| Supply Current | IDD | No load, $\overline{PDTS}$=1 | | 21 | | mA |
| Power Down Current | IDDPD | No load, $\overline{PDTS}$=0 | | 90 | | µA |
| Input High Voltage | $V_{IH}$ | $\overline{PDTS}$ | 2 | | | V |
| Input Low Voltage | $V_{IL}$ | $\overline{PDTS}$ | | | 0.8 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -4 mA | VDD-0.4 | | | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -12 mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 12 mA | | | 0.4 | V |
| Short Circuit Current | $I_{OS}$ | Clock outputs | | ±70 | | mA |
| Input Capacitance, inputs | $C_{IN}$ | | | 5 | | pF |

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Nominal Output Impedance | $Z_{OUT}$ | | | 20 | | Ω |
| Internal pull-up resistor | $R_{PU}$ | $\overline{PDTS}$ pins | | 700 | | kΩ |
| Internal pull-down resistor | $R_{PD}$ | | | 200 | | kΩ |

## AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3V ±5%**, Ambient Temperature 0 to +70°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Input Frequency | $f_{IN}$ | | | 27 | | MHz |
| Output Rise Time | $t_{OR}$ | 20% to 80% (Note 1) | | 1.0 | | ns |
| Output Fall Time | $t_{OF}$ | 80% to 20% (Note 1) | | 1.0 | | ns |
| Output Clock Duty Cycle | | at VDD/2 (Note 1) | 40 | | 60 | % |
| Absolute Clock Period Jitter | | (Note 1) | | ± 100 | | ps |
| Frequency synthesis error | | | | 0 | | ppm |
| Output Enable Time | $t_{OE}$ | $\overline{PDTS}$ high to output locked to ±1% | | 250 | | µs |
| Output Disable Time | $t_{OD}$ | $\overline{PDTS}$ low to tri-state | | 20 | | ns |

Note 1: Measured with a 15 pF load.

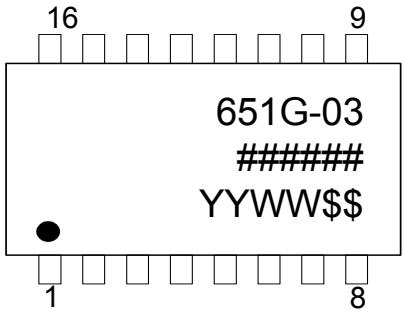


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## Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air | | 78 | | °C/W |
| | $\theta_{JA}$ | 1 m/s air flow | | 70 | | °C/W |
| | $\theta_{JA}$ | 3 m/s air flow | | 68 | | °C/W |
| Thermal Resistance Junction to Case | $\theta_{JC}$ | | | 37 | | °C/W |

## Marking Diagram




Notes:

1. ###### is the lot code.

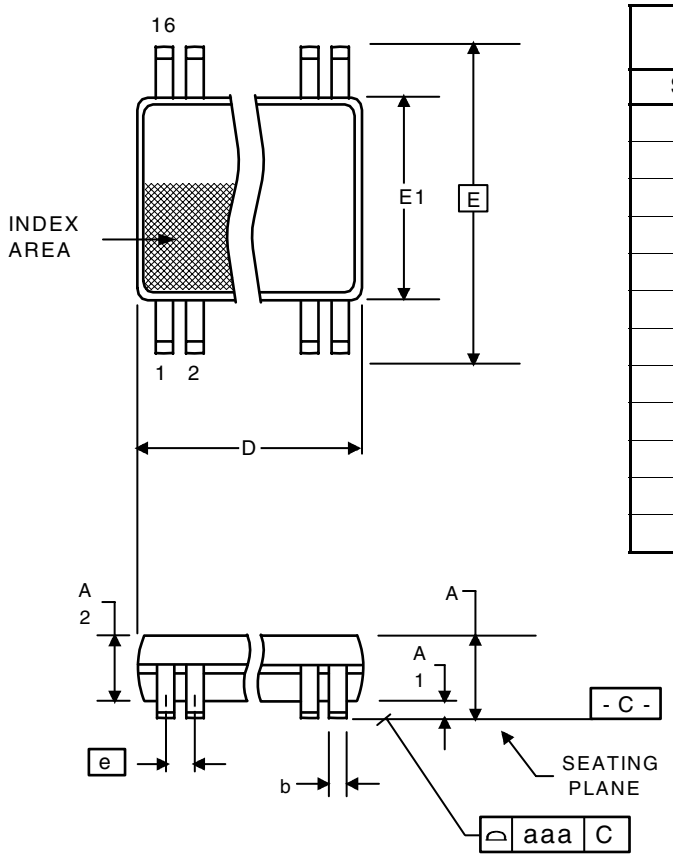
2. YYWW is the last two digits of the year, and the week number that the part was assembled.



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## Package Outline and Package Dimensions (16-pin TSSOP, 173 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95




| | Millimeters | | Inches | |
|---|---|---|---|---|
| **Symbol** | **Min** | **Max** | **Min** | **Max** |
| A | -- | 1.20 | -- | 0.047 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 0.80 | 1.05 | 0.032 | 0.041 |
| b | 0.19 | 0.30 | 0.007 | 0.012 |
| C | 0.09 | 0.20 | 0.0035 | 0.008 |
| D | 4.90 | 5.1 | 0.193 | 0.201 |
| E | 6.40 BASIC | | 0.252 BASIC | |
| E1 | 4.30 | 4.50 | 0.169 | 0.177 |
| e | 0.65 Basic | | 0.0256 Basic | |
| L | 0.45 | 0.75 | 0.018 | 0.030 |
| $\alpha$ | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | 0.004 |

## Ordering Information

| Part / Order Number | Marking (both) | Shipping packaging | Package | Temperature |
|---|---|---|---|---|
| ICS651G-03 | (see gage 6) | Tubes | 16-pin TSSOP | 0 to +70 °C |
| ICS651G-03T | | Tape and Reel | 16-pin TSSOP | 0 to +70 °C |

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