SPREAD SPECTRUM CLOCK SYNTHESIZER ICS650-41

Description

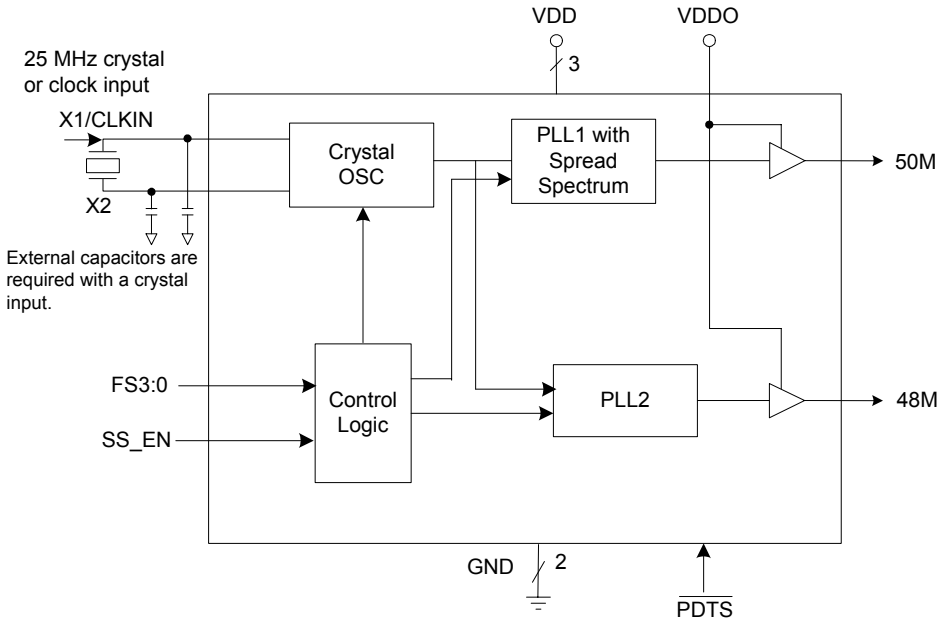
The ICS650-41 is a spread spectrum clock synthesizer intended for video projector applications. It generates an EMI optimized 50 MHz clock signal (EMI peak reduction of 7 to 14 dB on 3rd through 19th harmonics) through the use of Spread Spectrum techniques from a 25 MHz crystal or clock input. For the 50 MHz output, the modulation rate is 50 kHz.

In addition to the EMI optimized clock signal, the device generates a 48 MHz clock for USB.

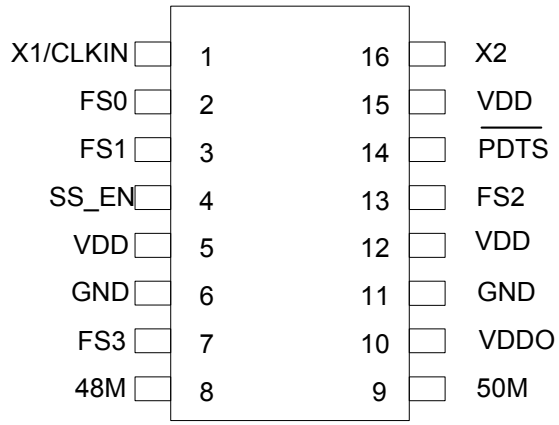
Features

- Packaged in 16-pin TSSOP (173 mil)
- Supply voltages: VDD = 3.3 V, VDDO = 2.5 V
- Peak-to-peak jitter: ±125 ps typ
- Output duty cycle 45/55% (worst case)
- Guarantees +85°C operational condition
- 25 MHz crystal or reference clock input
- Zero (0) ppm frequency error on all output clocks
- Advanced, low-power CMOS process
- Industrial temperature range

Block Diagram



Pin Assignment



16-pin (173 mil) TSSOP

Spread Spectrum and Output Configuration Table

FS3	FS2	FS1	FS0	Spread Type	SS Out
0	0	0	0	Center	±0.25
0	0	0	1	Center	±0.50
0	0	1	0	Center	±0.75
0	0	1	1	Center	±1.00
0	1	0	0	Center	±1.25
0	1	0	1	Center	±1.50
0	1	1	0	Center	±1.75
0	1	1	1	Center	±2.00
1	0	0	0	Down	-0.5
1	0	0	1	Down	-0.75
1	0	1	0	Down	-1.0
1	0	1	1	Down	-1.25
1	1	0	0	Down	-1.5
1	1	0	1	Down	-1.75
1	1	1	0	Down	-2.0
1	1	1	1	Down	-2.25

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/CLKIN	Input	Crystal input. Connect this pin to a 25 MHz crystal or external input clock.
2	FS0	Input	Select pin 0. Internal pull-up resistor. See table on page 2.
3	FS1	Input	Select pin 1. Internal pull-up resistor. See table on page 2.
4	SS_EN	Input	Spread spectrum enable pin. Internal pull-up resistor. Enabled = high.
5	VDD	Power	Connect to +3.3 V.
6	GND	Power	Connect to ground.
7	FS3	Input	Select pin 3. Internal pull-up resistor. See table on page 2.
8	48M	Output	Fixed 48 MHz output. Weak internal pull-down when tri-state.
9	50M	Output	Spread Spectrum output. Weak internal pull-down when tri-stated.
10	VDDO	Power	Connect to +2.5 V.
11	GND	Power	Connect to ground.
12	VDD	Power	Connect to +3.3 V.
13	FS2	Input	Select pin 2. Internal pull-up resistor. See table on page 2.
14	$\overline{\text{PDTS}}$	Input	Powers down entire chip. Tri-states CLK outputs when low. Internal pull-up.
15	VDD	Power	Connect to +3.3 V.
16	X2	Output	Crystal Output. Connect this pin to a 25 MHz crystal. Do not connect if clock input is used.

External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS650-41 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between each VDD and the PCB ground plane.

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal (C_L -6 pF)*2. In this equation, C_L= crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF [(16-6) x 2] = 20.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitors should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pins should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS650-41. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS650-41. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature (max. of 10 seconds)	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0	–	+85	° C
Power Supply Voltage (measured in respect to GND)	+3.135	+3.3	+3.465	V
Power Supply Voltage (VDDO)	+2.375	+2.5	+2.625	V
Power Supply Ramp Time, Figure 4			4	ms

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%, VDDO = 2.5 V ±5%** , Ambient Temperature 0 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Supply Current	IDD	no load		27		mA
		$\overline{PDTS}$ = 0, no load		40		uA
	IDDO	no load		4		mA
		$\overline{PDTS}$ = 0, no load		1		uA
Input High Voltage	V_{IH}	FS3:0, $\overline{PDTS}$, SS_EN	2			V
Input Low Voltage	V_{IL}	FS3:0, $\overline{PDTS}$, SS_EN			0.8	V
Input High Voltage	V_{IH}	X1/CLKIN	0.7 x VDD			V
Input Low Voltage	V_{IL}	X1/CLKIN			0.3 x VDD	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	1.8			V
Output Low Voltage	V_{OL}	I_{OL} = 4 mA			0.6	V
Short Circuit Current	I_{OS}			±50		mA
Nominal Output Impedance	Z_O			20		Ω
Internal Pull-up Resistor	R_{PU}	FS3:0, $\overline{PDTS}$, SS_EN		360		kΩ
Input Leakage Current	I_I	FS3:0, $\overline{PDTS}$, SS_EN, VIN=VDD		1		uA
Internal Pull-down Resistor	R_{PD}	CLK outputs		900		kΩ
Input Capacitance	C_{IN}	Inputs		4		pF

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%, VDDO = 2.5 V ±5%**, Ambient Temperature 0 to +85° C

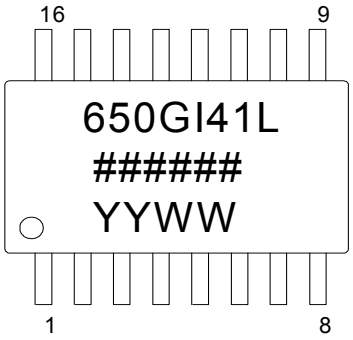
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}	Crystal or clock input		25		MHz
Spread Spectrum Modulation Frequency				50		kHz
Duty Cycle	t_2/t_1	at VDD/2, Note 1 and Figures 1 and 2	45	50	55	%
Output Fall Time	t_3	80% to 20%, Note 1 and Figures 1 & 3		1.5		ns
Output Rise Time	t_4	20% to 80%, Note 1 and Figures 1 & 3		1.5		ns
One Sigma Clock Period Jitter		Note 1		30		ps
Absolute Jitter, Peak-to-Peak	t_{ja}	Deviation from mean, SS_EN=0, Note1 & Figures 1 and 6		±125		ps
Output Enable Time	t_{EN}	$\overline{PDTS}$ high to PLL locked to within 1% of final value, Figure 5		2.5	5	ms
Output Disable Time	t_{DIS}	$\overline{PDTS}$ low to tri-state, Figure 5		20		ns
Power-up Time	t_P	PLL lock-time from power-up to 1% of final value, Figure 4		6	10	ms

Note 1: Measured with 15 pF load.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		78		°C/W
	θ_{JA}	1 m/s air flow		70		°C/W
	θ_{JA}	3 m/s air flow		68		°C/W
Thermal Resistance Junction to Case	θ_{JC}			37		°C/W

Marking Diagram



Notes:

1. ###### is the lot number.
2. YYWW is the last two digits of the year and the week number that the part was assembled.

Timing Diagrams

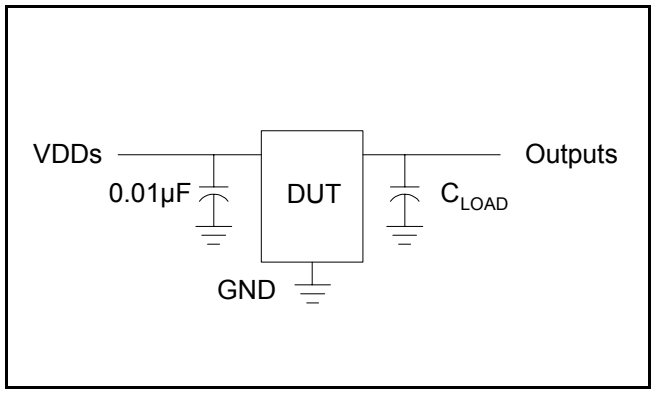


Figure 1: Test and Measurement Setup

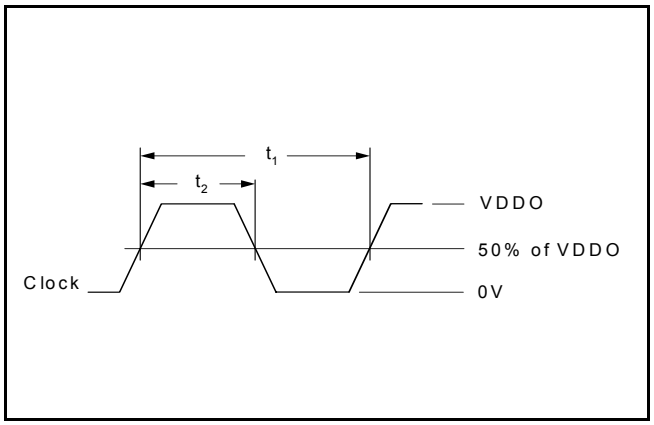


Figure 2: Duty Cycle Definitions

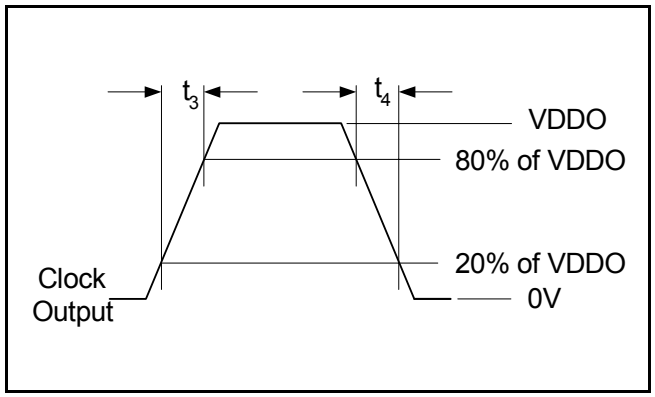


Figure 3: Rise and Fall Time Definitions

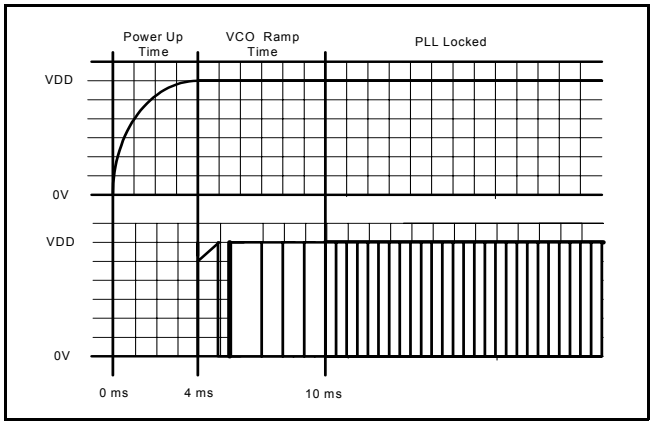


Figure 4: Power Up and PLL Lock Timing

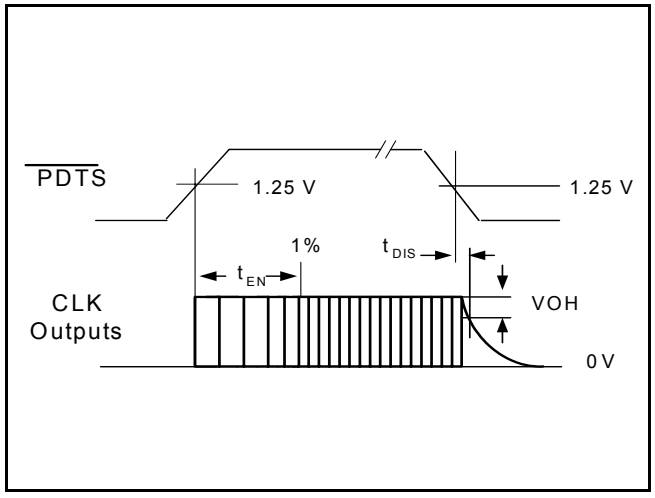


Figure 5: $\overline{\text{PDTS}}$ to Stable Clock Output Timing

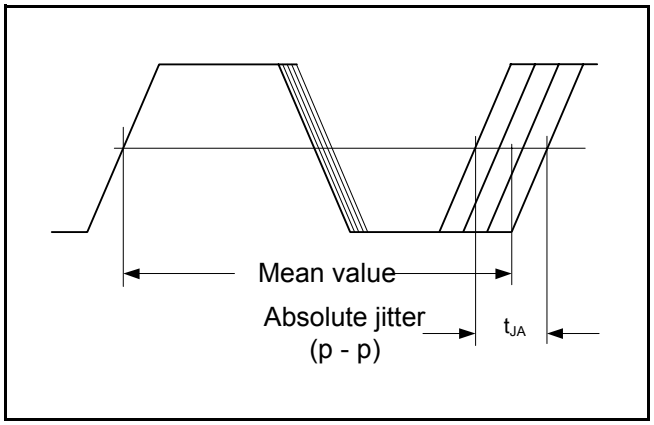
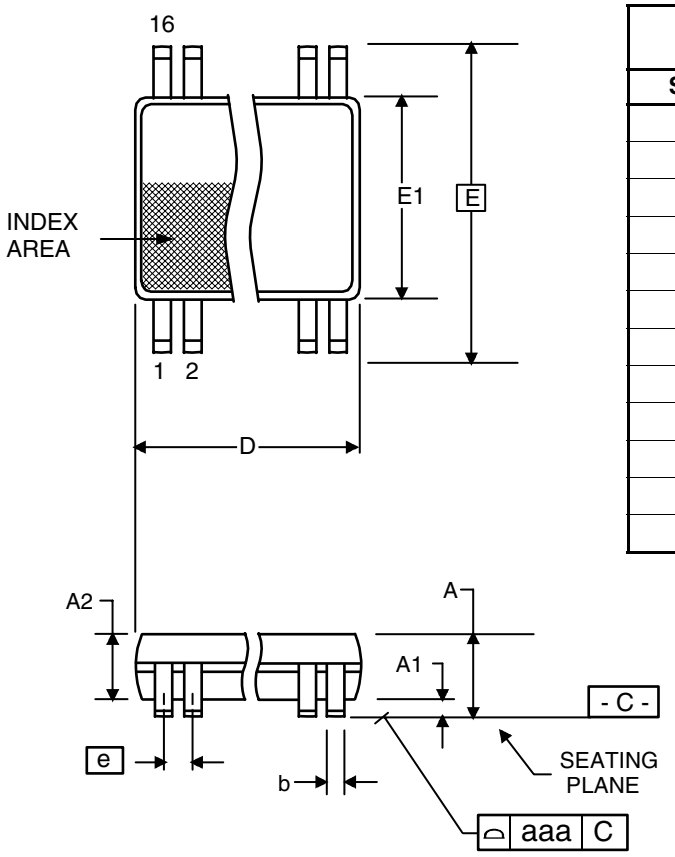


Figure 6: Short Term Jitter Definition

Package Outline and Package Dimensions (16-pin TSSOP, 173 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
650GI-41LF	650GI41L	Tubes	16-pin TSSOP	0 to +85° C
650GI-41LFT	650GI41L	Tape and Reel	16-pin TSSOP	0 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Revision History

Rev.	Originator	Date	Description of Change
B	P.Griffith	10/07/04	Changed the input frequency from 14.31818 to 25 MHz; changed Short Circuit Current from ±70 to ±50; added separate Pull-up resistor spec for SS_EN; added “I” to part ordering number
C	P. Griffith	11/15/04	Changed AC and DC parameters to reflect measured char values: I_{DD}, I_{DDO}, V_{IH}, V_{IL}, R_{PU}, I_I, R_{PD}, t_1,.t_2, t_3, t_4, t_{ja}, t_{EN}, t_{DIS}, t_P. Added Figures for key parameters.
D	P. Griffith	12/06/04	Changed jitter spec to +/-150 ps and duty cycle to 45% min, 55% max.
E	P. Griffith	1/17/05	Renamed pin 1 to X1/CLKin on page2, improved jitter spec to +/-125 ps on front page and in electrical tables, changed rise and fall time to 1.5 ns typical to reflect balanced drive, changed typical ID spec to 4 ma, updated graphs on page 8 to reflect separate VDDO and correct bypass capacitor value, updated marking diagram and ordering table to reflect Pb-free device.
G		10/27/09	Updated ordering information

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