ICS502
LOCO™ PLL Clock Multiplier

Description

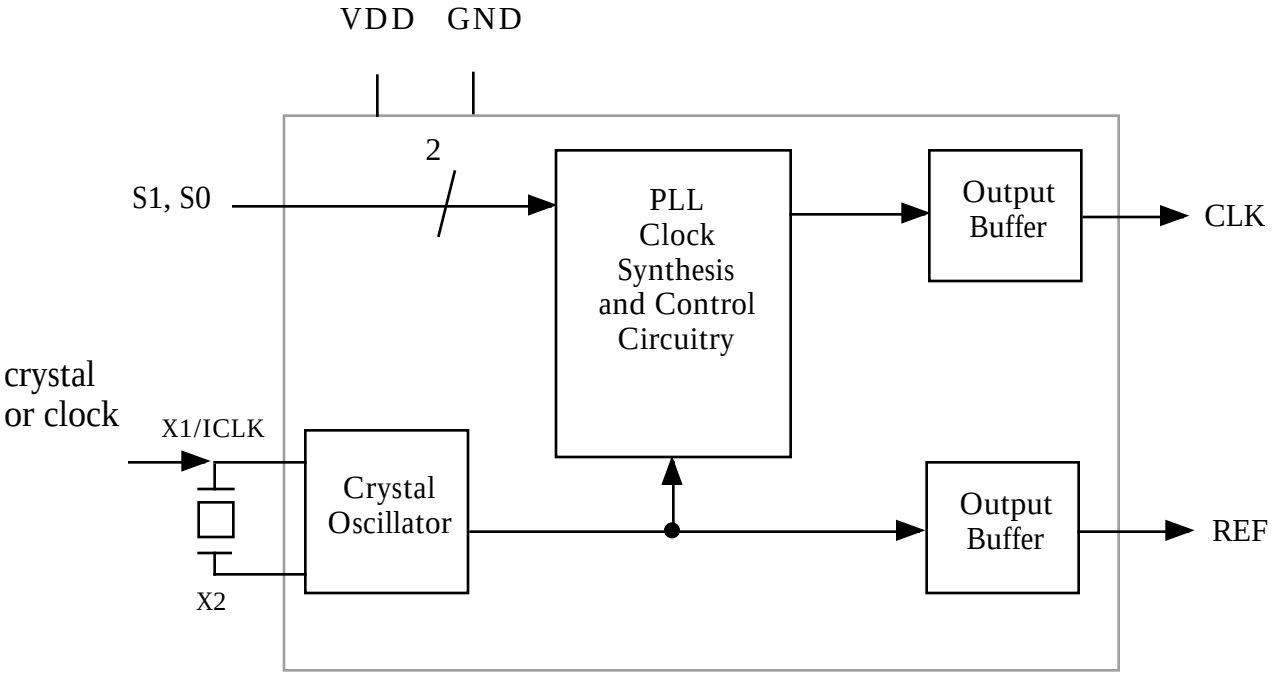
The ICS502 LOCO™ is the most cost effective way to generate a high quality, high frequency clock output and a reference from a low frequency crystal or clock input. The name LOCO stands for LOw Cost Oscillator, as it is designed to replace crystal oscillators in most electronic systems. Using Phase-Locked-Loop (PLL) techniques, the device uses a standard fundamental mode, inexpensive crystal to produce output clocks up to 160 MHz.

Stored in the chip's ROM is the ability to generate 6 different multiplication factors, allowing one chip to output many common frequencies (see page 2).

Features

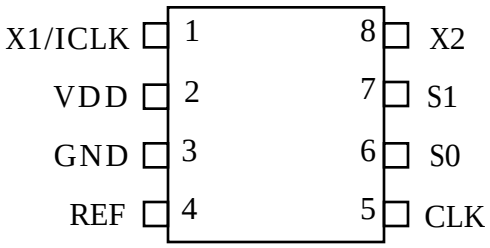
- Packaged as 8 pin SOIC or die
- ICS' lowest cost PLL clock plus reference
- Zero ppm multiplication error
- Easy to cascade with other 5xx series
- Input crystal frequency of 5 - 27 MHz
- Input clock frequency of 2 - 50 MHz
- Output clock frequencies up to 160 MHz
- Low jitter - 50 ps one sigma
- Compatible with all popular CPUs
- Duty cycle of 45/55 up to 160 MHz
- Operating voltages of 3.0 to 5.5V
- Industrial temperature version available
- 25mA drive capability at TTL levels
- Advanced, low power CMOS process

Block Diagram



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Pin Assignment



Clock Decoding Table (MHz)

S1	S0	CLK
0	0	x2
0	1	x5
M	0	x3
M	1	x3.33
1	0	x4
1	1	x2.5

Minimum input frequency for all selections is per table on page 3.

0 = connect directly to ground.
1 = connect directly to VDD.
M = leave unconnected (floating).

Common Output Frequencies Examples (MHz)

Output	20	25	30	32	33.33	37.5	40	48	50	54	60
Input	10	10	10	16	10	15	20	16	20	13.5	20
Selection (S1, S0)	0, 0	1, 1	M, 0	0, 0	M, 1	1, 1	0, 0	M, 0	1, 1	1, 0	M, 0
Output	64	66.66	72	75	80	81	90	100	108	120	135
Input	16	20	24	15	20	27	27	20	27	24	27
Selection (S1, S0)	1, 0	M, 1	M, 0	0, 1	1, 0	M, 0	M, 1	0, 1	1, 0	0, 1	0, 1

Note that all of the above outputs are achieved by using an inexpensive 10MHz to 27MHz crystal. Consult MicroClock/ICS on how to achieve other output frequencies.

Pin Descriptions

Number	Name	Type	Description
1	X1/ICLK	I	Crystal connection or clock input.
2	VDD	P	Connect to +3.3V or +5V.
3	GND	P	Connect to ground.
4	REF	O	Buffered crystal oscillator output clock.
5	CLK	O	Clock output per Table above.
6	S0	I	Select 0 for output clock. Connect to GND or VDD.
7	S1	TI	Select 1 for output clock. Connect to GND or VDD or float.
8	X2	O	Crystal connection. Leave unconnected for clock input.

Key: I = Input, TI = Tri-Level Input, O = output, P = power supply connection

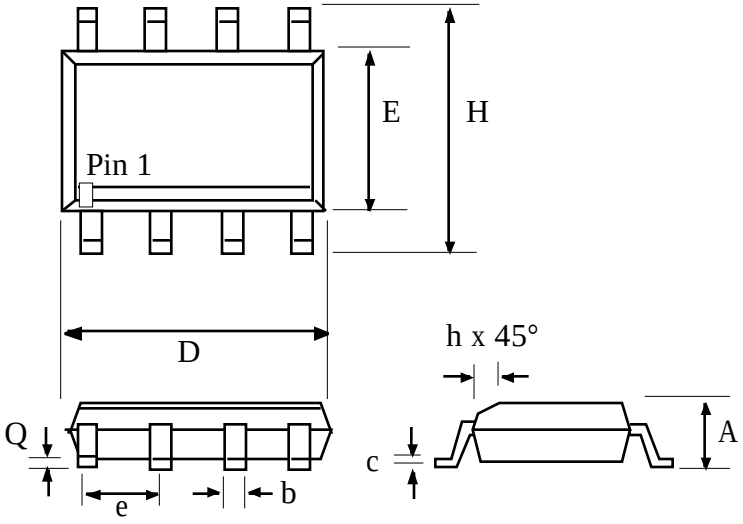
Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (stresses beyond these can permanently damage the device)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+0.5	V
Clock Output	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	C
	ICS502MI only	-40		85	C
Soldering Temperature	Max of 10 seconds			260	C
Storage temperature		-65		150	C
DC CHARACTERISTICS (VDD = 5.0V unless otherwise noted)					
Operating Voltage, VDD		3		5.5	V
Input High Voltage, VIH, ICLK only	ICLK (Pin 1)	(VDD/2)+1	VDD/2		V
Input Low Voltage, VIL, ICLK only	ICLK (Pin 1)		VDD/2	(VDD/2)-1	V
Input High Voltage, VIH	S0	2			V
Input Low Voltage, VIL	S0			0.8	V
Input High Voltage, VIH	S1	VDD-0.5			V
Input Low Voltage, VIL	S1			0.5	V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
IDD Operating Supply Current, 20 MHz crystal	No Load, 100MHz		20		mA
Short Circuit Current	CLK output		±70		mA
On-Chip Pull-up Resistor	Pin 6		270		kΩ
Input Capacitance, S1, S0	Pins 6, 7		4		pF
AC CHARACTERISTICS (VDD = 5.0V unless otherwise noted)					
Input Frequency, crystal input		5		27	MHz
Input Frequency, clock input		2		50	MHz
Output Frequency, VDD = 4.5 to 5.5V	0 C to +70 C	14		160	MHz
	-40 C to +85 C	14		140	MHz
Output Frequency, VDD = 3.0 to 3.6V	0 C to +70 C	14		100	MHz
	-40 C to +85 C	14		90	MHz
Output Clock Rise Time	0.8 to 2.0V		1		ns
Output Clock Fall Time	2.0 to 0.8V		1		ns
Output Clock Duty Cycle	at VDD/2	45	49 to 51	55	%
Absolute Clock Period Jitter	Deviation from mean		±120		ps
One Sigma Clock Period Jitter			50		ps

External Components / Crystal Selection

The ICS502 requires a 0.01µF decoupling capacitor to be connected between VDD and GND. It must be connected close to the ICS502 to minimize lead inductance. No external power supply filtering is required for this device. A 33Ω terminating resistor can be used next to the CLK pin. The total on-chip capacitance is approximately 13 pF, so a parallel resonant, fundamental mode crystal should be used. For crystals with a specified load capacitance greater than 13 pF, crystal capacitors should be connected from each of the pins X1 and X2 to Ground as shown in the Block Diagram on page 1. The value (in pF) of these crystal caps should be = $(C_L-13)*2$, where C_L is the crystal load capacitance in pF. These external capacitors are only required for applications where the exact frequency is critical. For a clock input, connect to X1 and leave X2 unconnected (no capacitors on either).

Package Outline and Package Dimensions



8 pin SOIC

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.055	0.068	1.397	1.7272
b	0.013	0.019	0.330	0.483
D	0.185	0.200	4.699	5.080
E	0.150	0.160	3.810	4.064
H	0.225	0.245	5.715	6.223
e	.050 BSC		1.27 BSC	
h		0.015		0.381
Q	0.004	0.01	0.102	0.254

Ordering Information

Part/Order Number	Marking	Package	Temperature
ICS502M	ICS502M	8 pin SOIC	0 to 70 C
ICS502MT	ICS502M	8 pin SOIC on tape and reel	0 to 70 C
ICS502MI	ICS502I	8 pin SOIC	-40 to +85 C
ICS502MIT	ICS502I	8 pin SOIC on tape and reel	-40 to +85 C

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