10Base-T/100Base-TX Integrated PHYceiver™

General

The ICS1892, an enhanced version of the ICS 1890, is a fully integrated, physical-layer device (PHY) that is compliant with both the 10Base-T and 100Base-TX CSMA/CD Ethernet Standard, ISO/IEC 8802-3.

The ICS1892 incorporates digital signal processing (DSP) in its Physical Medium Dependent (PMD) sublayer. As a result, it can transmit and receive data on unshielded twisted-pair (UTP) category 5 cable with attenuation in excess of 24 dB at 100 MHz. With this ICS-patented technology, the ICS1892 can virtually eliminate errors from killer packets.

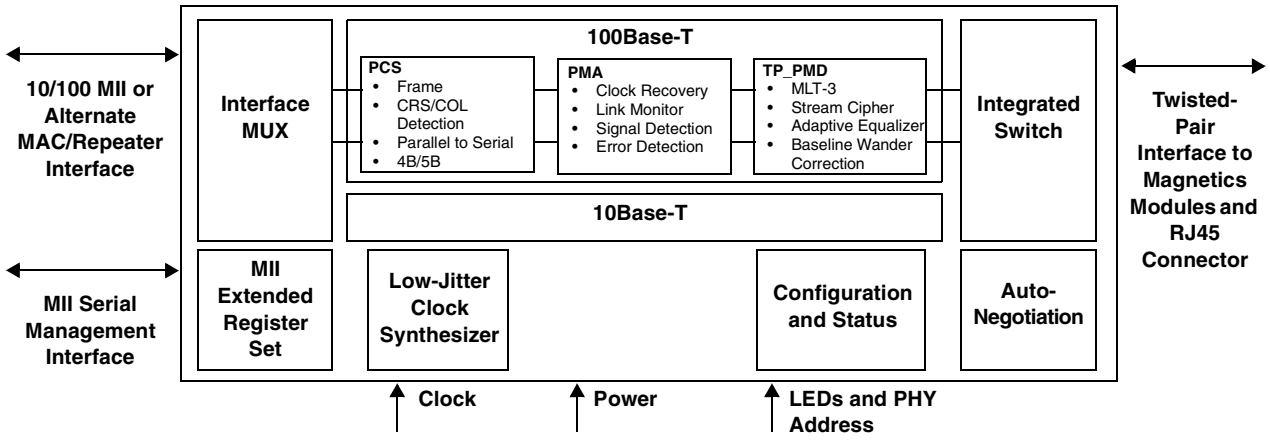
The ICS1892 supports a broad range of applications: data terminal equipment (network interface cards and motherboards), switches, repeaters, bridges, and routers. Its Media Independent Interface (MII) supports direct chip-to-chip and motherboard-to-daughterboard connections as well as connections to an MII connector and cable. The ICS1892 also provides a Serial Management Interface for exchanging command and status information with a Station Management (STA) entity.

The ICS1892 Media Dependent Interface (MDI) can be configured to provide either half- or full-duplex operation at data rates of 10 MHz or 100 MHz. The MDI configuration can be done manually (with input pins or control register settings) or automatically (using the Auto-Negotiation features). When the ICS1892 Auto-Negotiation sublayer is enabled, it exchanges technology capability data with its remote link partner and automatically selects the highest-performance operating mode they have in common.

Features

- Supports category 5 cables with attenuation in excess of 24 dB at 100 MHz across a temperature range from -5° to +85° C
- DSP-based baseline wander correction to virtually eliminate killer packets across temperature range of from -5° to +85° C
- Low-power, 0.5-micron CMOS
- Single 5.0-V power supply.
- Single-chip, fully integrated PHY provides PCS, PMA, PMD, and AUTONEG sublayers of IEEE standard
- 10Base-T and 100Base-TX IEEE 802.3 compliant
- Fully integrated, DSP-based PMD includes:
  - Adaptive equalization and baseline wander correction
  - Transmit wave shaping and stream cipher scrambler
  - MLT-3 encoder and NRZ/NRZI encoder
- Highly configurable design supports:
  - Node, repeater, and switch applications
  - Managed and unmanaged applications
  - 10M or 100M half- and full-duplex modes
  - Parallel detection
  - Auto-negotiation, with Next Page capabilities
- MAC/Repeater Interface can be configured as:
  - 10M or 100M Media Independent Interface
  - 100M Symbol Interface (bypasses the PCS)
  - 10M 7-wire Serial Interface
- Provides Loopback Modes for Diagnostic Functions
- Small Footprint 64-pin Low-Profile LQFP and MQFP packages available

ICS1892 Block Diagram



ICS reserves the right to make changes in the device data identified in this publication without further notice. ICS advises its customers to obtain the latest version of all device data to verify that any information being relied upon by the customer is current and accurate.

Table of Contents

Section	Title	Page
Chapter 1	**Abbreviations and Acronyms**	**9**
Chapter 2	**Conventions and Nomenclature**	**11**
Chapter 3	**ICS 1892 Enhanced Features**	**13**
Chapter 4	**Overview of the ICS 1892**	**15**
4.1	100Base-TX Operation	16
4.2	10Base-T Operation	16
Chapter 5	**Operating Modes Overview**	**17**
5.1	Reset Operations	18
5.1.1	General Reset Operations	18
5.1.2	Specific Reset Operations	19
5.2	Power-Down Operations	20
5.3	Automatic Power-Saving Operations	21
5.4	Auto-Negotiation Operations	21
5.5	100Base-TX Operations	22
5.6	10Base-T Operations	22
5.7	Half-Duplex and Full-Duplex Operations	22
Chapter 6	**Interface Overviews**	**23**
6.1	MII Data Interface	24
6.2	100M Symbol Interface	25
6.3	10M Serial Interface	27
6.4	Link Pulse Interface	29
6.5	Serial Management Interface	30
6.6	Twisted-Pair Interface	30
6.7	Clock Reference Interface	30
6.7.1	Clock Source: Oscillator or CMOS Driver	30
6.7.2	Clock Source: Crystal	31
6.8	Configuration Interface	32
6.9	Status Interface	32
Chapter 7	**Functional Blocks**	**33**
7.1	Functional Block: Media Independent Interface	34
7.2	Functional Block: Auto-Negotiation	35
7.2.1	Auto-Negotiation General Process	36
7.2.2	Auto-Negotiation: Parallel Detection	37
7.2.3	Auto-Negotiation: Remote Fault Signaling	37
7.2.4	Auto-Negotiation: Reset and Restart	38
7.2.5	Auto-Negotiation: Progress Monitor	39

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Table of Contents

Section	Title	Page
7.3	Functional Block: 100Base-X PCS and PMA Sublayers	41
7.3.1	PCS Sublayer	41
7.3.2	PMA Sublayer	41
7.3.3	PCS/PMA Transmit Modules	42
7.3.4	PCS/PMA Receive Modules	43
7.3.5	PCS Control Signal Generation	44
7.3.6	4B/5B Encoding/Decoding	45
7.4	Functional Block: 100Base-TX TP-PMD Operations	46
7.4.1	100Base-TX Operation: Stream Cipher Scrambler/Descrambler	46
7.4.2	100Base-TX Operation: MLT-3 Encoder/Decoder	46
7.4.3	100Base-TX Operation: DC Restoration	46
7.4.4	100Base-TX Operation: Adaptive Equalizer	47
7.4.5	100Base-TX Operation: Twisted-Pair Transmitter	47
7.4.6	100Base-TX Operation: Twisted-Pair Receiver	47
7.4.7	100Base-TX Operation: Auto Polarity Correction	48
7.4.8	100Base-TX Operation: Isolation Transformer	48
7.5	Functional Block: 10Base-T Operations	49
7.5.1	10Base-T Operation: Manchester Encoder/Decoder	49
7.5.2	10Base-T Operation: Clock Synthesis	49
7.5.3	10Base-T Operation: Clock Recovery	49
7.5.4	10Base-T Operation: Idle	50
7.5.5	10Base-T Operation: Link Monitor	50
7.5.6	10Base-T Operation: Smart Squelch	51
7.5.7	10Base-T Operation: Carrier Detection	51
7.5.8	10Base-T Operation: Collision Detection	51
7.5.9	10Base-T Operation: Jabber	52
7.5.10	10Base-T Operation: SQE Test	52
7.5.11	10Base-T Operation: Twisted-Pair Transmitter	53
7.5.12	10Base-T Operation: Twisted-Pair Receiver	53
7.5.13	10Base-T Operation: Auto Polarity Correction	54
7.5.14	10Base-T Operation: Isolation Transformer	54
7.6	Functional Block: Management Interface	55
7.6.1	Management Register Set Summary	55
7.6.2	Management Frame Structure	55

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Table of Contents

Section	Title	Page
Chapter 8	**Management Register Set**	**58**
8.1	Introduction to Management Register Set	59
8.1.1	Management Register Set Outline	59
8.1.2	Management Register Bit Access	60
8.1.3	Management Register Bit Default Values	60
8.1.4	Management Register Bit Special Functions	61
8.2	Register 0: Control Register	62
8.2.1	Reset (bit 0.15)	62
8.2.2	Loopback Enable (bit 0.14)	63
8.2.3	Data Rate Select (bit 0.13)	63
8.2.4	Auto-Negotiation Enable (bit 0.12)	63
8.2.5	Low Power Mode (bit 0.11)	64
8.2.6	Isolate (bit 0.10)	64
8.2.7	Restart Auto-Negotiation (bit 0.9)	64
8.2.8	Duplex Mode (bit 0.8)	65
8.2.9	Collision Test (bit 0.7)	65
8.2.10	IEEE Reserved Bits (bits 0.6:0)	65
8.3	Register 1: Status Register	66
8.3.1	100Base-T4 (bit 1.15)	66
8.3.2	100Base-TX Full Duplex (bit 1.14)	67
8.3.3	100Base-TX Half Duplex (bit 1.13)	67
8.3.4	10Base-T Full Duplex (bit 1.12)	67
8.3.5	10Base-T Half Duplex (bit 1.11)	67
8.3.6	IEEE Reserved Bits (bits 1.10:7)	68
8.3.7	MF Preamble Suppression (bit 1.6)	68
8.3.8	Auto-Negotiation Complete (bit 1.5)	68
8.3.9	Remote Fault (bit 1.4)	69
8.3.10	Auto-Negotiation Ability (bit 1.3)	69
8.3.11	Link Status (bit 1.2)	69
8.3.12	Jabber Detect (bit 1.1)	70
8.3.13	Extended Capability (bit 1.0)	70
8.4	Register 2: PHY Identifier Register	71

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Table of Contents

Section	Title	Page
8.5	Register 3: PHY Identifier Register	73
8.5.1	OUI bits 19-24 (bits 3.15:10)	73
8.5.2	Manufacturer's Model Number (bits 3.9:4)	73
8.5.3	Revision Number (bits 3.3:0)	74
8.6	Register 4: Auto-Negotiation Register	75
8.6.1	Next Page (bit 4.15)	75
8.6.2	IEEE Reserved Bit (bit 4.14)	76
8.6.3	Remote Fault (bit 4.13)	76
8.6.4	Technology Ability Field (bits 4.12:5)	76
8.6.5	Selector Field (Bits 4.4:0)	77
8.7	Register 5: Auto-Negotiation Link Partner Ability Register	78
8.7.1	Next Page (bit 5.15)	78
8.7.2	Acknowledge (bit 5.14)	79
8.7.3	Remote Fault (bit 5.13)	79
8.7.4	Technology Ability Field (bits 5.12:5)	79
8.7.5	Selector Field (bits 5.4:0)	79
8.8	Register 6: Auto-Negotiation Expansion Register	80
8.8.1	IEEE Reserved Bits (bits 6.15:5)	80
8.8.2	Parallel Detection Fault (bit 6.4)	81
8.8.3	Link Partner Next Page Able (bit 6.3)	81
8.8.4	Next Page Able (bit 6.2)	81
8.8.5	Page Received (bit 6.1)	81
8.8.6	Link Partner Auto-Negotiation Able (bit 6.0)	81
8.9	Register 7: Auto-Negotiation Next Page Transmit Register	82
8.9.1	Next Page (bit 7.15)	83
8.9.2	IEEE Reserved Bit (bit 7.14)	83
8.9.3	Message Page (bit 7.13)	83
8.9.4	Acknowledge 2 (bit 7.12)	83
8.9.5	Toggle (bit 7.11)	83
8.9.6	Message Code Field / Unformatted Code Field (bits 7.10:0)	83
8.10	Register 8: Auto-Negotiation Next Page Link Partner Ability Register	84
8.10.1	Next Page (bit 8.15)	85
8.10.2	IEEE Reserved Bit (bit 8.14)	85
8.10.3	Message Page (bit 8.13)	85
8.10.4	Acknowledge 2 (bit 8.12)	85
8.10.5	Message Code Field / Unformatted Code Field (bits 8.10:0)	85

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Table of Contents

Section	Title	Page
8.11	Register 16: Extended Control Register	86
8.11.1	Command Override Write Enable (bit 16.15)	87
8.11.2	ICS Reserved (bits 16.14:11)	87
8.11.3	PHY Address (bits 16.10:6)	87
8.11.4	Stream Cipher Scrambler Test Mode (bit 16.5)	87
8.11.5	ICS Reserved (bit 16.4)	87
8.11.6	NRZ/NRZI Encoding (bit 16.3)	87
8.11.7	Invalid Error Code Test (bit 16.2)	88
8.11.8	ICS Reserved (bit 16.1)	88
8.11.9	Stream Cipher Disable (bit 16.0)	88
8.12	Register 17: Quick Poll Detailed Status Register	89
8.12.1	Data Rate (bit 17.15)	90
8.12.2	Duplex (bit 17.14)	90
8.12.3	Auto-Negotiation Progress Monitor (bits 17.13:11)	91
8.12.4	100Base Receive Signal Lost (bit 17.10)	91
8.12.5	PLL Lock Error (bit 17.9)	92
8.12.6	False Carrier (bit 17.8)	92
8.12.7	Invalid Symbol (bit 17.7)	92
8.12.8	Halt Symbol (bit 17.6)	93
8.12.9	Premature End (bit 17.5)	93
8.12.10	Auto-Negotiation Complete (bit 17.4)	93
8.12.11	100Base-TX Signal Detect (bit 17.3)	93
8.12.12	Jabber Detect (bit 17.2)	93
8.12.13	Remote Fault (bit 17.1)	94
8.12.14	Link Status (bit 17.0)	94
8.13	Register 18: 10Base-T Operations Register	95
8.13.1	ICS Reserved (bit 18.15)	95
8.13.2	Polarity Reversed (bit 18.14)	96
8.13.3	ICS Reserved (bits 18.13:6)	96
8.13.4	Jabber Inhibit (bit 18.5)	96
8.13.5	ICS Reserved (bit 18.4)	96
8.13.6	Auto Polarity Inhibit (bit 18.3)	96
8.13.7	SQE Test Inhibit (bit 18.2)	96
8.13.8	Link Loss Inhibit (bit 18.1)	97
8.13.9	Squelch Inhibit (bit 18.0)	97

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Table of Contents

Section	Title	Page
8.14	Register 19: Extended Control Register 2	98
8.14.1	Node/Repeater Configuration (bit 19.15)	99
8.14.2	Hardware/Software Priority Status (bit 19.14)	99
8.14.3	Remote Fault (bit 19.13)	99
8.14.4	ICS Reserved (bits 19.12:2)	99
8.14.5	Automatic 10Base-T Power-Down (bit 19.1)	100
8.14.6	Automatic 100Base-TX Power-Down (bit 19.0)	100
Chapter 9	**ICS 1892 Pin Listing and Pin Descriptions**	**101**
9.1	ICS 1892 Pin Listings	101
9.1.1	Pin Listing by Pin Number	102
9.1.2	Pin Listings by Alphabetical Pin Name	103
9.2	ICS 1892 Pin Descriptions	104
9.2.1	Transformer Interface Pins	104
9.2.2	Multifunction (Multiplexed) Pins: PHY Address and LED Pins	105
9.2.3	Configuration Pins	106
9.2.4	MAC/Repeater Interface Pins	109
9.2.5	Reserved Pins	118
9.2.6	Ground and Power Pins	118
Chapter 10	**DC and AC Operating Conditions**	**120**
10.1	Absolute Maximum Ratings	120
10.2	Recommended Operating Conditions	120
10.3	Recommended Component Values	121
10.4	DC Operating Characteristics	122
10.4.1	DC Operating Characteristics for Supply Current	122
10.4.2	DC Operating Characteristics for TTL Inputs and Outputs	122
10.4.3	DC Operating Characteristics for REF_IN	122
10.4.4	DC Operating Characteristics for Media Independent Interface	123
10.5	Timing Diagrams	124
10.5.1	Timing for Clock Reference In (REF_IN) Pin	124
10.5.2	Timing for Transmit Clock (TXCLK) Pin	125
10.5.3	Timing for Receive Clock (RXCLK) Pin	126
10.5.4	100M MII / 100M Stream Interface: Synchronous Transmit Timing	127
10.5.5	10M MII: Synchronous Transmit Timing	128
10.5.6	MII / 100M Stream Interface: Synchronous Receive Timing	129
10.5.7	MII Management Interface Timing	130
10.5.8	10M Serial Interface: Receive Latency	131
10.5.9	10M Media Independent Interface: Receive Latency	132
10.5.10	10M Serial Interface: Transmit Latency	133
10.5.11	10M Media Independent Interface: Transmit Latency	134
10.5.12	MII / 100M Stream Interface: Transmit Latency	135
10.5.13	MII: Carrier Assertion/De-Assertion (Half-Duplex Transmission)	136

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Table of Contents

Section	Title	Page
10.5.14	100M MII / 100M Stream Interface: Receive Latency	137
10.5.15	Media Dependent Interface: Input-to-Carrier Assertion/De-Assertion	138
10.5.16	Reset: Power-On Reset	139
10.5.17	Reset: Hardware Reset and Power-Down	140
10.5.18	10Base-T: Heartbeat Timing (SQE)	141
10.5.19	10Base-T: Jabber Timing	142
10.5.20	10Base-T: Normal Link Pulse Timing	143
10.5.21	Auto-Negotiation Fast Link Pulse Timing	144
Chapter 11	**Physical Dimensions of ICS 1892 Package**	**145**
Chapter 12	**Ordering Information**	**147**

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Chapter 1 Abbreviations and Acronyms

Table 1-1 lists and interprets the abbreviations and acronyms used throughout this data sheet.

Table 1-1. Abbreviations and Acronyms

Abbreviation / Acronym	Interpretation
4B/5B	4-Bit / 5-Bit Encoding/Decoding
ANSI	American National Standards Institute
CMOS	complimentary metal-oxide semiconductor
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
CW	Command Override Write
DSP	digital signal processing
ESD	End-of-Stream Delimiter
FDDI	Fiber Distributed Data Interface
FLP	Fast Link Pulse
IDL	A ‘dead’ time on the link following a 10Base-T packet, not to be confused with idle
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronic Engineers
ISO	International Standards Organization
LH	Latching High
LL	Latching Low
LMX	Latching Maximum
MAC	Media Access Control
Max.	maximum
Mbps	Megabits per second
MDI	Media Dependent Interface
MF	Management Frame
MII	Media Independent Interface
Min.	minimum
MLT-3	Multi-Level Transition Encoding (3 Levels)
N/A	Not Applicable
NLP	Normal Link Pulse
No.	Number
NRZ	Not Return to Zero
NRZI	Not Return to Zero, Invert on one
OSI	Open Systems Interconnection

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Table 1-1. Abbreviations and Acronyms (*Continued*)

Abbreviation / Acronym	Interpretation
OUI	Organizationally Unique Identifier
PCS	Physical Coding sublayer
PHY	physical-layer device The ICS1892 is a physical-layer device, also referred to as a ‘PHY’ or ‘PHYceiver’. (The ICS 1890 is also a physical-layer device.)
PLL	phase-locked loop
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
ppm	parts per million
QFP	quad flat pack
RO	read only
R/W	read/write
R/W0	read/write zero
SC	self-clearing
SF	Special Functions
SFD	Start-of-Frame Delimiter
SI	Stream Interface Serial Interface Symbol Interface With reference to the MII/SI pin, the acronym ‘SI’ has multiple meanings. • Generically, SI means 'Stream Interface', and is documented as such in the ICS 1890 data sheet. • However, when the MAC/Repeater Interface is configured for: – 10M operations, SI is an acronym for 'Serial Interface'. – 100M operations, SI is an acronym for 'Symbol Interface'.
SQE	Signal Quality Error
SSD	Start-of-Stream Delimiter
STA	Station Management Entity
STP	shielded twisted pair
TAF	Technology Ability Field
TP-PMD	Twisted-Pair Physical Layer Medium Dependent
Typ.	typical
UTP	unshielded twisted pair

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Chapter 2 Conventions and Nomenclature

Table 2-1 lists and explains the conventions and nomenclature used throughout this data sheet.

Table 2-1. Conventions and Nomenclature

Item	Convention / Nomenclature
Asterisk (*)	Within this table, see the item ‘Pin (or signal) names’
Bits	• A bit in a register is identified using the format ‘register.bit’. For example, bit 0.15 is bit 15 of register 0. • When a colon is used with bits, it indicates the range of bits. For example, bits 1.15:11 are bits 15, 14, 13, 12, and 11 of register 1. • For a range of bits, the order is always from the most-significant bit to the least-significant bit.
Code groups	Within this table, see the item ‘Symbols’
Colon (:)	Within this table, see these items: • ‘Bits’ • ‘Pin (or signal) names’
Numbers	• As a default, all numbers use the decimal system (that is, base 10) unless followed by a lowercase letter. A string of numbers followed by a lowercase letter: – A ‘b’ represents a binary (base 2) number – An ‘h’ represents a hexadecimal (base 16) number – An ‘o’ represents an octal (base 8) number • All numerical references to registers use decimal notation (and not hexadecimal).
Pin (or signal) names	• All pin or signal names are provided in capital letters. • A pin name that includes a forward slash ‘/’ is a multi-function, configuration pin. These pins provide the ability to select between two ICS1892 functions. The name provided: – Before the ‘/’ indicates the pin name and function when the signal level on the pin is logic zero. – After the ‘/’ indicates the pin name and function when the signal level on the pin is logic one. For example, the HW/SW pin selects between Hardware (HW) mode and Software (SW) mode. – When the signal level on the HW/SW pin is logic zero, the ICS1892 Hardware mode is selected. – When the signal level on the HW/SW pin is logic one, the ICS1892 Software mode is selected. • An asterisk appended to the end of a pin name or signal name (such as RESET*) indicates an active-low operation. • When a colon is used with pin or signal names, it indicates a range. For example, TXD[3:0] represents pins/signals TXD3, TXD2, TXD1, and TXD0. • When pin name abbreviations are spelled out, words in parentheses indicate additional description that is not part of the pin name abbreviation.

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Table 2-1. Conventions and Nomenclature (*Continued*)

Item	Convention / Nomenclature
Registers	• A bit in a register is identified using the format 'register.bit'. For example, bit 0.15 is bit 15 of register 0. • All numerical references to registers use decimal notation (and not hexadecimal). • When register name abbreviations are spelled out, words in parentheses indicate additional description that is not part of the register name abbreviation.
Signal references	• When referring to signals, the terms: – 'FALSE', 'low', or 'zero' represent signals that are logic zero. – 'TRUE', 'high', or 'one' represent signals that are logic one. • Chapter 10, "DC and AC Operating Conditions" defines the electrical specifications for 'logic zero' and 'logic one' signals.
Symbols	• In this data sheet, code group names are referred to as 'symbols' and they are shown between '/' (slashes). For example, the symbol /J/ represents the first half of the Start-of-Stream Delimiter (SSD1). • Symbol sequences are shown in succession. For example, /I/J/K/ represents an IDLE followed by the SSD.
Terms: 'set', 'active', 'asserted',	The terms 'set', 'active', and 'asserted' are synonymous. They do not necessarily infer logic one. (For example, an active-low signal can be set to logic zero.)
Terms: 'cleared', 'de-asserted', 'inactive'	The terms 'cleared', 'inactive', and 'de-asserted' are synonymous. They do not necessarily infer logic zero.
Terms: 'twisted-pair receiver'	In reference to the ICS1892, the term 'Twisted-Pair Receiver' refers to the set of Twisted-Pair Receive output pins (TP_RXP and TP_RXN).
Terms: 'twisted-pair transmitter'	In reference to the ICS1892, the term 'Twisted-Pair Transmitter' refers to the set of Twisted-Pair Transmit output pins (TP_TXP and TP_TXN).

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Chapter 3 ICS1892 Enhanced Features

The ICS1892 is an enhanced version of the ICS 1890. In contrast to the ICS 1890, the ICS1892 offers significant improvements in both performance and features while maintaining backward compatibility. The specific differences between these devices are listed below.

1. The ICS1892 employs an advanced digital signal processing (DSP) architecture that improves the 100Base-TX Receiver performance beyond that of any other PHY in the market. Specifically:
   a. The ICS1892 DSP-based, adaptive equalization process allows the ICS1892 to accommodate a maximum cable attenuation/insertion loss of 29 dB, which is nearly equivalent to the attenuation loss of a 150-meter Category 5 cable.
   b. The ICS1892 DSP-based, baseline-wander correction process virtually eliminates killer packets.
2. The analog 10Base-T Receive Phase-Locked Loop (PLL) of the ICS 1890 is replaced with a digital PLL in the ICS1892, thereby resulting in lower jitter and improved stability.
3. The ICS 1890 Frequency-Locked Loop (FLL) that is part of the 100Base-TX Clock and Data Recovery circuitry is replaced with a digital FLL in the ICS1892, also resulting in lower jitter and improved stability.
4. The ICS1892 transmit circuits are improved in contrast to the ICS 1890, resulting in a decrease in the magnitude of the 10Base-T harmonic content generated during transmission. (See ISO/IEC 8802-3: 1993 clause 8.3.1.3.)
5. The ICS1892 supports the Auto-Negotiation Next Page functions described in IEEE Std 802.3u-1995 clause 28.2.3.4.
6. The ICS1892 supports Management Frame (MF) Preamble Suppression.
7. The ICS1892 provides the Remote Jabber capability.
8. The ICS1892 has an improved version of the ICS 1890 10Base-T Squelch operation.
9. The ICS1892 “seeds” (that is, initializes) the Transmit Stream Cipher Shift register by using the ICS1892 PHY address from Table 8-16, which minimizes crosstalk and noise in repeater applications.
10. The ICS1892 offers an automatic 10Base-T power-down mode.
11. The enhanced features of the ICS1892 required some modifications to the ICS 1890 Management Registers. However, the ICS1892 Management Registers are backward-compatible with the ICS 1890 Management Registers. Table 3-1 summarizes the differences between the ICS 1890 and the ICS1892 Management Registers.

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Table 3-1. Summary of Differences between ICS 1890 and ICS1892 Registers

Register. Bit(s)	ICS 1890		ICS1892	
	Function	**Default**	**Function**	**Default**
1.6	Reserved	0b (always)	Management Frame Preamble Suppression	0b
3.9:4	Model Number	000010b	Model Number	000011b
3:0	Revision Number	0011b	Revision Number	0000b
6.2	Next Page Able	0b (always)	Next Page Able	1b
7.15:0	Not applicable (N/A)	N/A	Auto-Negotiate Next Page Transmit Register	2001h
8.15:0	N/A	N/A	Auto-Negotiate Next Page Link Partner Ability	0000h
9.15:0 through 15.15:0	IEEE reserved.	0000h	IEEE reserved. **Note:** Although the default value is changed, this response more accurately reflects an MDIO access to registers 9–15.	FFFFh
18.15	Reserved	0b	Remote Jabber	0b
19.1	Reserved	0b	Automatic 10Base-T Power Down	1b
20.15:0 through 31.15:0	N/A	N/A	ICS test registers. (There is no claim of backward compatibility for these registers.)	See specific registers and bits.

Note:

1. There are new registers and bits. For example:
   a. Registers 7 and 8 are new (that is, the ICS 1890 does not have these registers).
   b. Registers 20 through 31 are new ICS test registers.
2. For some bits (such as the model number and revision number bits), the default values are changed.

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Chapter 4 Overview of the ICS1892

The ICS1892 is a stream processor. During data transmission, it accepts sequential nibbles from its MAC (Media Access Control)/Repeater Interface, converts them into a serial bit stream, encodes them, and transmits them over the medium through an external isolation transformer. When receiving data, the ICS1892 converts and decodes a serial bit stream (acquired from an isolation transformer that interfaces with the medium) into sequential nibbles. It subsequently presents these nibbles to its MAC/Repeater Interface.

The ICS1892 implements the OSI model's physical layer, consisting of the following, as defined by the ISO/IEC 8802-3 standard:

- Physical Coding sublayer (PCS)
- Physical Medium Attachment sublayer (PMA)
- Physical Medium Dependent sublayer (PMD)
- Auto-Negotiation sublayer

The ICS1892 is transparent to the next layer of the OSI model, the link layer. The link layer has two sublayers: the Logical Link Control sublayer and the MAC sublayer. The ICS1892 can interface directly to a MAC and offers multiple, configurable modes of operation. Alternately, this configurable interface can be connected to a repeater, which extends the physical layer of the OSI model.

The ICS1892 transmits framed packets acquired from its MAC/Repeater Interface and receives encapsulated packets from another PHY, which it translates and presents to its MAC/Repeater Interface.

Note: As per the ISO/IEC standard, the ICS1892 does not affect, nor is it affected by, the underlying structure of the MAC/repeater frame it is conveying.

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4.1 100Base-TX Operation

During 100Base-TX data transmission, the ICS1892 accepts packets from a MAC/repeater and inserts Start-of-Stream Delimiters (SSDs) and End-of-Stream Delimiters (ESDs) into the data stream. The ICS1892 encapsulates each MAC/repeater frame, including the preamble, with an SSD and an ESD. As per the ISO/IEC Standard, the ICS1892 replaces the first octet of each MAC preamble with an SSD and appends an ESD to the end of each MAC/repeater frame.

When receiving data from the medium, the ICS1892 removes each SSD and replaces it with the pre-defined preamble pattern before presenting the nibbles to its MAC/Repeater Interface. When the ICS1892 encounters an ESD in the data stream, signifying the end of the frame, it ends the presentation of nibbles to its MAC/Repeater Interface. Therefore, the local MAC/repeater receives an unaltered copy of the transmitted frame sent by the remote MAC/repeater.

During periods when MAC frames are being neither transmitted nor received, the ICS1892 signals and detects the IDLE condition on the Link Segment. In the 100Base-TX mode, the ICS1892 transmit channel sends a continuous stream of scrambled ones to signify the IDLE condition. Similarly, the ICS1892 receive channel continually monitors its data stream and looks for a pattern of scrambled ones. The results of this signaling and monitoring provide the ICS1892 with the means to establish the integrity of the Link Segment between itself and its remote link partner and informing its Station Management Entity (STA) of the link status.

For 100M data transmission, the ICS1892 MAC/Repeater Interface can be configured to provide either a 100M Media Independent Interface (MII) or a 100M Symbol Interface. With the Symbol Interface configuration, the data stream bypasses the ICS1892 Physical Coding sublayer (PCS) and the following results:

1. The ICS1892 shifts the responsibility of performing the 4B/5B translation to the MAC/repeater. As a result, the requirement is for a 5-bit data path between the MAC/repeater and the ICS1892.
2. The latency through the ICS1892 reduces. (The ICS1892 provides this 100M Symbol Interface primarily for repeater applications for which latency is a critical performance parameter.)

4.2 10Base-T Operation

During 10Base-T data transmission, the ICS1892 inserts only the IDL delimiter into the data stream. The ICS1892 appends the IDL delimiter to the end of each MAC frame. It is not required to insert an SSD-like delimiter because the 10Base-T preamble already has a Start-of-Frame delimiter (SFD).

When receiving data from the medium (such as a twisted-pair cable), the ICS1892 uses the preamble to synchronize its receive clock. When the ICS1892 receive clock establishes lock, it presents the preamble nibbles to its MAC/Repeater Interface. The 10M MAC/Repeater Interface can be configured as either a 10M MII, a 10M Serial Interface, or a Link Pulse Interface.

In 10M operations, during periods when MAC frames are being neither transmitted nor received, the ICS1892 signals and detects Normal Link Pulses. This action allows the integrity of the Link Segment with the remote link partner to be established and then reported to the ICS1892's STA.

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Chapter 5 Operating Modes Overview

The ICS1892 operating modes and interfaces are configurable with one of two methods. The first configuration method is by using hardware pins. With this method, the HW/SW (hardware/software) pin determines whether it is the hardware pins or the register bits that have priority for configuring the ICS1892.

The second – and more typical – configuration method is by using register bits, typically controlled from software. The register bits are accessible through a standard MII (Media Independent Interface) Serial Management Port. Even when the MAC/Repeater Interface is not supporting the standard MII Data Interface, access to the Serial Management Port is provided (that is, operation of the Serial Management Port is independent of the MAC/Repeater Interface configuration).

The ICS1892 provides a number of configuration functions to support a variety of operations. For example, the MAC/Repeater Interface can be configured to operate as a 10M MII, a 100M MII, a 100M Symbol Interface, a 10M Serial Interface, or a Link Pulse Interface. The protocol on the Medium Dependent Interface (MDI) can be configured to support either 10M or 100M operations in either half-duplex or full-duplex modes.

The ICS1892 is fully compliant with the ISO/IEC 8802-3 standard, as it pertains to both 10Base-T and 100Base-TX operations. The feature-rich ICS1892 allows easy migration from 10-Mbps to 100-Mbps operations as well as from systems that require support of both 10M and 100M links.

This chapter is an overview of the following ICS1892 modes of operation:

- Section 5.1, “Reset Operations”
- Section 5.2, “Power-Down Operations”
- Section 5.3, “Automatic Power-Saving Operations”
- Section 5.4, “Auto-Negotiation Operations”
- Section 5.5, “100Base-TX Operations”
- Section 5.6, “10Base-T Operations”
- Section 5.7, “Half-Duplex and Full-Duplex Operations”

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5.1 Reset Operations

This section first discusses reset operations in general and then specific ways in which the ICS1892 can be configured for various reset options.

5.1.1 General Reset Operations

The following reset operations apply to all the specific ways in which the ICS1892 can be reset, which are discussed in Section 5.1.2, “Specific Reset Operations”.

5.1.1.1 Entering Reset

When the ICS1892 enters a reset condition (either through hardware, power-on reset, or software), it does the following:

1. Isolates the MAC/Repeater Interface input pins
2. Drives all MAC/Repeater Interface output pins low
3. Tri-states the signals on its Twisted-Pair Transmit pins (TP_TXP and TP_TXN)
4. Initializes all its internal modules and state machines to their default states
5. Enters the power-down state
6. Initializes all internal latching low (LL), latching high (LH), and latching maximum (LMX) Management Register bits to their default values

5.1.1.2 Exiting Reset

When the ICS1892 exits a reset condition, it does the following:

1. Exits the power-down state
2. Latches the Serial Management Port Address of the ICS1892 into the Extended Control Register, bits 16.10:6. [See Section 8.11.3, “PHY Address (bits 16.10:6)”.]
3. Enables all its internal modules and state machines
4. Sets all Management Register bits to either (1) their default values or (2) the values specified by their associated ICS1892 input pins, as determined by the HW/SW pin
5. Enables the Twisted-Pair Transmit pins (TP_TXP and TP_TXN)
6. Resynchronizes both its Transmit and Receive Phase-Locked Loops, which provide its transmit clock (TXCLK) and receive clock (RXCLK)
7. Releases all MAC/Repeater Interface pins, which takes a maximum of 640 ns after the reset condition is removed

5.1.1.3 Hot Insertion

As with the ICS 1890, the ICS1892 reset design supports ‘hot insertion’ of its MII. (That is, the ICS1892 can connect its MAC/Repeater Interface to a MAC/repeater while power is already applied to the MAC/repeater.)

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5.1.2 Specific Reset Operations

This section discusses the following specific ways that the ICS1892 can be reset:

- Hardware reset (using the RESET* pin)
- Power-on reset (applying power to the ICS1892)
- Software reset (using Control Register bit 0.15)

Note: At the completion of a reset (either hardware, power-on, or software), the ICS1892 sets all registers to their default values.

5.1.2.1 Hardware Reset

Entering Hardware Reset

Holding the active-low RESET* pin low for a minimum of five REF_IN clock cycles initiates a hardware reset (that is, the ICS1892 enters the reset state). During reset, the ICS1892 executes the steps listed in Section 5.1.1.1, “Entering Reset”.

Exiting Hardware Reset

After the signal on the RESET* pin transitions from a low to a high state, the ICS1892 completes in 640 ns (that is, in 16 REF_IN clocks) steps 1 through 5, listed in Section 5.1.1.2, “Exiting Reset”. After the first five steps are completed, the Serial Management Port is ready for normal operations, but this action does not signify the end of the reset cycle. The reset cycle completes when the transmit clock (TXCLK) and receive clock (RXCLK) are available, which is typically 53 ms after the RESET* pin goes high. [For details on this transition, see Section 10.5.17, “Reset: Hardware Reset and Power-Down”.]

Note:

1. The MAC/Repeater Interface is not available for use until the TXCLK and RXCLK are valid.
2. The Control Register bit 0.15 does not represent the status of a hardware reset. It is a self-clearing bit that is used to initiate a software reset.

5.1.2.2 Power-On Reset

Entering Power-On Reset

When power is applied to the ICS1892, it waits until the potential between V_{DD} and V_{SS} achieves a minimum voltage of 4.5 VDC before entering reset and executing the steps listed in Section 5.1.1.1, “Entering Reset”. After entering reset from a power-on condition, the ICS1892 remains in reset for approximately 20 µs. (For details on this transition, see Section 10.5.16, “Reset: Power-On Reset”.)

Exiting Power-On Reset

The ICS1892 automatically exits reset and performs the same steps as for a hardware reset. (See Section 5.1.1.2, “Exiting Reset”.)

Note: The only difference between a hardware reset and a power-on reset is that during a power-on reset, the ICS1892 isolates the RESET* input pin. All other functionality is the same. As with a hardware reset, the Control Register bit 0.15 does not represent the status of a power-on reset.

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5.1.2.3 Software Reset

Entering Software Reset

Initiation of a software reset occurs when a management entity writes a logic one to Control Register bit 0.15. When this write occurs, the ICS1892 enters the reset state for two REF_IN clock cycles.

Note: Entering a software reset is nearly identical to entering a hardware reset or a power-on reset, except that during a software-initiated reset, the ICS1892 does not enter the power-down state.

Exiting Software Reset

At the completion of a reset (either hardware, power-on, or software), the ICS1892 sets all registers to their default values. This action automatically clears (that is, sets equal to logic zero) Control Register bit 0.15, the software reset bit. Therefore, for a software reset (only), bit 0.15 is a self-clearing bit that indicates the completion of the reset process.

Note:

1. The RESET* pin is active low but Control Register bit 0.15 is active high.
2. Exiting a software reset is nearly identical to exiting a hardware reset or a power-on reset, except that upon exiting a software-initiated reset, the ICS1892 does not re-latch its Serial Management Port Address into the Extended Control Register. [For information on the Serial Management Port Address, see Section 8.11.3, “PHY Address (bits 16.10:6)”.]
3. The Control Register bit 0.15 does not represent the status of a hardware reset. It is a self-clearing bit that is used to initiate a software reset. During a hardware or power-on reset, Control Register bit 0.15 does not get set to logic one. As a result, this bit 0.15 cannot be used to indicate the completion of the reset process for hardware or power-on resets.

5.2 Power-Down Operations

The ICS1892 enters the power-down state whenever either (1) the RESET* pin is low or (2) Control Register bit 0.11 (the Power-Down bit) is logic one. In the power-down state, the ICS1892 disables all internal functions and drives all MAC/Repeater Interface output pins to logic zero except for those that support the MII Serial Management Port. In addition, the ICS1892 tri-states its Twisted-Pair Transmit pins (TP_TXP and TP_TXN) to achieve an additional reduction in power.

There is one significant difference between entering the power-down state by setting Control Register bit 0.11 as opposed to entering the power-down state during a reset. When the ICS1892 enters the power-down state:

- By setting Control Register bit 0.11, the ICS1892 maintains the value of all Management Register bits except for the latching low (LL), latching high (LH), and latching maximum (LMX) status bits. Instead, these LL, LH, and LMX Management Register bits are re-initialized to their default values.
- During a reset, the ICS1892 sets all of its Management Register bits to their default values. It does not maintain the state of any Management Register bit.

For more information on power-down operations, see the following:

- Section 8.14, “Register 19: Extended Control Register 2”
- Section 10.4, “DC Operating Characteristics”, which has tables that specify the ICS1892 power consumption while in the power-down state

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5.3 Automatic Power-Saving Operations

The ICS1892 has power-saving features that automatically minimize its total power consumption while it is operating. Table 5-1 lists the ICS1892 automatic power-saving features for the various modes.

Table 5-1. Automatic Power-Saving Features, 10Base-T and 100Base-TX Modes

Power-Saving Feature	Mode for ICS1892	
	10Base-T Mode	**100Base-TX Mode**
Disable Internal Modules	In 10Base-T mode, the ICS1892 disables all its internal 100Base-TX modules.	In 100Base-TX mode, the ICS1892 disables all its internal 10Base-T modules.
STA Control of Automatic Power-Saving Features	When an STA sets the state of the ICS1892 Extended Control Register 2, bit 19.0 to logic: • Zero, the 100Base-TX modules always remain enabled, even during 10Base-T operations. • One, the ICS1892 automatically disables 100Base-TX modules while the ICS1892 is operating in 10Base-T mode.	When an STA sets the state of the ICS1892 Extended Control Register 2, bit 19.1 to logic: • Zero, the 10Base-T modules always remain enabled, even during 100Base-TX operations. • One, the ICS1892 automatically disables 10Base-T modules while the ICS1892 is operating in 100Base-TX mode.

5.4 Auto-Negotiation Operations

The ICS1892 has an Auto-Negotiation sublayer. It provides both an input pin, ANSEL (Auto-Negotiation Select) and a Control Register bit (bit 0.12) to determine whether its Auto-Negotiation sublayer is enabled or disabled. The ICS1892 HW/SW input pin exclusively selects whether the ANSEL pin (which is used for the hardware mode) or Control Register bit 0.12 (which is used for the software mode) controls its Auto-Negotiation sublayer.

When enabled, the ICS1892 Auto-Negotiation sublayer exchanges technology capability data with its remote link partner and automatically selects the highest-performance operating mode it has in common with its remote link partner. For example, if the ICS1892 supports 100Base-TX and 10Base-T modes – but its link partner supports 100Base-TX and 100Base-T4 modes – the two devices automatically select 100Base-TX as the highest-performance common operating mode. For details regarding initialization and control of the auto-negotiation process, see Section 7.2, “Functional Block: Auto-Negotiation”.

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5.5 100Base-TX Operations

The ICS1892 100Base-TX mode is a primary operating mode that provides 100Base-TX physical layer (PHY) services as defined in the ISO/IEC 8802-3 standard. In the 100Base-TX mode, the ICS1892 is a 100M translator between a MAC/repeater and the physical transmission medium. As such, the ICS1892 has two interfaces, both of which are fully configurable: one to the MAC/repeater and one to the Link Segment. In 100Base-TX mode, the ICS1892 provides the following functions:

- Data conversion from both parallel-to-serial and serial-to-parallel formats
- Data encoding/decoding (4B/5B, NRZ/NRZI, and MLT-3)
- Data scrambling/descrambling
- Data transmission/reception over a twisted-pair medium

To accurately transmit and receive data, the ICS1892 employs DSP-based wave shaping, adaptive equalization, and baseline wander correction. In addition, in 100Base-TX mode, the ICS1892 provides a variety of control and status means to assist with Link Segment management. For more information on 100Base-TX, see Section 7.4, “Functional Block: 100Base-TX TP-PMD Operations”.

5.6 10Base-T Operations

The ICS1892 10Base-T mode is another primary operating mode that provides 10Base-T physical layer (PHY) services as defined in the ISO/IEC 8802-3 standard. In the 10Base-T mode, the ICS1892 is a 10M translator between a MAC/repeater and the physical transmission medium. As such, the ICS1892 has two interfaces, both of which are fully configurable: one to the MAC/repeater and one to the Link Segment. In 10Base-T mode, the ICS1892 provides the following functions:

- Data conversion from both parallel-to-serial and serial-to-parallel formats
- Manchester data encoding/decoding
- Data transmission/reception over a twisted-pair medium

In addition, in 10Base-T mode, the ICS1892 provides a variety of control and status means to assist with Link Segment management. For more information on 10Base-T, see Section 7.5, “Functional Block: 10Base-T Operations”.

5.7 Half-Duplex and Full-Duplex Operations

The ICS1892 supports half-duplex and full-duplex operations for both 10Base-T and 100Base-TX applications. Full-duplex operation allows simultaneous transmission and reception of data, which effectively doubles the Link Segment throughput to either 20 Mbps (for 10Base-T operations) or 200 Mbps (for 100Base-TX operations).

As per the ISO/IEC standard, full-duplex operations differ slightly from half-duplex operations. These differences are necessary, as during full-duplex operations a PHY actively uses both its transmit and receive data paths simultaneously.

- In 10Base-T full-duplex operations, the ICS1892 disables its loopback function (that is, it does not automatically loop back data from its transmitter to its receiver and disable its SQE Test function).
- In both 10Base-T and 100Base-TX full-duplex operations, the ICS1892 asserts its CRS signal only in response to receive activity while its COL signal always remains inactive.

For more information on half-duplex and full-duplex operations, see the following sections:

- Section 8.2, “Register 0: Control Register”
- Section 8.2.8, “Duplex Mode (bit 0.8)”
- Section 8.3, “Register 1: Status Register”
- Section 8.6, “Register 4: Auto-Negotiation Register”

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Chapter 6 Interface Overviews

The ICS1892 MAC/Repeater Interface is fully configurable, thereby allowing it to accommodate many different applications.

This chapter includes overviews of the following MAC/repeater-to-PHY interfaces:

- Section 6.1, “MII Data Interface”
- Section 6.2, “100M Symbol Interface”
- Section 6.3, “10M Serial Interface”
- Section 6.4, “Link Pulse Interface”
- Section 6.5, “Serial Management Interface”
- Section 6.6, “Twisted-Pair Interface”
- Section 6.7, “Clock Reference Interface”
- Section 6.8, “Configuration Interface”
- Section 6.9, “Status Interface”

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6.1 MII Data Interface

The most common configuration for the ICS1892 MAC/Repeater Interface is to configure the MAC/Repeater Interface as a Medium Independent Interface (MII) operating at either 10 Mbps or 100 Mbps (depending on the configuration). When the MAC/Repeater Interface is configured for the MII Data Interface mode, the MAC/Repeater Interface is used to transfer between the ICS1892 and the MAC/repeater framed, 4-bit parallel nibbles, along with control and status signals.

The ICS1892 implements an MII that is fully compliant with the IEEE Std 802.3u when connecting to MACs or repeaters. The ICS1892 MII supports a variety of interfaces to MACs and repeaters, which can occur as follows:

- On the same board (that is chip to chip)
- On a motherboard to a daughterboard
- Through an MII connector and cable (in a manner similar to AUI connections)

Clause 22 of the ISO/IEC standard defines the MII between an Ethernet PHY and the MAC/Reconciliation sublayer for 10-Mbps and 100-Mbps operations. The specification supports a variety of physical media, including 100Base-TX, 100Base-T4, and 100Base-FX. The specification is such that use of a specific medium for the Link Segment is transparent to the MAC. The ICS1892 supports this definition for both 100Base-TX and 10Base-T operations.

The ISO/IEC-specified MII has both a transmit and a receive data path. Each data path can synchronously exchange 4 bits of data (that is, nibbles).

- The transmit data path includes the following:
  - A data nibble, TXD[3:0]
  - A transmit data clock to synchronize transfers, TXCLK
  - A transmit enable signal, TXEN
  - A transmit error signal, TXER
- The receive data path includes the following:
  - A separate data nibble, RXD[3:0]
  - A receive data clock to synchronize transfers, RXCLK
  - A receive data valid signal, RXDV
  - A receive error signal, RXER

Both the transmit clock and the receive clock are provided to the MAC/Reconciliation sublayer by the ICS1892 (that is, the ICS1892 sources the TXCLK and RXCLK signals).

Clause 22 also defines as part of the MII a Carrier Sense signal (CRS) and a Collision Detect signal (COL). The ICS1892 is fully compliant with these definitions and sources both of these signals to the MAC/repeater. When operating in:

- Half-duplex mode, the ICS1892 asserts the Carrier Sense signal when data is being either transmitted or received. While operating in half-duplex mode, the ICS1892 also asserts the Collision Detect signal to indicate that data is being received while a transmission is in progress.
- Full-duplex mode, the ICS1892 asserts the Carrier Sense signal only when receiving data and forces the Collision Detect signal to remain inactive.

As mentioned in Section 5.1.1.3, “Hot Insertion”, the ICS1892 design allows hot insertion of its MII. That is, it is possible to connect its MII to a MAC when power is already applied to the MAC. To support this functionality, the ICS1892 isolates its MII signals and tri-states the signals on the Twisted-Pair Transmit pins (TP_TXP and TP_TXN) during a power-on reset. Upon completion of the reset process, the ICS1892 enables its MII and enables its Twisted-Pair Transmit signals.

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6.2 100M Symbol Interface

The 100M Symbol Interface has a primary objective of supporting 100Base-TX repeater applications for which the repeater requires only recovered parallel data and for which the repeater provides all the necessary framing and control functions.

When the Mac/Repeater Interface is configured for 100M Symbol operations, the ICS1892 and the MAC/repeater exchange unframed 5-bit, parallel symbols at a 25-MHz clock rate.

The ICS1892 configuration functions determine the operation of the MAC/Repeater Interface. The configuration functions are controlled by either input pins (in which case, the HW/SW pin is logic zero to select the hardware mode) or Management Register bits (in which case, the HW/SW pin is logic one to select the software mode).

- In hardware mode, the ICS1892 enables the 100M Symbol Interface when both of the following are true:
  - The MII/SI input pin is logic one (that is, the selection is for the Symbol Interface).
  - The 10/100SEL input pin is logic one (that is, the selection is for 100M operations).
- In software mode, the ICS1892 enables the 100M Symbol Interface when both the following are true:
  - The MII/SI input pin is logic one (that is, the selection is for the Symbol Interface).
  - The Control Register Data Rate bit (bit 0.13) is set to logic one (that is, the selection is for selecting 100M operations)

Note: In software mode, the 10/100SEL pin becomes an output that indicates the state of bit 0.13.

The 100M Symbol Interface bypasses the ICS1892 PCS and provides a direct unscrambled, unframed, 5-bit interface between the MAC/repeater and the PMA sublayer. A benefit of bypassing the PCS is a reduction in the latency through the ICS1892. That is, when the ICS1892 MAC/Repeater Interface is configured as a 100M Symbol Interface, the bit delays through the ICS1892 are smaller than the standard MII Data Interface can allow. The ICS1892 provides this 100M Symbol Interface primarily for Repeater applications, for which latency is a critical performance parameter.

In addition to the exchange of symbol data, the ICS1892 provides ISO/IEC-compliant control signals (such as CRS) to the MAC/repeater. The ICS1892 CRS signal provides a fast look-ahead, which can benefit a repeater application.

In the 100M Symbol Interface mode, the ICS1892 continues to assert the CRS signal using its PCS logic. This action does not affect the bit delay or latency because the PCS CRS logic examines the bits received from the PMA sublayer serially. In fact, because the PCS CRS does not wait for a nibble or symbol to be constructed, the PCS CRS is available in advance of the symbol generation. Therefore, by employing the PCS CRS generation logic, the ICS1892 can provide an ‘early’ indication of a Carrier Detect to the MAC/repeater.

The 100M Symbol Interface consists of the following fourteen signals: STCLK, STD[4:0], SRCLK, SRD[4:0], SCRS, and SD. (When the ICS1892 MAC/Repeater Interface is configured for 100M Symbol operations, its default MII pin names and their associated functions are redefined. For more information, see Section 9.2.4.2, “MAC/Repeater Interface Pins for 100M Symbol Interface”.)

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Table 6-1 lists the pin mappings for the ICS1892 100M Symbol Interface mode.

Table 6-1. Pin Mappings for 100M Symbol Interface Mode

Default 10M / 100M MII Pin Names	MAC/Repeater Interface Pin Mappings, Configured for 100M Symbol Interface Mode
COL	No connect. [Because the MAC/repeater sources both active and 'idle' data, a PHY cannot distinguish between an active and idle transmission channel (that is, to a PHY the transmit channel always appears active). Therefore, a PHY cannot accurately detect a collision.]
CRS	SCRS
LSTA	SD
MDC	MDC
MDIO	MDIO
RXCLK	SRCLK
RXD0	SRD0
RXD1	SRD1
RXD2	SRD2
RXD3	SRD3
RXDV	No connect. (Data exchanged between the MAC/repeater and a PHY is not framed in the 100M Symbol Interface mode. Therefore, RXDV has no meaning.)
RXER	SRD4
TXCLK	STCLK
TXD0	STD0
TXD1	STD1
TXD2	STD2
TXD3	STD3
TXEN	No connect. (100Base-TX operations require continuous transmission of data. Therefore, the MAC/repeater is responsible for sourcing IDLE symbols when it is not transmitting data.)
TXER	STD4

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6.3 10M Serial Interface

When the Mac/Repeater Interface is configured as a 10M Serial Interface, the ICS1892 and the MAC/repeater exchange a framed, serial bit stream along with associated control signals. The 10M Serial Interface configuration is ideally suited to applications that already incorporate a serial 10Base-T MAC with a standard '7-wire' interface. The ICS1892 MAC/Repeater Interface can be configured for 10M Serial Interface operations, as determined by ICS1892 configuration functions. When the HW/SW pin is set for:

- Hardware mode, the 10M Serial Interface is selected when the following are true:
  - The MII/SI input pin is logic one (that is, the selection is for a Serial Interface).
  - The 10/100SEL input pin is logic zero (that is, the selection is for 10M operations).
  - The 10/LP input pin is logic zero
- Software mode, the 10M Serial Interface is selected when the following are true:
  - The MII/SI input pin is logic one (that is, the selection is for a Serial Interface).
  - The Control Register Data Rate bit (bit 0.13) is logic zero (that is, the selection is for 10M operations).
  - The 10/LP input pin is logic zero

Note: In software mode, the 10/100SEL pin becomes an output that indicates the state of bit 0.13.

The 10M Serial Interface has two data paths: one for data transmission and one for data reception. Each data path exchanges a serial bit stream with the MAC/repeater at a 10-MHz clock rate. A benefit of using the 10M Serial Interface – in contrast to the 10M MII Interface – is a reduction in the bit latency through the ICS1892. This reduction is attributed to the elimination of both parallel-to-serial and serial-to-parallel data conversions.

The 10M Serial Interface consists of the following nine signals: 10TCLK, 10TXEN, 10TD, 10RCLK, 10RXDV, 10RD, 10CRS, 10COL, and LSTA. (When the ICS1892 MAC/Repeater Interface is configured for 10M Serial operations, both its default MII pin names and their associated functions are redefined. For more information, see Section 9.2.4.3, "MAC/Repeater Interface Pins for 10M Serial Interface".)

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Table 6-2 lists the pin mappings for the ICS1892 10M Serial Interface mode.

Table 6-2. Pin Mappings for 10M Serial Interface Mode

Default 10M / 100M MII Pin Names	MAC/Repeater Interface Pin Mappings, Configured for 10M Serial Interface Mode
COL	10COL
CRS	10CRS
LSTA	LSTA
MDC	MDC
MDIO	MDIO
RXCLK	10RCLK
RXD0	10RD
RXD1, RXD2, RXD3	No connect. [Data reception is serial, so only the 10RD (RXD0) pin is needed.]
RXDV	10RXDV
RXER	No connect. (10Base-T mode does not support error generation or detection.)
TXCLK	10TCLK
TXD0	10TD
TXD1, TXD2, TXD3	No connect. [Data transmission is serial, so only the 10TD (TXD0) pin is needed.]
TXEN	10TXEN
TXER	No connect. (0Base-T mode does not support error generation or detection.)

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6.4 Link Pulse Interface

The Link Pulse Interface allows an application to control each step in the auto-negotiation process except for the actual generation and reception of 10Base-T link pulses (that is, Normal Link Pulses). The ICS1892 MAC/Repeater Interface can be configured as a Link Pulse Interface as determined by ICS1892 configuration functions.

The Link Pulse Interface is selected as follows:

- The HW/SW pin must be set for the hardware setting (logic low).
- The MII/SI input pin must be set for the Symbol/Serial Interface (logic high).
- The 10/LP input pin must be set for Link Pulse mode (logic high).
- The 10/100SEL input pin must be set for 100M operations (logic high).

Although the 10/100SEL pin must be set for 100M operations, a Normal Link Pulse has the same ISO/IEC definition regardless of whether the 10/100SEL pin is set for 10M (10 MHz) or 100M (100 MHz.)

The Link Pulse Interface allows the MAC/repeater to control the transmission of Normal Link Pulses to the remote link partner, thereby allowing the MAC/repeater to control the auto-negotiation processes.

The Link Pulse Interface consists of the following five signals: LTCLK, LPTX, LRCLK, LPRX, and SD. (When the ICS1892 MAC/Repeater Interface is configured for Link Pulse operations, its default MII pins are redefined. For more information, see Section 9.2.4.4, “MAC/Repeater Interface Pins for Link Pulse Interface”.)

Table 6-3 lists the ICS1892 pin mappings for the ICS1892 Link Pulse Interface mode.

Table 6-3. Pin Mappings for Link Pulse Interface Mode

Default 10M / 100M MII Pin Names	MAC/Repeater Interface Pin Mappings, Configured for Link Pulse Interface Mode
COL	No connect
CRS	No connect
LSTA	SD
MDC	MDC
MDIO	MDIO
RXCLK	LRCLK
RXD0, RXD1, RXD2, RXD3	No connect
RXDV	No connect
RXER	LPRX
TXCLK	LTCLK
TXD0, TXD1, TXD2, TXD3	No connect
TXEN	No connect
TXER	LPTX

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6.5 Serial Management Interface

The ISO/IEC 8802-3 standard specifies a two-wire Serial Management Interface and protocol as part of the MII. This interface is used to exchange configuration, control, and status information between a Station Management entity (an STA) and a physical layer device (a PHY). The ISO/IEC standard specifies a frame structure and protocol for this interface as well as a set of Management Registers that it can access. The ICS1892 implementation of this interface complies fully with the ISO/IEC standard. It provides a bi-directional data pin (MDIO) along with an input pin for the clock (MDC). The clock is used to synchronize all data transfers between a PHY and the STA.

In addition to the ISO/IEC defined registers, the ICS1892 provides several extended status and control registers to provide more refined control of the MII and MDI interfaces. For example, the QuickPoll Detailed Status Register provides the ability to acquire the most-important status functions with a single MDIO read.

In the ICS1892, the MDIO and MDC pins remain active for all the MAC/Repeater Interface modes, that is, 10M/100M MII, 100M Symbol, 10M Serial, and Link Pulse. Therefore, to the ICS1892 the signals from these pins represent the Serial Management Interface, not just the MII Management Interface.

6.6 Twisted-Pair Interface

The ICS1892 twisted-pair interface consists of the following:

- Twisted-Pair Transmitter: The differential Twisted-Pair Transmit pins TP_TXP and TP_TXN
- Twisted-Pair Receiver: The differential Twisted-Pair Receive pins TP_RXP and TP_RXN
- Transmit current-select pins: 10TCSR and 100TCSR

The ICS1892 uses the same pins for both 10Base-T and 100Base-TX operating modes. The differential Twisted-Pair Transmit and Twisted-Pair Receive pins directly interface with a universal magnetic module, which in turn interfaces with a single RJ-45 connector. The universal magnetic module has two isolation transformers: one for the transmit channel and one for the receive channel. The isolation transformers provide the interface between the ICS1892 and the twisted-pair medium.

6.7 Clock Reference Interface

The REF_IN and REF_OUT pins provide the ICS1892 Clock Reference Interface. The ICS1892 requires a single clock reference with a frequency of 25 MHz ±50 parts per million. This accuracy is necessary to meet the interface requirements of the ISO/IEE 8802-3 standard, specifically clauses 22.2.2.1 and 24.2.3.4.

The ICS1892 supports three clock source configurations. The clock source can be from (1) an oscillator, (2) a CMOS driver, or (3) a crystal. The following paragraphs offer specific design recommendations for these clock sources.

6.7.1 Clock Source: Oscillator or CMOS Driver

When using either an oscillator or a CMOS driver, the design must provide a connection from the clock source to the ICS1892 REF_IN pin while leaving the ICS1892 REF_OUT pin unconnected. ICS also recommends that the design provide a dedicated driver for the REF_IN pin.

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6.7.2 Clock Source: Crystal

Figure 6-1 shows the recommended configuration when a crystal is used to supply the ICS1892 clock source. As shown, connect the two leads of the crystal between the ICS1892 pins REF_IN and REF_OUT. To properly load the crystal, also add two capacitors (C1 and C2 of Figure 6-1): one connected between REF_IN and ground (digital domain) and one connected between REF_OUT and ground (digital domain).

Note: Because a crystal is a tuned RLC circuit, crystal loading has a significant impact on the clock source accuracy.

As revealed by an impedance analysis of the recommended crystal configuration circuit, capacitors C1 and C2 are in series. In addition, the circuit has stray capacitance, which Figure 6-1 shows as CS3 and CS4. This stray capacitance is the collective result of board layout and pad capacitance.

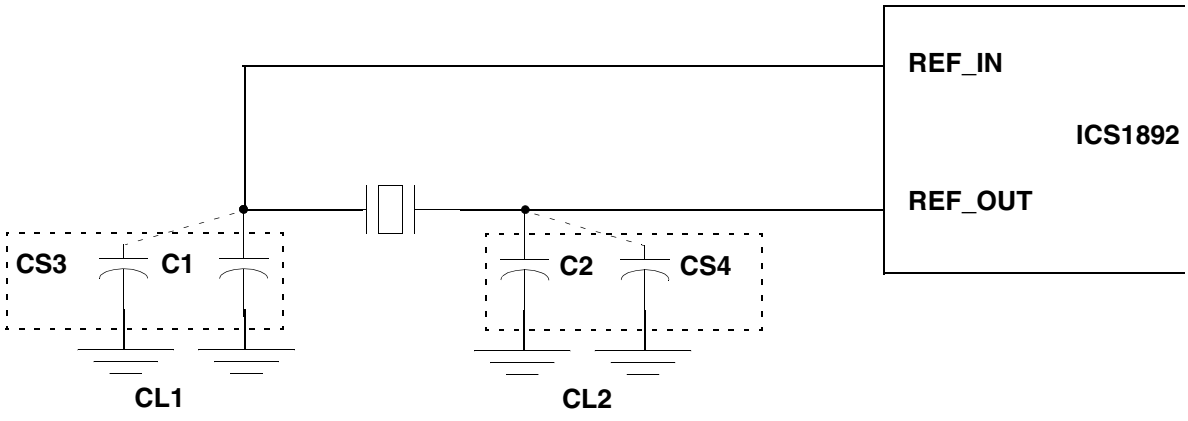
Stray capacitance CS3 is in parallel with C1, depicted cumulatively as CL1. Stray capacitance CS4 is in parallel with C2, depicted cumulatively as CL2. Therefore, the total capacitive load as viewed by the crystal is the series sum of the two capacitors CL1 and CL2. (To add capacitors in series, add their inverse.)

If the capacitors C1 and C2 have the same value (which is recommended), then CL1 = CL2. In this case, each capacitance CL1 and CL2 equals twice the rated load capacitance of the crystal. For example, if CS3 = CS4 = 5 pF, and the rated capacitive load of the crystal is 25 pF, then C1 = C2 = 45 pF. (CL1 = CL2 = 50 pF. Therefore, CL1 in parallel with CL2 equals 25 pF.)

Crystal accuracy is affected by load capacitance. The following factors also affect the crystal accuracy and must be considered when selecting a crystal for a design:

- The crystal cut. The crystal must be cut for accuracy. In some cases, this cut can require using a fixture that has equivalent capacitive loading characteristics as the final application.
- The crystal temperature characteristics
- The crystal aging characteristics
- CL1 and CL2, that is, the specific capacitive loading that occurs as a result of the particular printed circuit board that is used and the board layout

Figure 6-1. Recommended Configuration for a Crystal Clock Source



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6.8 Configuration Interface

The Configuration and Status Interface pins (10/100SEL, 10/LP, ANSEL, DPXSEL, HW/SW, MII/SI, NOD/REP, RESET* and RXTRI) allow the ICS1892 to be completely configured and controlled in hardware. With these pins, the ICS1892 can accommodate the following:

- 10M or 100M operations
- 5 MAC/Repeater Interface configurations:
  - 10M MII
  - 100M MII
  - 100M Symbol
  - 10M Serial
  - Link Pulse
- Node or repeater applications
- Full-duplex or half-duplex data links

In addition to the ISO/IEC-specified, MII control signals, the ICS1892 provides RXTRI, which is a tri-state enable pin for the MII receive data path. When this pin is active (that is, a logic one), the pins RXCLK, RXD[3:0], RXER, and RXDV are all tri-stated. Functionally, this pin affects the MII receive channel in the same way as the Control Register's isolate bit, bit 0.10. (The isolate bit also affects the transmit data path.) The ICS1892 can tri-state these seven signals for all five types of MAC/Repeater Interface configurations, not just the MII interface.

6.9 Status Interface

The ICS1892 LSTA pin provides a Link Status, and the LOCK pin provides a Stream Cipher Locking Status. In addition, as listed in Table 6-4, the ICS1892 provides the five multiplexed pins that monitor the data link by providing signals that drive LEDs. (Table 9.2.2 lists the pin numbers.)

Table 6-4. Pins for Monitoring the Data Link

Pin	LED Driven by the Pin's Output Signal
P0AC	AC (Link **Ac**tivity) LED
P1CL	CL (**Col**lisions) LED
P2LI	LI (**L**ink **I**ntegrity) LED
P3TD	TD (**T**ransmit **D**ata) LED
P4RD	RD (**R**eceive **D**ata) LED

The ICS1892 multiplexes each of these five LED output signals with one of the five PHY address inputs. The following example shows how this multiplexing takes place:

1. The PHY Address bit P0 and the link activity LED (AC) share pin 58. During a reset of the ICS1892, the signal on the link activity LED pin (as well as the other four LED pins) become inputs.
2. When the ICS1892 leaves the reset state, it latches the state of these inputs into the PHY Address bits (that is, the Serial Management Port Address) described in Table 8-16.
3. Next, the ICS1892 converts these pin signals to output signals that can drive an LED directly as follows: The state/value of each PHY Address bit is selected by connecting its associated LED signal to either V_{DD} (to select a logic one) or V_{SS} (to select a logic zero).
4. After the reset process completes, the ICS1892 uses the latched PHY address to drive the LED, independent of its connection to V_{DD} or V_{SS}.

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Chapter 7 Functional Blocks

This chapter discusses the following ICS1892 functional blocks.

- Section 7.1, “Functional Block: Media Independent Interface”
- Section 7.2, “Functional Block: Auto-Negotiation”
- Section 7.3, “Functional Block: 100Base-X PCS and PMA Sublayers”
- Section 7.4, “Functional Block: 100Base-TX TP-PMD Operations”
- Section 7.5, “Functional Block: 10Base-T Operations”
- Section 7.6, “Functional Block: Management Interface”

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7.1 Functional Block: Media Independent Interface

All ICS1892 MII interface signals are fully compliant with the ISO/IEC 8802-3 standard. In addition, the ICS1892 MIIs can support two data transfer rates: 25 MHz (for 100Base-TX operations) and 2.5 MHz (for 10Base-T operations).

The Media Independent Interface (MII) consists of two primary components:

1. An interface between a MAC (Media Access Control sublayer) and the PHY (that is, the ICS1892). This MAC-PHY part of the MII consists of three subcomponents:
   a. A synchronous Transmit interface that includes the following signals:
      (1) A data nibble, TXD[3:0]
      (2) An error indicator, TXER
      (3) A delimiter, TXEN
      (4) A clock, TXCLK
   b. A synchronous Receive interface that includes the followings signals:
      (1) A data nibble, RXD[3:0]
      (2) An error indicator, RXER
      (3) A delimiter, RXDV
      (4) A clock, RXCLK
   c. A Media Status or Control interface that consists of a Carrier Sense signal (CRS) and a Collision Detection signal (COL).
2. An interface between the PHY (the ICS1892) and an STA (Station Management entity). The STA-PHY part of the MII is a two-wire, Serial Management Interface that consists of the following:
   a. A clock (MDC)
   b. A synchronous, bi-directional data signal (MDIO) that provides an STA with access to the ICS1892 Management Register set

The ICS1892 Management Register set (discussed in Chapter 8, “Management Register Set”) consists of the following:

- Basic Management registers.

  As defined in the ISO/IEC 8802-3 standard, these registers include the following:
  – Control Register (register 0), which handles basic device configuration
  – Status Register (register 1), which reports basic device capabilities and status
- Extended Management registers.

  As defined in the ISO/IEC 8802-3 standard, the ICS1892 supports Extended registers that provide access to the Organizationally Unique Identifier and all auto-negotiation functionality.
- ICS (Vendor-Specific) Management registers.

  The ICS1892 provides vendor-specific registers for enhanced PHY operations. Among these is the QuickPoll Detailed Status Register that provides a comprehensive and consolidated set of real-time PHY information. Reading the QuickPoll register enables the MAC to obtain comprehensive status data with a single register access.

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7.2 Functional Block: Auto-Negotiation

The auto-negotiation logic of the ICS1892 has the following main functions:

- To determine the capabilities of the remote link partner, (that is, the device at the other end of the link segment's medium or cable)
- To advertise the capabilities of the ICS1892 to the remote link partner
- To establish a protocol with the remote link partner using the highest-performance operating mode that they have in common

The design of the ICS1892 Auto-Negotiation sublayer supports both legacy 10Base-T connections as well as new connections that have multiple technology options for the link. For example, when the ICS1892 has the auto-negotiation process enabled and it is operating with a 10Base-T remote link partner, the ICS1892 monitors the link and automatically selects the 10Base-T operating mode – even though the remote link partner does not support auto-negotiation. This process, called parallel detection, is automatic and transparent to the remote link partner and allows the ICS1892 to function seamlessly with existing legacy network structures without any management intervention.

(For an overview of the auto-negotiation process, see Section 5.4, "Auto-Negotiation Operations".)

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7.2.1 Auto-Negotiation General Process

The Auto-Negotiation sublayer uses a physical signaling technique that is transparent at the packet level and all higher protocol levels. This technique builds on the link pulse mechanism employed in 10Base-T operations and is fully compliant with clause 28 of the ISO/IEC 8802-3 standard.

During the auto-negotiation process, both the ICS1892 and its remote link partner use Fast Link Pulses (FLPs) to simultaneously ‘advertise’ (that is, exchange) information on their respective technology capabilities as follows:

1. For the auto-negotiation process to take place, both the ICS1892 and its remote link partner must first both support and be enabled for Auto-Negotiation.
2. The ICS1892 obtains the data for its FLP bursts from the Auto-Negotiation Advertisement Register (Register 4).
3. Both the ICS1892 and the remote link partner substitute Fast Link Pulse (FLP) bursts in place of the Normal Link Pulses (NLPs). In each FLP burst, the ICS1892 transmits information on its technology capability through its Link Control Word, which includes link configuration and status data.
4. Similarly, the ICS1892 places the Auto-Negotiation data received from its remote link partner's FLP bursts into the Auto-Negotiation Link Partner Ability Register (Register 5).
5. After the ICS1892 and its remote link partner exchange technology capability information, the ICS1892 Auto-Negotiation sublayer contrasts the data in Registers 4 and 5 and automatically selects for the operating mode the highest-priority technology that both Register 4 and 5 have in common. (That is, both the ICS1892 and its remote link partner use a predetermined priority list for selecting the operating mode, thereby ensuring that both sides of the link make the same selection.) As follows from Annex 28B of the ISO/IEC 8802-3 standard, the pre-determined technology priorities are listed from 1 (highest priority) to 5 (lowest priority):

   (1) 100Base-TX full duplex

   (2) 100Base-T4. (The ICS1892 does not support this technology.)

   (3) 100Base-TX (half duplex)

   (4) 10Base-T full duplex

   (5) 10Base-T (half duplex)

   Table 7-1 shows an example of how the selection process of the highest-priority technology takes place.

Table 7-1. Example of Selection Process of Highest-Priority Technology

If Register 4 Has These Technologies:	If Register 5 Has These Technologies:	Resulting Highest-Priority Common Technology from Auto-Negotiation Sublayer
(3) 100Base-TX half duplex	(1) 100Base-TX full duplex	(3) 100Base-TX half duplex
(4) 10Base-T full duplex	(3) 100Base-TX half duplex	

6. To indicate that the auto-negotiation process is complete, the ICS1892 sets bits 1.5 and 17.4 high to logic one. After successful completion of the auto-negotiation process, the ICS1892 Auto-Negotiation sublayer performs the following steps:
   a. It sets to logic one the Status Register’s Auto-Negotiation Complete bit (bit 1.5, which is also available in the QuickPoll register as bit 17.4).
   b. It enables the negotiated link technology (such as the 100Base Transmit modules and 100Base Receive modules).
   c. It disables the unused technologies to reduce the overall power consumption.

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7.2.2 Auto-Negotiation: Parallel Detection

The ICS1892 supports parallel detection. It is therefore compatible with networks that do not support the auto-negotiation process. When enabled, the Auto-Negotiation sublayer can detect legacy 10Base-T link partners as well as 100Base-TX link partners that do not have an auto-negotiation capability.

The Auto-Negotiation sublayer performs this parallel detection function when it does not get a response to its FLP bursts. In these situations, the Auto-Negotiation sublayer performs the following steps:

1. It sets the LP_AutoNeg_Able bit (bit 6.0) to logic zero, thereby identifying the remote link partner as not being capable of executing the auto-negotiation process.
2. It sets the bit in the Auto-Negotiation Link Partner Abilities Register that corresponds to the 'parallel detected' technology [for example, half-duplex, 10Base-T (bit 5.5) or half-duplex, 100Base-TX (bit 5.7)]. IEEE specification allows only half-duplex operation with auto-negotiation paralled detect partners.
3. It sets the Status Register's Auto-Negotiation Complete bit (bit 1.5) to logic one, indicating completion of the auto-negotiation process.
4. It enables the detected link technology and disables the unused technologies.

A remote link partner that does not support the auto-negotiation process does not respond to the transmitted FLP bursts. The ICS1892 detects this situation and responds according to the data it receives. The ICS1892 can receive one of five potential responses to the FLP bursts it is transmitting: FLP bursts, 10Base-T link pulses (that is, Normal Link Pulses), scrambled 100Base IDLEs, nothing, or a combination of signal types.

A 10Base-T link partner transmits only Normal Link Pulses when idle. When the ICS1892 receives Normal Link Pulses, it concludes that the remote link partner is a device that can use only 10Base-T technology. A 100Base-TX node without an Auto-Negotiation sublayer transmits 100M scrambled IDLE symbols in response to the FLP bursts. Upon receipt of the scrambled IDLEs, the ICS1892 concludes that its remote link partner is a 100Base-TX node that does not support the auto-negotiation process. For both 10Base-T and 100Base-TX nodes without an Auto-Negotiation sublayer, the ICS1892 clears bit 6.0 to logic zero, indicating that the link partner cannot perform the auto-negotiation process.

If the remote link partner responds to the FLP bursts with FLP bursts, then the link partner is a 100Base-TX node that can support the auto-negotiation process. In this case, the ICS1892 sets to logic one the Auto-Negotiation Expansion Register's Link Partner Auto-Negotiation Ability bit (bit 6.0).

If the Auto-Negotiation sublayer does not receive any signal when monitoring the receive channel, then the QuickPoll Detailed Status Register's Signal Detect bit (bit 17.3) is set to logic one, indicating that no signal is present.

Another possibility is that the ICS1892 senses that it is receiving multiple technology indications. In this situation, the ICS1892 cannot determine which technology to enable. It informs the STA of this problem by setting to logic one the Auto-Negotiation Expansion Register's Parallel Detection Fault bit (bit 6.4).

7.2.3 Auto-Negotiation: Remote Fault Signaling

If the remote link partner detects a fault, the ICS1892 reports the remotely detected fault to the STA by setting to logic one the Remote Fault Detected bit(s), 1.4, 5.13, and 17.1. The reception of a remote link fault during the technology exchange also indicates that the remote link partner can perform remote fault detection and the Remote Fault bit (bit 19.13) is set to logic one. In general, the reception of a remote fault means that the remote link partner has a problem with the integrity of its receive channel.

Similarly, if the ICS1892 detects a link fault, it transmits a remote fault-detected condition to its remote link partner. In this situation, the ICS1892 sets to logic one the Auto-Negotiation Link Partner Ability Register's Remote Fault Indication bit (bit 5.13). In addition, the ICS1892 sets to logic one the Extended Control Register's bit 19.13, indicating that it sent a remote fault to its remote link partner.

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7.2.4 Auto-Negotiation: Reset and Restart

If enabled, execution of the ICS1892 auto-negotiation process occurs at power-up and upon management request. There are two primary ways to begin the Auto-Negotiation state machine:

- ICS1892 reset
- Auto-Negotiation Restart

7.2.4.1 Auto-Negotiation Reset

During a reset, the ICS1892 initializes its Auto-Negotiation sublayer modules to their default states. (That is, the Auto-Negotiation Arbitration State Machine and the Auto-Negotiation Progress Monitor reset to their idle states.) In addition, the Auto-Negotiation Progress Monitor status bits are all set to logic zero. This action occurs for any type of reset (hardware reset, software reset, or power-on reset).

7.2.4.2 Auto-Negotiation Restart

As with a reset, during an Auto-Negotiation restart, the ICS1892 initializes the Auto-Negotiation Arbitration State Machine and the Auto-Negotiation Progress Monitor modules to their default states. However, during an Auto-Negotiation Restart, the Auto-Negotiation Progress Monitor status bits maintain their current state. Only three events can alter the state of the Auto-Negotiation Progress Monitor status bits after a Restart: (1) an STA read operation, (2) a reset, or (3) the Auto-Negotiation Arbitration State Machine progressing to a higher state or value.

The Auto-Negotiation Progress Monitor Status bits change only if they are progressing to a state with a value greater than their current state (that is, a state with a higher logical value than that of their current state). For a detailed explanation of these bits and their operation, see Section 7.2.5, “Auto-Negotiation: Progress Monitor”.

After the Auto-Negotiation Arbitration State Machine reaches its final state (which is Auto-Negotiation Complete), only an STA read of the QuickPoll Detailed Status Register or an ICS1892 reset can alter these status bits.

Any one of the following situations initiate a restart of the ICS1892 Auto-Negotiation sublayer:

- A link failure
- In software mode (that is, HW/SW pin is logic one), either of the following actions initiate a restart of the ICS1892 Auto-Negotiation sublayer:
  - Writing a logic one to the Control Register’s Restart Auto-Negotiation bit (bit 0.9), which is a self-clearing bit.
  - Toggling the Control Register’s Auto-Negotiation Enable bit (bit 0.12) from a logic one to a logic zero, and back to a logic one.
- In hardware mode (that is, HW/SW pin is a logic zero), toggling the ANSEL (Auto-Negotiation Select) pin from a logic one to a logic zero, and back to a logic one.

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7.2.5 Auto-Negotiation: Progress Monitor

Under typical circumstances, the Auto-Negotiation sublayer can establish a connection with the ICS1892's remote link partner. However, some situations can prevent the auto-negotiation process from properly achieving this goal. For these situations, the ICS1892 has an Auto-Negotiation Progress Monitor to provide detailed status information to its Station Management (STA) entity. With this status information, the STA can diagnose the failure mechanism and – in some situations – establish the link by correcting the problem.

When enabled, the auto-negotiation process typically requires less than 500 ms to execute, independent of the link partner's ability to perform the auto-negotiation process. Typically, an STA polls both the Auto-Negotiation Complete bit (bit 1.5) and the Link Status bit (bit 1.2) to determine when a link is successfully established, either through auto-negotiation or parallel detection. The STA can then poll the Auto-Negotiation Link Partner Ability Register and determine the highest-performance operating mode in common with the capabilities it is advertising.

The ISO/IEC-defined priority table determines the established link type. As a simpler alternative, the STA can read the QuickPoll Detailed Status Register and determine the link type from the Data Rate bit (bit 17.15) and the Duplex bit (bit 17.14). For convenience, the QuickPoll Register also includes the Link Status bit (bit 17.0) and the Auto-Negotiation Complete bit (bit 17.4).

If (1) the auto-negotiation process does not complete, or (2) the link is not established, or (3) both the auto-negotiation process does not complete and the link is not established, then the STA can determine the cause of the link failure by using the outputs of the ICS1892 Auto-Negotiation Progress Monitor.

The Auto-Negotiation Progress Monitor provides the STA with four status bits of data to indicate both the history and the present state of the auto-negotiation process. This status data is provided in the QuickPoll Detailed Status register by using the Auto-Negotiation Complete bit (bit 17.4) as well as bits 17.13:11. The bit order, from most-significant bit to least-significant bit, is 17.4, 17.13, 17.12, and 17.11. Using these four bits, the Auto-Negotiation Progress Monitor provides nine state codes detailing the operation of the auto-negotiation process for the STA. [For more information, see Section 8.12.3, "Auto-Negotiation Progress Monitor (bits 17.13:11)".]

The nine Auto-Negotiation Progress Monitor state codes are 0h through 8h and Fh. The Auto-Negotiation Progress Monitor automatically latches the values of the Auto-Negotiation Arbitration State Machine into the status bits only if the value of the present state is greater than the value that is currently in the status bits.

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For example, if the status bits have a value of 3h and the auto-negotiation process moves into:

- State 1, the Auto-Negotiation Progress Monitor does not update the status bits to indicate the new state.
- State 5, the Auto-Negotiation Progress Monitor updates the status bits to indicate the new state, State 5. In this case, the status bits increase in value until either the auto-negotiation process successfully completes or the STA reads the Auto-Negotiation Progress Monitor status bits.

  When the STA reads the status bits, the present state of the auto-negotiation process is automatically latched into the status bits, regardless of how they compare to the value currently in the latch. However, the read presents the STA with the previously latched values of the status bits, not the values just latched into the status register by the read. Therefore, the STA must perform two reads of the status bits to determine the present state of the Auto-Negotiation Arbitration State Machine.

  The first read provides a 'history' of the auto-negotiation process, (that is, the highest state achieved by the auto-negotiation process). The second read provides the present state of the auto-negotiation process. This behavior allows management to determine the greatest forward progress made by the auto-negotiation logic, which is valuable for diagnosing link errors and failures.

Note: Once the auto-negotiation process completes successfully, the value of all the Progress Monitor status bits and the Auto-Negotiation Complete bit have a value of logic one. A read operation of the QuickPoll Register provides a value of logic one for the Auto-Negotiation Complete bit and an octal value of 111 for the status bits.

However, subsequent reads of the QuickPoll Register also provide a value of logic one for the Auto-Negotiation Complete bit. The octal value of the status bits are ‘000’, providing the link remains established. That is, if the link fails, the Auto-Negotiation sublayer is restarted and subsequent reads provide the value of the Auto-Negotiation Arbitration State Machine.

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7.3 Functional Block: 100Base-X PCS and PMA Sublayers

Clause 24 of the ISO/IEC specification defines the 100Base-X Physical Coding sublayer (PCS) and Physical Medium Attachment (PMA) sublayers. The ICS1892 is fully compliant with this clause in its implementation.

7.3.1 PCS Sublayer

The ICS1892 100Base-X PCS sublayer provides two interfaces: one to a MAC/repeater and the other to the ICS1892 PMA sublayer. In addition, it performs the transmit, receive, and control functions in compliance with the ISO/IEC 8802-3 standard.

The ICS1892 100Base-X PCS PCS sublayer consists of the following:

- PCS Transmit sublayer, which provides the following:
  - Parallel-to-serial conversion
  - 4B/5B encoding
  - Collision detection
- PCS Receive sublayer, which provides the following:
  - Serial-to-parallel conversion
  - 4B/5B encoding
  - Carrier detection
  - Code group framing
- Two PCS controls, which provide the following functions for the MAC/Repeater Interface:
  - Assertion of the CRS carrier sense signal (which is part of the carrier sense modules)
  - Assertion of the COL collision detection signal (which is part of the transmit modules)

Note: When configured for 100M Symbol mode operations, the MAC/Repeater Interface bypasses most of the PCS. When the ICS1892 MAC/Repeater Interface is in this mode, most of its PCS Transmit and Receive modules are inactive. However, its PCS control functions (CRS and COL) remain operational.

7.3.2 PMA Sublayer

The ICS1892 100Base-X PMA Sublayer consists of two interfaces: one to the Physical Coding sublayer and the other to the Physical Medium Dependent sublayer. Functionally, the PMA sublayer is responsible for the following:

- Link Monitoring
- Carrier Detection
- NRZI encoding/decoding
- Transmit Clock Synthesis
- Receive Clock Recovery

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7.3.3 PCS/PMA Transmit Modules

Both the PCS and PMA sublayers have Transmit modules.

7.3.3.1 PCS Transmit Module

The ICS1892 PCS Transmit module accepts nibbles from the MAC/Repeater Interface and converts the nibbles into 5-bit 'code groups' (referred to here as 'symbols'). Then the PCS Transmit module performs a parallel-to-serial conversion on the symbols, and subsequently passes the resulting serial bit stream to the PMA sublayer.

The first 16 nibbles of each MAC/Repeater Frame represent the Frame Preamble. The PCS replaces the first two nibbles of the Frame Preamble with the Start-of-Stream Delimiter (SSD), that is, the symbols /J/K/. After receipt of the last Frame nibble, detected when TX_EN = FALSE, the PCS appends to the end of the Frame an End-of-Stream Delimiter (ESD), that is, the symbols /T/R/. (The ICS1892 PCS does not alter any other data included within the Frame.)

The PCS Transmit module also performs collision detection. When the transmission and reception of data occur simultaneously, then in compliance with the ISO/IEC specification, when the ICS1892 is in:

- Half-duplex mode, the ICS1892 asserts the collision detection signal (COL).
- Full-duplex mode, COL is always FALSE.

7.3.3.2 PMA Transmit Module

The ICS1892 PMA Transmit module accepts a serial bit stream from the PCS and converts it into NRZI format. Subsequently, the PMA passes the NRZI bit stream to the Twisted-Pair Physical Medium Dependent (TP-PMD) sublayer.

The ICS1892 PMA Transmit module uses a digital PLL to synthesize a transmit clock from the Clock Reference Interface. When the ICS1892 is configured for an interface that is:

- 10M MII (that is, 10Base-T), the TXCLK signal is 2.5 MHz
- 10M Serial Interface, the TXCLK signal is 10 MHz
- Either of the following, the TXCLK signal (a buffered version of the REF_IN signal) is 25 MHz:
  - 100M MII (that is, 100Base-TX)
  - 100M Symbol Interface

Note:

1. All of the TXCLK signals are derived from the REF_IN signal that goes to the digital PLL.
2. For the MII, for both the 10Base-T and 100Base-TX modes, the clock that is generated synchronizes all data transfers across the MII.

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7.3.4 PCS/PMA Receive Modules

Both the PCS and PMA sublayers have Receive modules.

7.3.4.1 PCS Receive Module

The ICS1892 PCS Receive module accepts both a serial bit stream and a clock signal from the PMA sublayer. The PCS Receive module converts the bit stream from a serial format to a parallel format and then processes the data to detect the presence of a carrier.

When a link is in the idle state, the PCS Receive module receives IDLE symbols. (All bits are logic one.) Upon receiving two non-contiguous zeros in the bit stream, the PCS Receive module examines the ensuing bits and attempts to locate the Start-of-Stream Delimiter (SSD), that is, the /J/K/ symbols.

Upon verification of a valid SSD, the PCS Receive module substitutes the first two standard nibbles of a Frame Preamble for the detected SSD. In addition, the PCS Receive module uses the SSD to begin framing the ensuing data into 5-bit code symbols. The final PCS Receive module performs 4B/5B decoding on the symbols and then synchronously passes the resulting nibbles to the MAC/Repeater Interface.

The Receive state machine continues to accept PMA data, convert it from serial to parallel format, frame it, decode it, and pass it to the MAC/Repeater Interface. During this time, the Receive state machine alternates between the Receive and Data States and continues this process until detection of one of the following:

- An End-of-Stream Delimiter (ESD, that is, the /T/R/ symbols)
- An error
- A premature end (IDLEs)

Upon receipt of an ESD, the Receive state machine returns to the IDLE state without passing the ESD to the MAC/Repeater Interface. Detection of an error forces the Receive state machine to assert the receive error signal (RX_ER) and wait for the next symbol. If the ICS1892 Receive state machine detects a premature end, it forces the assertion of the RX_ER signal, sets the Premature End bit (bit 17.5) to logic one, and transitions to the IDLE State.

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7.3.4.2 PMA Receive Modules

The ICS1892 PMA Receive module provides the following two functions:

- NRZI Decoding
  - The Receive module performs the NRZI decoding on the serial bit stream received from the Twisted-Pair Physical Medium Dependent (TP-PMD) sublayer. It converts the bit stream to a unipolar, positive, binary format which the PMA subsequently passes it to the PCS.
  - The PMA extracts the clock embedded in the serial data stream.
- Receive Clock Recovery

  The Receive Clock Recovery function consists of a phase-locked loop (PLL) that operates on the serial data stream received from the PMD sublayer. This PLL automatically synchronizes itself to the clock encoded in the serial data stream and then provides both a recovered clock and data stream to the PCS.

The Receive Clock PLL requires a clock reference to acquire lock. Without a clock source, it continually searches for a reference signal. Therefore, when the ICS1892 does not detect the presence of any signal on its receive channel, it uses a Transmit Clock function to generate a reference for the Receive Clock PLL. This is TBD.

The PMA Link Monitoring function observes the Receive Clock PLL. If the Receive Clock PLL cannot acquire 'lock' on the serial data stream, it asserts an error signal. The status of this error signal can be read in the QuickPoll Detailed Status Register's PLL Lock Error bit (bit 17.9). This bit is a latching high (LH) bit. (For more information on latching high and latching low bits, see Section 8.1.4.1, "Latching High Bits" and Section 8.1.4.2, "Latching Low Bits".)

In general, the ICS1892 PMA Link Monitor functions continually audit the state of the connection with the remote link partner. They assert a receive channel error if a receive signal is not detected or if a PLL Lock Error occurs. These errors, in turn, generate a link fault and force the link monitor functions to clear both the Status Register's Link Status bit (bit 1.2) and the QuickPoll Detailed Status Register's Link Status bit (bit 17.0).

7.3.5 PCS Control Signal Generation

For the PCS sublayer, there are two control signals: a Carrier Sense signal (CRS) and a Collision Detect signal (COL).

The CRS control signals is generated as follows:

1. When a logic zero is detected in an idle bit stream, the Receive Functions examine the ensuing bits.
2. When the Receive Functions find the first two non-contiguous zero bits, the Receive state machine moves into the Carrier Detect state.
3. As a result, the Boolean Receiving variable is set to TRUE.
4. Consequently, the Carrier Sense state machine moves into the Carrier Sense 'on' state, which asserts the CRS signal.
5. If the PCS Functions:
   a. Cannot confirm either the /I/J/ (IDLE, J) symbols or the /J/K/ symbols, the receive error signal (RX_ER) is asserted, and the Receive state machine returns to the IDLE state. In IDLE, the Boolean Receiving variable is set to FALSE, thereby causing the Carrier Sense state machine to set the CRS signal to FALSE.
   b. Can confirm the /I/J/K/ symbols, then the Receive state machine transitions to the 'Receive' state.

The COL control signal is generated by the transmit modules. For details, see Section 7.3.3.1, "PCS Transmit Module".

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7.3.6 4B/5B Encoding/Decoding

The 4B/5B coding methodology maps each 4-bit nibble to a 5-bit symbol (also called a “code group”). There are 32 five-bit symbols, which include the following:

- Of the 32 five-bit symbols, 16 five-bit symbols are required to represent the 4-bit nibbles.
- The remaining 16 five-bit symbols are available for control functions. The IEEE Standard defines 6 symbols for control, and the remaining 10 symbols of this grouping are invalid. The 6 control symbols include the following:
  - /H/ represents a Transmit Error
  - /I/ represents an IDLE
  - Two symbols represent the Start-of-Stream Delimiter (SSD): /J/ and /K/
  - Two symbols represent the End-of-Stream Delimiter (ESD): /T/ and /R/

  If the ICS1892 PCS receives:
  - One of the 10 undefined symbols, it sets the QuickPoll Detailed Status Register’s Invalid Symbol bit (bit 17.7) to logic one.
  - A Halt symbol, it sets the Halt Symbol Detected bit in the QuickPoll Detailed Status Register (bit 17.6) to logic one.

Note: By an STA (1) setting the Extended Control Register’s Transmit Invalid Codes bit (bit 16.2) to logic one and (2) asserting the TXER signal, an STA can force the ICS1892 to transmit symbols that are typically classified as invalid. For more information, see Section 8.11.7, “Invalid Error Code Test (bit 16.2)”.

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7.4 Functional Block: 100Base-TX TP-PMD Operations

The ICS1892 supports both 10Base-T and 100Base-TX operations. The ICS1892 TP-PMD modules perform 100Base-TX Twisted-Pair Physical Media Dependent (TP-PMD) stream cipher scrambling/descrambling and MLT-3 encoding/decoding (3-level, multi-level transition) in compliance with the ANSI Standard X3.263: 199X FDDI TP-PMD as called out in the ISO/IEC 8802-3 standard. The ICS1892 TP-PMD also performs DC restoration and adaptive equalization on the received signals.

Note:

1. For an overview of the 100Base-TX, see Section 5.5, “100Base-TX Operations”.
2. For more information on the Twisted-Pair Interface, see Section 6.6, “Twisted-Pair Interface”.

7.4.1 100Base-TX Operation: Stream Cipher Scrambler/Descrambler

When the ICS1892 is operating in 100Base-TX mode, it employs a stream cipher scrambler/descrambler that complies with the ANSI Standard X3.263: 199X FDDI TP-PMD. The purpose of the stream cipher scrambler is to spread the transmission spectrum to minimize electromagnetic compatibility problems. The stream cipher descrambler restores the received serial bit stream to its unscrambled form.

The MAC/Repeater Interface bypasses the stream cipher scrambler/descrambler when in the 100M Symbol Interface mode.

7.4.2 100Base-TX Operation: MLT-3 Encoder/Decoder

When operating in the 100Base-TX mode, the ICS1892 TP-PMD sublayer employs an MLT-3 encoder and decoder. During data transmission, the TP-PMD encoder converts the NRZI bit stream received from the PMA sublayer to a 3-level Multi-Level Transition code. The three levels are +1, 0, and -1. The results of MLT-3 encoding provide a reduction in the transmitted energy over the critical frequency range from 20 MHz to 100 MHz. The TP-PMD MLT-3 decoder converts the received three-level signal back to an NRZI bit stream.

7.4.3 100Base-TX Operation: DC Restoration

100Base-TX operations employ a stream cipher scrambler to minimize peak amplitudes in the frequency spectrum. However, the nature of the stream cipher and MLT-3 encoding is such that long sequences of consecutive zeros or ones can exist. These unbalanced data patterns produce an undesirable DC component in the data stream.

Baseline wander adversely affects the noise immunity of the receiver, because the ‘baseline’ signal moves or ‘wanders’ from its nominal DC value.

The ICS1892 employs a unique technique to restore the DC component ‘lost’ by the medium. As a result, the design is very robust and immune to noise, independent of the data.

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7.4.4 100Base-TX Operation: Adaptive Equalizer

The ICS1892 TP-PMD sublayer employs adaptive equalization circuitry to compensate for signal amplitude and phase distortion incurred from the transmission medium. At a data rate of 100 Mbps, the transmission medium (that is, the cable) introduces significant signal distortion because of high-frequency attenuation and phase shift. The high-frequency loss occurs primarily because of the cable skin effect that causes the conductor resistance to rise as the square of the frequency rises.

In shielded twisted-pair (STP) and unshielded twisted-pair (UTP) category 5 cables with maximum lengths of 130 meters, the ICS1892 adaptive equalizer accurately compensates for these losses.

For a UTP Category 5 cable that is 100 meters long (the maximum length as per the EIA/TIA-568-A standard), there are three distinct levels to resolve to recover the MLT-3 encoded data. As a result, the pulse shape of the received signal is critical.

The ICS1892 employs a DSP-based adaptive equalization technique to compensate for a wide range of cable lengths. The optimizing parameter for the equalizer adaptation process is the overall ICS1892 bit error rate, which provides the ICS1892 with a very high overall reliability.

7.4.5 100Base-TX Operation: Twisted-Pair Transmitter

For both 10Base-T and 100Base-TX operations, the ICS1892 uses the same Twisted-Pair Transmit pins (TP_TXP and TP_TXN) as well as the same internal functional module. The twisted-pair transmitter module is a current-driven, differential driver that can supply either of the following:

- A two-level 10Base-T (that is, Manchester-encoded) signal
- A three-level 100Base-TX (that is, MLT-3 encoded) signal

The ICS1892 interfaces with the medium through an isolation transformer (also called a magnetic module). The ICS1892 transmitter uses wave-shaping techniques to control the output signal rise and fall times (thereby eliminating the need for expensive external filters) and interfaces directly to the isolation transformer.

Note:

1. In reference to the ICS1892, the term ‘Twisted-Pair Transmitter’ refers to the set of Twisted-Pair Transmit output pins (TP_TXP and TP_TXN).
2. For information on the 10Base-T Twisted-Pair Transmitter, see Section 7.5.11, “10Base-T Operation: Twisted-Pair Transmitter”.

7.4.6 100Base-TX Operation: Twisted-Pair Receiver

Twisted-Pair Receiver operations are similar to Twister-Pair Transmitter operations, in that for both 10Base-T and 100Base-TX operations, the ICS1892 uses the same Twister-Pair Receive pins (TP_RXP and TP_RXN).

However, unlike the transmitter operations (which use the same internal functional module), the ICS1892 employs separate internal twisted-pair receiver modules to process the incoming data: one for 10Base-T operations and one for 100Base-TX operations. The internal twisted-pair receiver modules interface with the medium through an isolation transformer. The 100Base-TX receiver module accepts and processes a differential three-level 100Base-TX (that is, MLT-3 encoded) signal from the isolation transformer.

Note:

1. In reference to the ICS1892, the term ‘Twisted-Pair Receiver’ refers to the set of Twisted-Pair Receive output pins (TP_RXP and TP_RXN).
2. For information on the 10Base-T Twisted-Pair Receiver, see Section 7.5.12, “10Base-T Operation: Twisted-Pair Receiver”.

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7.4.7 100Base-TX Operation: Auto Polarity Correction (FLP)

- 100Base-TX does not have polarity but the auto-negotiation FLP are sensitive to polarity.

The ICS1892 can sense and then automatically correct a signal polarity that is reversed on its Twisted-Pair Receiver inputs. A signal polarity reversal occurs if the input signals on the TP_RXP and TP_RXN pins are crossed or swapped (a problem that can occur during network installation or wiring).

The ICS1892 corrects a reversed signal polarity by examining the signal polarity of the Normal Link Pulses. Control of this feature is provided by using the 10Base-T Operations Register bit 18.3, the Auto Polarity-Inhibit bit. When this bit is logic:

- Zero, the ICS1892 automatically senses and corrects a reversed or inverted signal polarity on its Twisted-Pair Receive pins (TP_RXP and TP_RXN).
- One, the ICS1892 disables this feature.

When the ICS1892 detects a reversed signal polarity on its Twisted-Pair Receiver pins and the Auto Polarity-Inhibit bit is also logic zero, the ICS1892 (1) automatically corrects the data stream and (2) sets the Polarity Reversed bit (bit 18.14) to logic one, to indicate to the STA that this situation exists. Bit 18.14 is a latching high (LH) bit. (For more information on latching high and latching low bits, see Section 8.1.4.1, “Latching High Bits” and Section 8.1.4.2, “Latching Low Bits”.)

Note:

1. The Auto Polarity Correction Function is primarily a 10Base-T operation. However, it is part of the Twisted-Pair Receiver and is operational during the 100Base-TX auto-negotiation process.
2. For information on the 10Base-T Auto Polarity Correction, see Section 7.5.13, “10Base-T Operation: Auto Polarity Correction”.

7.4.8 100Base-TX Operation: Isolation Transformer

As per the ISO/IEC specification, the ICS1892 interfaces with a medium through an isolation transformer. Typically, for each magnetic module there are two isolation transformers: one for the ICS1892 Twisted-Pair Transmitter and the other for the ICS1892 Twisted-Pair Receiver. For both 10Base-T and 100Base-TX operations, these isolation transformers provide both physical isolation as well as the means for coupling a signal between the ICS1892 and the medium.

Note:

1. For information on magnetic modules, see Section 6.6, “Twisted-Pair Interface”.
2. For information on the 10Base-T Isolation Transformer operation, see Section 7.5.14, “10Base-T Operation: Isolation Transformer”.

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7.5 Functional Block: 10Base-T Operations

The ICS1892 supports both 10Base-T and 100Base-TX operations. When configured for 10Base-T mode, the MAC/Repeater Interface can provide either a 10M MII (Media Independent Interface) or a 10M Serial Interface. The Twisted-Pair Interface is not configurable. ISO/IEC standards specifically define its operation. (For more information on the Twisted-Pair Interface, see Section 6.6, “Twisted-Pair Interface”.)

There are some important differences between 10Base-T and 100Base-TX operations. The 10Base-T operation is fundamentally simpler than 100Base-TX. The data rate is slower, requiring less encoding than 100Base-TX operations (that is, the bandwidth requirements and the line attenuation issues are not as severe as with 100-MHz operations). Consequently, when the ICS1892 is set for 10Base-T operations, it uses fewer sublayers in contrast to 100Base-TX operations.

For an overview of 10Base-T operations, see Section 5.6, “10Base-T Operations”.

7.5.1 10Base-T Operation: Manchester Encoder/Decoder

The ISO/IEC specification requires the use of a Manchester-encoded signal for 10Base-T operations. During transmission operations, the ICS1892 acquires data from the MAC/Repeater Interface, in either 4-bit nibbles or as a serial bit stream.

A Manchester Encoder encodes the data before passing it to the Twisted-Pair Transmitter. In a Manchester-encoded signal, all logic:

- Ones are:
  - Positive during the first half of the bit period
  - Negative during the second half of the bit period
- Zeros are:
  - Negative during the first half of the bit period
  - Positive during the second half of the bit period

During reception operations, a Manchester Decoder translates the serial bit stream obtained from the Twisted-Pair Receiver into an NRZ bit stream. The Manchester Decoder subsequently passes the data to the MAC/Repeater Interface in either serial or parallel format, depending on the interface configuration. The advantages in using Manchester-encoded signals are the following:

- Each bit period has an encoded clock.
- The split-phase nature of the signal always provides a zero DC level regardless of the data.

The primary disadvantage in using Manchester-encoded signals is that it doubles the data rate, making it operationally prohibitive for 100-MHz operations.

7.5.2 10Base-T Operation: Clock Synthesis

The ICS1892 synthesizes the clocks required for synchronizing data transmission. In 10Base-T mode, the MAC/Repeater Interface can provide either a 10M MII (Media Independent Interface) or a 10M Serial Interface. When the ICS1892 is configured to support a:

- 10M MII interface, the ICS1892 synthesizes a 2.5-MHz clock for nibble-wide transactions
- 10M Serial Interface to the MAC/repeater, the ICS1892 synthesizes a 10-MHz clock

7.5.3 10Base-T Operation: Clock Recovery

The ICS1892 recovers its receive clock from the data stream obtained from the Twisted-Pair Receiver. It employs a phase-locked loop (PLL) to recover the clock from this Manchester-encoded data. Subsequently, the ICS1892 uses this recovered clock for synchronizing the data transmission between itself and the MAC/repeater. Receive-clock PLL acquisition begins with reception of the MAC Frame Preamble and continues as long as the ICS1892 is receiving data.

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7.5.4 10Base-T Operation: Idle

The ICS1892 10Base-T Idle Function transmits link pulses in the absence of data (that is, when the MAC/repeater is not requiring it to transmit any data). During this time the link is Idle, and the 10Base-T Idle Function begins periodically transmitting link pulses at a rate of one pulse every 16 ms, as defined in the ISO/IEC 8802-3 standard. In 10Base-T mode, the ICS1892 transmits link pulses whenever the MAC/repeater does not have any data available for transmission. The ICS1892 continues transmitting link pulses while receiving data. Because link pulses indicate an idle state for a link, this situation does not generate a Collision Detect signal (COL).

7.5.5 10Base-T Operation: Link Monitor

When the ICS1892 is in 10Base-T mode, the Link Monitor Function observes the data received by the 10Base-T Twisted-Pair Receiver to determine the link status. The results of this continual monitoring are stored in the Link Status bit. The Station Management entity (STA) can access the Link Status bit in either the Status Register (bit 1.2) or the QuickPoll Detailed Status Register (bit 17.0). This Link Status bit is a latching low (LL) bit. (For more information on latching high and latching low bits, see Section 8.1.4.1, “Latching High Bits” and Section 8.1.4.2, “Latching Low Bits”.)

The STA can control the execution of the Smart Squelch Function using bit 18.0 (the Smart Squelch Inhibit bit in the 10Base-T Operations Register). The Squelch Inhibit bit allows an STA to control the ICS1892 Squelch Detection in 10Base-T mode. When an STA sets this bit to logic:

- Zero, before the ICS1892 can establish a valid link, the ICS1892 must receive valid 10Base-T data.
- One, before the ICS1892 can establish a valid link, the ICS1892 must receive both valid 10Base-T data followed by an IDL.

The criteria used by the Link Monitoring Function to declare a link either valid (that is, ‘established’ or ‘up’) or invalid (that is, ‘failed’ or ‘down’) depends upon the present state of the link and the incoming data. When the 10Base-T link is:

- Valid, the Link Monitor Function continues to report the link as valid as long as it detects either data or Normal Link Pulses (NLPs) on its Twisted-Pair Receiver. If the 10Base-T Operations Register’s Smart Squelch Inhibit bit (bit 18.0) is:
  - Enabled, before the 10Base-T link can be valid, there must be an IDL at the end of a data packet.
  - Disabled, before the 10Base-T link can be valid, all that is needed is a data packet.
- Invalid, the Link Monitor Function must detect one of three events before transitioning the link from the invalid state to the valid state. If the ICS1892 receives any of the following it changes the status of the link from invalid to valid:
  - More than seven Normal Link Pulses (NLPs)
  - Any data
  - Any data followed by a valid IDL

  The ICS1892 receives data when the Twisted-Pair Receiver phase-locked loop can acquire lock and extract the receive clock from the incoming data stream for three bit times.

  If the ICS1892 receives neither data nor NLPs (that is, the link shows either no activity or inconsistent activity) for more than 81 to 83 ms, then the ICS1892 declares the link invalid and sets the LL Link Status bit to logic zero. The LL Link Status bit remains latched in the cleared state until a reset occurs or until the STA reads it while the link is valid.

Note:

1. When the link is invalid and the ICS1892 detects the presence of data, the ICS1892 does not transition the link to the valid state until after the reception of the present packet is complete.
2. Enabling or disabling the Smart Squelch Function affects the Link Monitor function.
3. A transition from the invalid state to the valid state does not automatically update the LL Link Status bit.

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7.5.6 10Base-T Operation: Smart Squelch

The Smart Squelch Function imposes more stringent requirements on the Link Monitor Function regarding the definition of a valid link, thereby providing a level of insurance that spurious noise is not mistaken for a valid link during cable installation.

The STA can control the execution of the Smart Squelch Function using bit 18.0 (the Smart Squelch Inhibit bit in the 10Base-T Operations Register). When bit 18.0 is logic:

- Zero (the default), the ICS1892 enables the Smart Squelch Function. In this case, the Link Monitor must confirm the presence of both data and a valid IDL at the end of the packet before declaring a link valid.

  For example, in 10Base-T mode, the ICS1892 appends an IDL to the end of each packet during data transmission. The receiving PHY sees this IDL and removes it from the data stream. Enabling this function requires the receiving PHY to confirm the presence of this IDL before declaring a link valid.
- One, the ICS1892 disables or inhibits the Smart Squelch Function. In this case, the Link Monitor does not have to confirm the presence of an IDL to declare a link valid (that is, the reception of any data is sufficient).

7.5.7 10Base-T Operation: Carrier Detection

The ICS1892 10Base-T Carrier Detection Function establishes the state of the Carrier Sense signal (CRS), based upon the state of the Boolean “transmitting” and “receiving” variables. These variables indicate whether the ICS1892 is (1) transmitting data, (2) receiving data, or (3) in a collision state (that is, the ICS1892 is both transmitting and receiving data on the twisted-pair medium, as defined in the ISO/IEC 8802-3 standard). When the ICS1892 is configured for:

- Half-duplex operations, the ICS1892 asserts the CRS signal when either transmitting or receiving data.
- Full-duplex operations (or when the ICS1892 is in the Repeater mode), the ICS1892 asserts the CRS signal only when it is receiving data.

7.5.8 10Base-T Operation: Collision Detection

The ICS1892 10Base-T Collision Detection Function establishes the state of the Collision Detection signal (COL) based upon both (1) the state of the Boolean ”receiving” variable and (2) the Transmit state machine. When the ICS1892 is operating in:

- Half-duplex mode, the ICS1892 asserts the COL signal to indicate it is receiving data while transmission of data is also in progress.
- Full-duplex mode, the ICS1892 always sets the Collision Detect signal to FALSE.

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7.5.9 10Base-T Operation: Jabber

According to the ISO/IEC 8802-3 standard, a jabber function detects abnormally long transmissions and takes appropriate actions to avoid them. The ICS1892 Jabber Function monitors the data stream sent to the Twisted-Pair Transmitter to limit the maximum continuous transmission time as per the ISO/IEC 8802-3 standard. The ISO/IEC specification defines the 10Base-T Jabber activation time limit (that is, the maximum transmission time) as between 20 ms and 150 ms. The ICS1892 Jabber Function complies with this specification and has a typical Jabber timer limit of 21 ms. (For more information, see Section 10.5.19, "10Base-T: Jabber Timing".)

When the Jabber Function detects that the transmission time exceeds the maximum Jabber time limit, the ICS1892 asserts the Collision Detect (COL) signal. During this 'jabber de-activation time', the data stream is interrupted and kept from reaching the Twisted-Pair Transmitter for a typical time of 324 ms. This time complies with the ISO/IEC specification of 0.5 ±0.25 sec (that is, from 250 ms to 750 ms). During this time, when interrupting the data stream and asserting the COL signal, the ICS1892 transmits Normal Link Pulses and sets the QuickPoll Detailed Status Register's Jabber Detected bit (bit 17.2) to logic one. This bit is a latching high (LH) bit. (For more information on latching high and latching low bits, see Section 8.1.4.1, "Latching High Bits" and Section 8.1.4.2, "Latching Low Bits".)

The ICS1892 provides the Station Management entity (STA) with the ability to disable the Jabber Function with the ICS1892 Jabber Inhibit bit (the 10Base-T Operations Register's bit 18.5). Setting bit 18.5 to logic:

- Zero (the default) implements the ISO/IEC specified function, as described above.
- One disables the ISO/IEC specified Jabber Function.

7.5.10 10Base-T Operation: SQE Test

The ICS1892 has a Signal Quality Error (SQE) Test module used exclusively for 10Base-T operations. When enabled, the ICS1892 performs the SQE Test at the completion of each transmitted packet (that is, whenever the TX_EN signal transitions from high to low). When TX_EN goes low, an enabled SQE Test typically delays 630 ns and subsequently asserts the COL signal to the MAC Interface for a typical duration of 1 µs duration. The ISO/IEC specification for (1) the delay is 10 bit times, ± 5 bit times and for (2) the duration is from 0.6 to 1.6 µs. The ICS1892 SQE Test Function is:

- Enabled only when all the following conditions are true:
  - The ICS1892 is in node mode.
  - The ICS1892 is in half-duplex mode.
  - A valid link is established.
  - The 10Base-T Operations Register's SQE Test Inhibit bit (bit 18.2) is logic zero (the default).
  - The TX_EN signal has transitioned from high to low.
- Disabled whenever any of the following are true:
  - As per the ISO/IEC specification, whenever the ICS1892 is in either of the following modes:
    - Repeater mode
    - Full-duplex mode
  - As per the ISO/IEC specification, whenever the ICS1892 detects a link failure, it automatically disables the SQE Test Function.
  - The 10Base-T Operations Register's SQE Test Inhibit bit (bit 18.2) is logic one. [This bit provides the Station Management entity (STA) with the ability to disable the SQE Test function.]

Note:

1. In 10Base-T mode, a bit time = 100 ns.
2. The SQE Test also has the name 10Base-T Heartbeat. For details on the SQE waveforms, see Section 10.5.18, "10Base-T: Heartbeat Timing (SQE)".

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7.5.11 10Base-T Operation: Twisted-Pair Transmitter

For both 10Base-T and 100Base-TX operations, the ICS1892 uses the same Twisted-Pair Transmit pins (TP_TXP and TP_TXN) as well as the same internal functional module. The twisted-pair transmitter module is a current-driven, differential driver that can supply either of the following:

- A two-level 10Base-T (that is, Manchester-encoded) signal
- A three-level 100Base-TX (that is, MLT-3 encoded) signal

The ICS1892 interfaces with the medium through an isolation transformer. The ICS1892 transmitter uses wave-shaping techniques to control the output signal rise and fall times (thereby eliminating the need for expensive external filters) and interfaces directly to the isolation transformer.

Note:

1. In reference to the ICS1892, the term 'Twisted-Pair Transmitter' refers to the set of Twisted-Pair Transmit output pins (TP_TXP and TP_TXN).
2. For information on the 100Base-TX Twisted-Pair Transmitter, see Section 7.4.5, "100Base-TX Operation: Twisted-Pair Transmitter".

7.5.12 10Base-T Operation: Twisted-Pair Receiver

Twisted-Pair Receiver operations are similar to Twister-Pair Transmitter operations, in that for both 10Base-T and 100Base-TX operations, the ICS1892 uses the same Twister-Pair Receive pins (TP_RXP and TP_RXN).

However, unlike the transmitter operations (which use the same internal functional module), the ICS1892 employs separate internal twisted-pair receiver modules to process the incoming data: one for 10Base-T operations and one for 100Base-TX operations. The internal twisted-pair receiver modules interface with the medium through an isolation transformer. The 10Base-T receiver module accepts and processes a differential two-level 10Base-T (that is, Manchester-encoded) signal from the isolation transformer.

Note:

1. In reference to the ICS1892, the term 'Twisted-Pair Receiver' refers to the set of Twisted-Pair Receive output pins (TP_RXP and TP_RXN).
2. For information on the 100Base-TX Twisted-Pair Receiver, see Section 7.4.6, "100Base-TX Operation: Twisted-Pair Receiver".

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7.5.13 10Base-T Operation: Auto Polarity Correction

The ICS1892 can sense and then automatically correct a signal polarity that is reversed on its Twisted-Pair Receiver inputs. A signal polarity reversal occurs if the input signals on the TP_RXP and TP_RXN pins are crossed or swapped (a problem that can occur during network installation or wiring).

The ICS1892 corrects a reversed signal polarity by examining the signal polarity of the Normal Link Pulses. Control of this feature is provided by using the 10Base-T Operations Register bit 18.3, the Auto Polarity-Inhibit bit. When this bit is logic:

- Zero, the ICS1892 automatically senses and corrects a reversed or inverted signal polarity on its Twisted-Pair Receive pins (TP_RXP and TP_RXN).
- One, the ICS1892 disables this feature.

When the ICS1892 detects a reversed signal polarity on its Twisted-Pair Receive pins and the Auto Polarity-Inhibit bit is also logic zero, the ICS1892 (1) automatically corrects the data stream and (2) sets the Polarity Reversed bit (bit 18.14) to logic one, to indicate to the STA that this situation exists. Bit 18.14 is a latching high (LH) bit. (For more information on latching high and latching low bits, see Section 8.1.4.1, “Latching High Bits” and Section 8.1.4.2, “Latching Low Bits”.)

Note:

1. The Auto Polarity Correction Function is primarily a 10Base-T operation. However, it is part of the Twisted-Pair Receiver and is operational during the 100Base-TX auto-negotiation process.
2. For information on the 100Base-TX Auto Polarity Correction, see Section 7.4.7, “100Base-TX Operation: Auto Polarity Correction (FLP)”.

7.5.14 10Base-T Operation: Isolation Transformer

As per the ISO/IEC specification, the ICS1892 interfaces with a medium through an isolation transformer. Typically, for each magnetic module there are two isolation transformers: one for the ICS1892 Twisted-Pair Transmitter and the other for the ICS1892 Twisted-Pair Receiver. For both 10Base-T and 100Base-TX operations, these isolation transformers provide both physical isolation as well as the means for coupling a signal between the ICS1892 and the medium.

Note:

1. For information on magnetic modules, see Section 6.6, “Twisted-Pair Interface”.
2. For information on the 10Base-T Isolation Transformer operation, see Section 7.4.8, “100Base-TX Operation: Isolation Transformer”

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7.6 Functional Block: Management Interface

As part of the MII, the ISO/IEC 8802-3 standard specifies a two-wire serial management interface and protocol. This interface is used to exchange control, status, and configuration information between the Station Management entity (STA) and the physical layer device (PHY). For using this management interface, the ISO/IEC standard specifies the following:

- A set of registers (Section 7.6.1, “Management Register Set Summary”)
- The frame structure (Section 7.6.2, “Management Frame Structure”)
- The protocol

The ICS1892 implementation of the management interface complies fully with the ISO/IEC standard. It provides a bi-directional data pin (MDIO) along with a clock (MDC) for synchronizing the data transfers. These pins remain active in all MAC/Repeater Interface modes (that is, the 10/100 MII, 100M Symbol, 10M Serial, and Link Pulse interface modes).

7.6.1 Management Register Set Summary

The ICS1892 implements a Management Register set that adheres to the ISO/IEC standard. This register set (discussed in detail in Chapter 8, “Management Register Set”) includes the mandatory ‘Basic’ Control and Status registers as well as the ICS-specific Extended registers.

7.6.2 Management Frame Structure

The Management Interface is a bi-directional serial interface to exchange configuration, control, and status data between a PHY such as the ICS1892 and the STA. The PHY and STA exchange data by using the defined register set. The STA initiates all transactions.

The ISO/IEC specification defines a Management Frame Structure for the serial data stream. The ICS1892 complies with the defined frame structure and protocol. Table 7-2 summarizes the Management Frame Structure.

Note: The Management Frame Structure starts from and returns to an IDLE condition. However, the IDLE periods are not part of the Management Frame Structure.

Table 7-2. Management Frame Structure Summary

Frame Field		Data	Comment
Acronym	**Frame Function**		
PRE	Preamble (Bit 1.6)	11..11	32 ones
SFD	Start of Frame	01	2 bits
OP	Operation Code	10/01 (read/write)	2 bits
PHYAD	PHY Address (Bits 16.10:6)	AAAAA	5 bits
REGAD	Register Address	RRRRR	5 bits
TA	Turnaround	Z0/10 (read/write)	2 bits
DATA	Data	DDD..DD	16 bits

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7.6.2.1 Management Frame Preamble

The ICS1892 continually monitors its management interface for a Management Frame Preamble (PRE), which indicates the start of an STA transaction. A Management Frame Preamble is a pattern of 32 contiguous logic one bits on the MDIO pin, along with 32 corresponding cycles on the MDC pin.

The ICS1892 supports the Management Frame (MF) Preamble Suppression capability on its Management Interface, thereby providing a method to shorten the Management Frame and provide an STA with faster access to the Management Registers. The Management Frame Preamble Suppression bit (bit 1.6 in the Status Register) indicates whether the ICS1892 can support frames that do not have a preamble.

- The ICS 1890, unlike the ICS1892, does not support MF preamble suppression. Consequently, for the ICS 1890, bit 1.6 (a Read-Only status bit) is permanently set to logic zero.
- The ICS1892 does support MF preamble suppression. To maintain backward compatibility, the ICS1892 MF Suppression Bit defaults to logic zero after a reset. However, for the ICS1892, this bit is now a Command Override Write bit instead of a Read-Only bit, thereby providing the STA with the ability to enable this feature. For an explanation of the Command Override Write bits, see Section 8.1.2, “Management Register Bit Access”.

7.6.2.2 Management Frame Start

A valid Management Frame includes a start-of-frame delimiter, SFD, immediately following the preamble. The SFD bit pattern is 01b and is synchronous with two cycles on the MDC pin.

7.6.2.3 Management Frame Operation Code

A valid Management Frame includes an operation code (OP) immediately following the start-of-frame delimiter. There are two valid operation codes: one for reading from a management register 10b and one for writing to a management register 01b. The ICS1892 does not respond to the codes 00b and 11b, which are invalid.

7.6.2.4 Management Frame PHY Address

The ISO/IEC specification is such that a maximum of 32 PHYs can use one set of MDC and MDIO interface pins. An STA uniquely identifies each of the PHYs sharing a management interface by using the 5-bit PHY Address field, PHYAD. A valid Management Frame includes a PHYAD field.

Upon receiving a valid STA transaction, the ICS1892 compares the PHYAD included within the frame with the value of the PHYAD bits stored during a power-on or hardware reset. (For information on the PHYAD bits, see Table 8-16.) The operation code responds to all transactions that match the internally stored address bits. The first PHYAD bit transmitted and received is the most-significant bit.

7.6.2.5 Management Frame Register Address

A valid Management Frame includes a 5-bit register address, the REGAD field. This field identifies which of the 32 Management Registers are to be involved in the transaction. If the operation code is a:

- Read, the REGAD identifies the register used as the source of data returned to the STA by the ICS1892.
- Write, the REGAD identifies the destination register, which is to receive the data sent by the STA to the ICS1892.

If the STA attempts to:

- Read from a non-existent ICS1892 register, the ICS1892 returns logic zero for all bits in the Data field.
- Write to a non-existent ICS1892 register, the ICS1892 isolates the Data field. The first REGAD bit transmitted and received is the most-significant bit.

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7.6.2.6 Management Frame Turnaround

A valid Management Frame includes a turnaround field (TA), which is a 2-bit time space between the REGAD field and the Data field. This field requires two bit times and allows the ICS1892 and the STA to avoid contentions during read transactions. During an operation that is a:

- Read, the ICS1892 remains in the high-impedance state during the first bit time and subsequently drives the MDIO pin to logic zero for the second bit time.
- Write, the ICS1892 waits while the STA transmits a logic one, followed by a logic zero on the MDIO signal.

7.6.2.7 Management Frame Data

A valid Management Frame includes a 16-bit Data field for exchanging data between the Management Registers, and the STA. All Management Registers are 16 bits wide, matching the width of the Data field. The first Data bit transmitted and received is the most-significant bit of a Management Register, bit X.15. During a transaction that is a:

- Read, OP is 10b and the ICS1892 obtains the value of the register identified in the REGAD field and returns the Data to the STA synchronously with the MDC cycles.
- Write, OP is 01b and the ICS1892 stores the value of the Data field in the register identified in the REGAD field.

If the STA attempts to:

- Read from a non-existent ICS1892 register, the ICS1892 returns logic zero for all bits in the Data field.
- Write to a non-existent ICS1892 register, the ICS1892 isolates the Data field.

7.6.2.8 Idle

MDIO is idle during the time between STA transactions. During this idle time, the ICS1892 disables its tri-state drivers and the MDIO pin enters a high-impedance state. The ISO/IEC 8802-3 standard requires that the signal be idle for at least one bit time between management transactions. However, the ICS1892 does not have this limitation as it can support a continual bit stream on its MDIO.

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Chapter 8 Management Register Set

The tables in this chapter details the functionality of the bits in the management register set. The tables include the register locations, the bit positions, the bit definitions, the STA Read/Write Access Types, the default bit values, and any special bit functions or capabilities (such as self-clearing). Following each table is a description of each bit. This chapter includes the following sections:

- Section 8.1, “Introduction to Management Register Set”
- Section 8.2, “Register 0: Control Register”
- Section 8.3, “Register 1: Status Register”
- Section 8.4, “Register 2: PHY Identifier Register”
- Section 8.5, “Register 3: PHY Identifier Register”
- Section 8.6, “Register 4: Auto-Negotiation Register”
- Section 8.7, “Register 5: Auto-Negotiation Link Partner Ability Register”
- Section 8.8, “Register 6: Auto-Negotiation Expansion Register”
- Section 8.9, “Register 7: Auto-Negotiation Next Page Transmit Register”
- Section 8.10, “Register 8: Auto-Negotiation Next Page Link Partner Ability Register”
- Section 8.11, “Register 16: Extended Control Register”
- Section 8.12, “Register 17: Quick Poll Detailed Status Register”
- Section 8.13, “Register 18: 10Base-T Operations Register”
- Section 8.14, “Register 19: Extended Control Register 2”

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8.1 Introduction to Management Register Set

This section explains in general terms the Management Register set discussed in this chapter. (For a summary of the Management Register set, see Section 7.6.1, “Management Register Set Summary”.)

8.1.1 Management Register Set Outline

This section outlines the ICS1892 Management Register set. Table 8-1 lists the ISO/IEC-specified Management Register Set that the ICS1892 implements.

Table 8-1. ISO/IEC-Specified Management Register Set

Register Address	Register Name	Basic / Extended
0	Control	Basic
1	Status	Basic
2,3	PHY Identifier	Extended
4	Auto-Negotiation Advertisement	Extended
5	Auto-Negotiation Link Partner Ability	Extended
6	Auto-Negotiation Expansion	Extended
7	Auto-Negotiation Next Page Transmit	Extended
8	Auto-Negotiation Next Page Link Partner Ability	Extended
9 through 15	Reserved by IEEE	Extended
16 through 31	Vendor-Specific (ICS) Registers	Extended

Table 8-2 lists the ICS-specific registers that the ICS1892 implements. These registers enhance the performance of the ICS1892 and provide the Station Management entity (STA) with additional control and status capabilities.

Table 8-2. ICS-Specific Registers

Register Address	Register Name	Basic / Extended
16	Extended Control	Extended
17	QuickPoll Detailed Status	Extended
18	10Base-T Operations	Extended
19	Auto-Negotiation Advertisement	Extended
20 through 31	Reserved by ICS	Extended

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8.1.2 Management Register Bit Access

The ICS1892 Management Registers include one or more of the three following types of bits:

Table 8-3. Description of Management Register Bit Types

Management Register Bit Types	Bit Symbol	Description
Read-Only	RO	An STA can obtain the value of a RO register bit. However, it cannot alter the value of (that is, it cannot write to) an RO register bit. The ICS1892 isolates any STA attempt to write a value to an RO bit.
Command Override Write	CW	An STA can read a value from a CW register bit. However, write operations are conditional, based on the value of the Command Register Override bit (bit 16.15). When bit 16.15 is logic: • Zero (the default), the ICS1892 isolates STA attempts to write to the CW bits (that is, CW bits cannot be altered when bit 16.15 is logic zero). • One, the ICS1892 permits an STA to alter the value of the CW bits in the subsequent register write. (Bit 16.15 is self-clearing and automatically clears to zero on the subsequent write.)
Read/Write	R/W	An STA can unconditionally read from or write to a R/W register bit.
Read/Write Zero	R/W0	An STA can unconditionally read from a R/W0 register bit, but only a '0' value can be written to this bit.

8.1.3 Management Register Bit Default Values

The tables in this chapter specify for each register bit the default value, if one exists. The ICS1892 sets all Management Register bits to their default values after a reset. Table 8-4 lists the valid default values for ICS1892 management register bits.

Table 8-4. Range of Possible Valid Default Values for ICS1892 Register Bits

Default Condition	Default Value
–	Indicates there is no default value for the bit
0	Indicates the bit's default value is logic zero
1	Indicates the bit's default value is logic one
State of pin at reset	For some bits, the default value depends on the state of a particular pin at reset (that is, the state value of a pin is latched at reset.) An example of pins that have a default condition that depends on the state of the pin at reset are the PHY / LED pins (P0AC, P1CL, P2LI, P3TD, and P4RD) discussed in Section 6.9, "Status Interface", Section 8.11, "Register 16: Extended Control Register", and Section 9.2.2, "Multi-Function (Multiplexed) Pins: PHY Address and LED Pins"

Note: The ICS1892 has a number of reserved bits throughout the Management Registers. Most of these bits provide enhanced test modes. The Management Register tables provide the default values for these bits. The STA must not change the value of these bits under any circumstance. If the STA inadvertently changes the default values of these reserved register bits, normal operation of the ICS1892 can be affected.

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8.1.4 Management Register Bit Special Functions

The three types of special functions for the Management Register bits include the following:

8.1.4.1 Latching High Bits

The purpose of a latching high (LH) bit is to record an event. An LH bit records an event by monitoring an active-high signal and then latching this active-high signal when it triggers (that is, when the event occurs).

A latching high bit, once set to logic one, remains set until either a reset occurs or it is read by an STA. Immediately following an STA read of an LH bit, the ICS1892 latches the current state of the signal into the LH bit. When an STA reads an LH bit:

- Once, the LH bit provides the STA with a history of whether or not the event has occurred since the last read of that bit. That is, this first read provides the STA with a history of the condition and subsequently latches the current state of the signal into the LH bit for the next read.
- Twice in succession, the LH bit provides the STA with the current state of the monitored signal.

8.1.4.2 Latching Low Bits

As with latching high bits, the purpose of a latching low (LL) bit is also to record an event. An LL bit records an event by monitoring an active-low signal and then latching this active-low signal when it triggers (that is, when the event occurs).

A latching low bit, once cleared to logic zero, remains cleared until either a reset occurs or it is read by an STA. Immediately following an STA read of an LL bit, the ICS1892 latches the current state of the active-low signal into the LL bit. When an STA reads an LL bit:

- Once, the LL bit provides the STA with a history of whether or not the event has ever occurred. That is, this first read provides the STA with a history of the condition and latches the current state of the signal into the LL bit for the next read.
- Twice in succession, the LL bit provides the STA with the current state of the monitored signal.

8.1.4.3 Latching Maximum Bits

For the ICS1892, the purpose of latching maximum (LMX) bits is to track the progress of internal state machines. The LMX bits act in combination with other LMX bits to save the maximum collective value of a defined group of LMX bits, from the most-significant bit to the least-significant bit.

For example, assume a group of LMX bits is defined as register bits 13 through 11. If these bits first have a value of 3o (octal) and then the state machine they are monitoring advances to state:

- 2o, then the 2o value does not get latched.
- 4o (or any other value greater than 3o), then in this case, the value of 4o does get latched.

LMX bits retain their value until either a reset occurs or they are read by an STA. Immediately following an STA read of a defined group of LMX bits, the ICS1892 latches the current state of the monitored state machine into the LMX bits. When an STA reads a group of LMX bits:

- Once, the LMX bits provide the STA with a history of the maximum value that the state machine has achieved and latches the current state of the state machine into the LMX bits for the next read.
- Twice in succession, the LMX bits provide the STA with the current state of the monitored state machine.

8.1.4.4 Self-Clearing Bits

Self-clearing (SC) bits automatically clear themselves to logic zero after a pre-determined amount of time without any further STA access. The SC bits have a default value of logic zero and are triggers to begin execution of a function. When the STA writes a logic one to an SC bit, the ICS1892 begins executing the function assigned to that bit. After the ICS1892 completes executing the function, it clears the bit to indicate that the action is complete.

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8.2 Register 0: Control Register

Table 8-5 lists the bits for the Control Register, a 16-bit register used to establish the basic operating modes of the ICS1892.

- The Control Register is accessible through the MII Management Interface.
- Its operation is independent of the MAC/Repeater Interface configuration.
- It is fully compliant with the ISO/IEC Control Register definition.

Note: For an explanation of acronyms used in Table 8-5, see Chapter 1, "Abbreviations and Acronyms".

Table 8-5. Control Register (Register 0 [0x00]

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
0.15	Reset	No effect	ICS1892 enters Reset mode	R/W	SC	0	3
0.14	Loopback enable	Disable Loopback mode	Enable Loopback mode	R/W	–	0	
0.13	Data rate select	10 Mbps operation	100 Mbps operation	R/W	–	1	
0.12	Auto-Negotiation enable	Disable Auto-Negotiation	Enable Auto-Negotiation	R/W	–	1	
0.11	Low-power mode	Normal power mode	Low-power mode	R/W	–	0	0/4†
0.10	Isolate	No effect	Isolate ICS1892 from MII	R/W	–	0/1†	
0.9	Auto-Negotiation restart	No effect	Restart Auto-Negotiation	R/W	SC	0	
0.8	Duplex mode	Half-duplex operation	Full-duplex operation	R/W	–	0	
0.7	Collision test	No effect	Enable collision test	R/W	–	0	0
0.6	IEEE reserved	Always 0	N/A	RO	–	0‡	
0.5	IEEE reserved	Always 0	N/A	RO	–	0‡	
0.4	IEEE reserved	Always 0	N/A	RO	–	0‡	
0.3	IEEE reserved	Always 0	N/A	RO	–	0‡	0
0.2	IEEE reserved	Always 0	N/A	RO	–	0‡	
0.1	IEEE reserved	Always 0	N/A	RO	–	0‡	
0.0	IEEE reserved	Always 0	N/A	RO	–	0‡	

† Whenever the PHY address of Table 8-16:

- Is equal to 00000 (binary), the Isolate bit 0.10 is logic one.
- Is not equal to 00000, the Isolate bit 0.10 is logic zero.

‡ As per the IEEE Std 802.3u, during any write operation to any bit in this register, the STA must write the default value to all Reserved bits.

8.2.1 Reset (bit 0.15)

This bit controls the software reset function. Setting this bit to logic one initiates an ICS1892 software reset during which all Management Registers are set to their default values and all internal state machines are set to their idle state. For a detailed description of the software reset process, see Section 5.1.2.3, "Software Reset".

During reset, the ICS1892 leaves bit 0.15 set to logic one and isolates all STA management register accesses for 640 ns. However, the reset process is not complete until bit 0.15 (a Self-Clearing bit), is set to logic zero, which indicates the reset process is terminated.

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8.2.2 Loopback Enable (bit 0.14)

This bit controls the Loopback mode for the ICS1892. Setting this bit to logic:

- Zero disables the Loopback mode.
- One enables the Loopback mode by disabling the Twisted-Pair Transmitter, the Twisted-Pair Receiver, and the collision detection circuitry. (The STA can override the ICS1892 from disabling the collision detection circuitry in Loopback mode by writing logic one to bit 0.7.) When the ICS1892 is in Loopback mode, the data presented at the MAC/repeater transmit interface is internally looped back to the MAC/repeater receive interface. The delay from the assertion of Transmit Data Enable (TXEN) to the assertion of Receive Data valid (RXDV) is less than 512 bit times.

8.2.3 Data Rate Select (bit 0.13)

This bit provides a means of controlling the ICS1892 data rate. Its operation depends on the state of several other functions, including the HW/SW input pin and the Auto-Negotiation Enable bit (bit 0.12). When the ICS1892 is configured for:

- Hardware mode (that is, the HW/SW pin is logic zero), the ICS1892 isolates this bit 0.13 and uses the 10/100SEL input pin to establish the data rate for the ICS1892. In this Hardware mode:
  - Bit 0.13 is undefined.
  - The ICS1892 provides a Data Rate Status bit (in the QuickPoll Detailed Status Register, bit 17.15), which always shows the setting of an active link.
- Software mode (that is, the HW/SW pin is logic one), the function of bit 0.13 depends on the Auto-Negotiation Enable bit 0.12. When Auto-Negotiation is:
  - Enabled, the ICS1892 isolates bit 0.13 and relies on the results of the auto-negotiation process to establish the data rate.
  - Disabled, bit 0.13 determines the data rate. In this case, setting bit 0.13 to logic:
    - Zero selects 10-Mbps ICS1892 operations.
    - One selects 100-Mbps ICS1892 operations.

8.2.4 Auto-Negotiation Enable (bit 0.12)

This bit provides a means of controlling the ICS1892 Auto-Negotiation sublayer. Its operation depends on the HW/SW input pin.

When the ICS1892 is configured for:

- Hardware mode, (that is, the HW/SW pin is logic zero), the ICS1892 isolates bit 0.12 and uses the ANSEL (Auto-Negotiation Select) input pin to determine whether to enable the Auto-Negotiation sublayer.

  Note: In Hardware mode, bit 0.12 is undefined.
- Software mode, (that is, the HW/SW pin is logic one), bit 0.12 determines whether to enable the Auto-Negotiation sublayer. When bit 0.12 is logic:
  - Zero:
    - The ICS1892 disables the Auto-Negotiation sublayer.
    - The ICS1892 bit 0.13 (the Data Rate bit) and bit 0.8 (the Duplex Mode bit) determine the data rate and the duplex mode.
  - One:
    - The ICS1892 enables the Auto-Negotiation sublayer.
    - The ICS1892 isolates bit 0.13 and bit 0.8.

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8.2.5 Low Power Mode (bit 0.11)

This bit provides one way to control the ICS1892 low-power mode function. When bit 0.11 is logic:

- Zero, there is no impact to ICS1892 operations.
- One, the ICS1892 enters the low-power mode. In this case, the ICS1892 disables all internal functions and drives all MAC/repeater output pins low except for those that support the MII Serial Management Port.

Note: There are two ways the ICS1892 can enter low-power mode. When entering low-power mode:

- By setting bit 0.11 to logic one, the ICS1892 maintains the value of all management register bits except the latching high (LH) and latching low (LL) status bits, which are re-initialized to their default values instead. (For more information on latching high and latching low bits, see Section 8.1.4.1, “Latching High Bits” and Section 8.1.4.2, “Latching Low Bits”.)
- During a reset, the ICS1892 sets all management register bits to their default values.

8.2.6 Isolate (bit 0.10)

This bit controls the ICS1892 Isolate function. When bit 0.10 is logic:

- Zero, there is no impact to ICS1892 operations.
- One, the ICS1892 electrically isolates its data paths from the MAC/Repeater Interface. The ICS1892 places all MAC/repeater output signals, (TXCLK, RXCLK, RXDV, RXER, RXD[3:0], COL, and CRS), in a high-impedance state and it isolates all MAC/repeater input signals, (TXD[3:0], TXEN, and TXER). In this mode, the Management Interface continues to operate normally (that is, bit 0.10 does not affect the Management Interface).

The default value for bit 0.10 depends upon the PHY address of Table 8-16. If the PHY address:

- Is equal to 00000b, then the default value of bit 0.10 is logic one, and the ICS1892 isolates itself from the MAC/Repeater Interface.
- Is not equal to 00000b, then the default value of bit 0.10 is logic zero, and the ICS1892 does not isolate its MAC/Repeater Interface.

8.2.7 Restart Auto-Negotiation (bit 0.9)

This bit allows an STA to restart the auto-negotiation process in Software mode (that is, the HW/SW pin is logic one). When bit 0.12 is logic:

- Zero, the Auto-Negotiation sublayer is disabled, and the ICS1892 isolates any attempt by the STA to set bit 0.9 to logic one.
- One (as set by an STA), the ICS1892 restarts the auto-negotiation process. Once the auto-negotiation process begins, the ICS1892 automatically sets this bit to logic zero, thereby providing the self-clearing feature.

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8.2.8 Duplex Mode (bit 0.8)

This bit provides a means of controlling the ICS1892 Duplex Mode. Its operation depends on several other functions, including the HW/SW input pin and the Auto-Negotiation Enable bit (bit 0.12). When the ICS1892 is configured for:

- Hardware mode (that is, the HW/SW pin is logic zero), the ICS1892 isolates bit 0.8 and uses the DPXSEL input pin to establish the Duplex mode for the ICS1892. In this Hardware mode:
  - Bit 0.8 is undefined.
  - The ICS1892 provides a Duplex Mode Status bit (in the QuickPoll Detailed Status Register, bit 17.14), which always shows the setting of an active link.
- Software mode (that is, the HW/SW pin is logic one), the function of bit 0.8 depends on the Auto-Negotiation Enable bit, 0.12. When the auto-negotiation process is:
  - Enabled, the ICS1892 isolates bit 0.8 and relies upon the results of the auto-negotiation process to establish the duplex mode.
  - Disabled, bit 0.8 determines the Duplex mode. Setting bit 0.8 to logic:
    - Zero selects half-duplex operations.
    - One selects full-duplex operations. (When the ICS1892 is operating in Loopback mode, it isolates bit 0.8, which has no effect on the operation of the ICS1892.)

8.2.9 Collision Test (bit 0.7)

This bit controls the ICS1892 Collision Test function. When an STA sets bit 0.7 to logic:

- Zero, the ICS1892 disables the collision detection circuitry for the Collision Test function. In this case, the COL signal does not track the TXEN signal. (The default value for this bit is logic zero, that is, disabled.)
- One, as per the ISO/IEE 8802-3 standard, clause 22.2.4.1.9, the ICS1892 enables the collision detection circuitry for the Collision Test function, even if the ICS1892 is in Loopback mode (that is, bit 0.14 is set to 1). In this case, the Collision Test function tracks the Collision Detect signal (COL) in response to the TXEN signal. The ICS1892 asserts the Collision signal (COL) within 512 bit times of receiving an asserted TXEN signal, and it de-asserts COL within 4 bit times of the de-assertion of the TXEN signal.

8.2.10 IEEE Reserved Bits (bits 0.6:0)

The IEEE reserves these bits for future use. When an STA:

- Reads a reserved bit, the ICS1892 returns a logic zero.
- Writes to a reserved bit, it must use the default value specified in this data sheet.

The ICS1892 uses some of these reserved bits to invoke auxiliary functions. To ensure proper operation of the ICS1892, an STA must maintain the default value of these bits. Therefore, ICS recommends that during any STA write operation, an STA write the default value to all reserved bits, even those bits that are Read Only.

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8.3 Register 1: Status Register

Table 8-6 lists the bits for the Status Register, an interface between the ICS1892 and the STA that has 16 bits of data. There are two types of status bits: some report the capabilities of the ICS1892, and some indicate the state of signals used to monitor internal circuits.

The STA accesses the Status Register using the Serial Management Interface. During a reset, the ICS1892 initializes the Status Register bits to pre-defined, default values.

Note: For an explanation of acronyms used in Table 8-5, see Chapter 1, "Abbreviations and Acronyms".

Table 8-6. Status Register (Register 1 [0x01])

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
1.15	100Base-T4	Always 0. (Not supported.)	N/A	RO	–	0	7
1.14	100Base-TX full duplex	Mode not supported	Mode supported	CW	–	1	
1.13	100Base-TX half duplex	Mode not supported	Mode supported	CW	–	1	
1.12	10Base-T full duplex	Mode not supported	Mode supported	CW	–	1	
1.11	10Base-T half duplex	Mode not supported	Mode supported	CW	–	1	8
1.10	IEEE reserved	Always 0	N/A	CW	–	0†	
1.9	IEEE reserved	Always 0	N/A	CW	–	0†	
1.8	IEEE reserved	Always 0	N/A	CW	–	0†	
1.7	IEEE reserved	Always 0	N/A	CW	–	0†	0
1.6	MF Preamble suppression	PHY requires MF Preambles	PHY does not require MF Preambles	RO	–	0	
1.5	Auto-Negotiation complete	Auto-Negotiation is in process, if enabled	Auto-Negotiation is completed	RO	LH	0	
1.4	Remote fault	No remote Fault Detected	Remote fault detected	RO	LH	0	
1.3	Auto-Negotiation ability	N/A	Always 1: PHY has Auto-Negotiation ability	RO	–	1	9
1.2	Link status	Link is invalid/down	Link is valid/established	RO	LL	0	
1.1	Jabber detect	No jabber condition	Jabber condition detected	RO	LH	0	
1.0	Extended capability	N/A	Always 1: PHY has extended capabilities	RO	–	1	

† As per the IEEE Std 802.3u, during any write operation to any bit in this register, the STA must write the default value to all Reserved bits.

8.3.1 100Base-T4 (bit 1.15)

The STA reads this bit to learn if the ICS1892 can support 100Base-T4 operations. Bit 1.15 of the ICS1892 is permanently set to logic zero, which informs an STA that the ICS1892 cannot support 100Base-T4 operations.

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8.3.2 100Base-TX Full Duplex (bit 1.14)

The STA reads this bit to learn if the ICS1892 can support 100Base-TX, Full Duplex operations. The ISO/IEC specification requires that the ICS1892 must set bit 1.14 to logic:

- Zero if it cannot support 100Base-TX, full-duplex operations.
- One if it can support 100Base-TX, full-duplex operations. (For the ICS1892, the default value of bit 1.14 is logic one. Therefore, when an STA reads the Status Register, the STA is informed that the ICS1892 supports 100Base-TX, full-duplex operations.)

This bit 1.14 is a Command Override Write bit, which allows an STA to alter the default value of this bit. [See the description of bit 16.15, the Command Override Write Enable bit, in Section 8.11, “Register 16: Extended Control Register”.]

8.3.3 100Base-TX Half Duplex (bit 1.13)

The STA reads this bit to learn if the ICS1892 can support 100Base-TX, half-duplex operations. The ISO/IEC specification requires that the ICS1892 must set bit 1.13 to logic:

- Zero if it cannot support 100Base-TX, half-duplex operations.
- One if it can support 100Base-TX, half-duplex operations. (For the ICS1892, the default value of bit 1.13 is logic one. Therefore, when an STA reads the Status Register, the STA is informed that the ICS1892 supports 100Base-TX, half-duplex operations.)

This bit 1.13 is a Command Override Write bit, which allows an STA to alter the default value of this bit. [See the description of bit 16.15, the Command Override Write Enable bit, in Section 8.11, “Register 16: Extended Control Register”.]

8.3.4 10Base-T Full Duplex (bit 1.12)

The STA reads this bit to learn if the ICS1892 can support 10Base-T, full-duplex operations. The ISO/IEC specification requires that the ICS1892 must set bit 1.12 to logic:

- Zero if it cannot support 10Base-T, full-duplex operations.
- One if it can support 10Base-T, full-duplex operations. (For the ICS1892, the default value of bit 1.12 is logic one. Therefore, when an STA reads the Status Register, the STA is informed that the ICS1892 supports 10Base-T, full-duplex operations.)

This bit 1.12 is a Command Override Write bit, which allows an STA to alter the default value of this bit. [See the description of bit 16.15, the Command Override Write Enable bit, in Section 8.11, “Register 16: Extended Control Register”.]

8.3.5 10Base-T Half Duplex (bit 1.11)

The STA reads this bit to learn if the ICS1892 can support 10Base-T, half-duplex operations. The ISO/IEC specification requires that the ICS1892 must set bit 1.11 to logic:

- Zero if it cannot support 10Base-T, half-duplex operations.
- One if it can support 10Base-T, half-duplex operations. (For the ICS1892, the default value of bit 1.11 is logic one. Therefore, when an STA reads the Status Register, the STA is informed that the ICS1892 supports 10Base-T, half-duplex operations.)

Bit 1.11 of the ICS1892 Status Register is a Command Override Write bit., which allows an STA to alter the default value of this bit. [See the description of bit 16.15, the Command Override Write Enable bit, in Section 8.11, “Register 16: Extended Control Register”.]

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8.3.6 IEEE Reserved Bits (bits 1.10:7)

The IEEE reserves these bits for future use. When an STA:

- Reads a reserved bit, the ICS1892 returns a logic zero.
- Writes a reserved bit, the STA must use the default value specified in this data sheet.

Both the ISO/IEC standard and the ICS1892 reserve the use of some Management Register bits. ICS uses some of these reserved bits to invoke ICS1892 test functions. To ensure proper operation of the ICS1892, an STA must maintain the default value of these bits. Therefore, ICS recommends that an STA write the default value to all reserved bits during all Management Register write operations.

Reserved bits 1.10:7 are Command Override Write (CW) bits. When bit 16.15, the Command Register Override bit is logic:

- Zero, the ICS1892 isolates all STA writes to CW bits.
- One, an STA can modify the value of these bits.

8.3.7 MF Preamble Suppression (bit 1.6)

Status Register bit 1.6 is the Management Frame (MF) Preamble Suppression bit. The ICS1892 sets bit 1.6 to inform the STA of its ability to receive frames that do not have a preamble. When this bit is logic:

- Zero, the ICS1892 is indicating it cannot accept frames with a suppressed preamble.
- One, the ICS1892 is indicating it can accept frames that do not have a preamble.

Although the ICS1892 supports Management Frame Preamble Suppression, its default value for bit 1.6 is logic zero. This default value ensures that bit 1.6 is backward compatible with the ICS 1890, which does not have this capability. As the means of enabling this feature, bit 1.6 of the ICS1892 is a Command Override Write bit, instead of a Read-Only bit as in the ICS 1890. An STA uses the bit 1.6 to enable MF Preamble Suppression in the ICS1892. [See the description of bit 16.15, the Command Override Write Enable bit, in Section 8.11, “Register 16: Extended Control Register”.]

8.3.8 Auto-Negotiation Complete (bit 1.5)

An STA reads bit 1.5 to determine the state of the ICS1892 auto-negotiation process. The ICS1892 sets the value of this bit using two criteria. When its Auto-Negotiation sublayer is:

- Disabled, the ICS1892 sets bit 1.5 to logic zero.
- Enabled, the ICS1892 sets bit 1.5 to a value based on the state of the Auto-Negotiation State Machine. When the Auto-Negotiation State Machine is enabled, it sets bit 1.5 to logic one only upon completion of the auto-negotiation process. This setting indicates to the STA that a link is arbitrated and the contents of Management Registers 4, 5 and 6 are valid. For more detailed information regarding the auto-negotiation process, see Section 7.2, “Functional Block: Auto-Negotiation”.

Bit 1.5 is a latching high (LH) bit. (For more information on latching high and latching low bits, see Section 8.1.4.1, “Latching High Bits” and Section 8.1.4.2, “Latching Low Bits”.)

Note: An Auto-Negotiation Restart does not clear an LH bit.

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8.3.9 Remote Fault (bit 1.4)

The STA reads bit 1.4 to determine if a Remote Fault exists. The ICS1892 sets bit 1.4 based on the Remote Fault bit received from its remote link partner. The ICS1892 receives the Remote Fault bit as part of the Link Code Word exchanged during the auto-negotiation process. If the remote link partner:

- Sets the Link Code Word Remote Fault bit to logic one, then the ICS1892 sets bit 1.4 to logic one. In this case, the remote link partner reports the detection of a fault, which typically occurs when the remote link partner is having a problem with its receive channel.
- Clears the Link Code Word Remote Fault bit to logic zero, then the ICS1892 sets bit 1.4 to logic zero.

Bit 1.4 is a latching high status bit. (For more information on latching high and latching low bits, see Section 8.1.4.1, “Latching High Bits” and Section 8.1.4.2, “Latching Low Bits”.)

Note: The STA can access the Remote Fault bit through Management Registers 1 (bit 1.4), 5 (bit 5.13), and 17 (bit 17.1). The Remote Fault bit is cleared when an STA reads any one of these bits.

8.3.10 Auto-Negotiation Ability (bit 1.3)

The STA reads bit 1.3 to determine if the ICS1892 can support the auto-negotiation process. If the ICS1892:

- Cannot support the auto-negotiation process, it clears bit 1.3 to logic zero.
- Can support the auto-negotiation process, it sets bit 1.3 to logic one. (For the ICS1892, the default value of bit 1.3 is logic one.)

8.3.11 Link Status (bit 1.2)

The purpose of this Link Status bit (as well as the QuickPoll Register’s Link Status bit, bit 17.0) is to determine if an established link is dropped, even momentarily. An STA reads bit 1.2 to determine the state of the link between the ICS1892 and its remote partner. To indicate a link that is:

- Valid, the ICS1892 sets bit 1.2 to logic one.
- Invalid, the ICS1892 clears bit 1.2 to logic zero.

This bit is a latching low (LL) bit that the Link Monitor function controls. (For more information on latching high and latching low bits, see Section 8.1.4.1, “Latching High Bits” and Section 8.1.4.2, “Latching Low Bits”.) The criterion used by the Link Monitor to determine if a link is valid or invalid depends on the following:

- Type of link
- Present link state (valid or invalid)
- Presence of any link errors
- Auto-negotiation process

The Link Monitor function observes the data received by either 10Base-T or 100Base-TX Twisted-Pair Receivers to determine the link status. The results of this continual monitoring are stored in the Link Status bit. An STA can access the Link Status bit in either the Status Register (bit 1.2) or the QuickPoll Detailed Status Register (bit 17.0).

If Auto-Negotiation mode is enabled, a local receive channel error occurs if link pulses are not present during the auto-negotiation process or when operating in the 10Base-T mode.

Note: The Link Status bit is accessible through two Management Registers and is set high when an STA reads either one of them.

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8.3.12 Jabber Detect (bit 1.1)

The purpose of this bit is to allow an STA to read this bit to determine if the ICS1892 detects a Jabber condition.

The ISO/IEC specification defines the requirements for detection of a Jabber condition.To detect a Jabber condition, the ICS1892 must first enable its Jabber Detection function, which is controlled by the Jabber Inhibit bit in the 10Base-T Operations register (bit 18.5). When bit 18.5 is logic:

- Zero, the ICS1892 disables Jabber Detection
- One, the ICS1892 enables Jabber Detection. In this case, when the ICS1892 detects a Jabber condition, it does the following:
  - It sets bit 1.2 to logic one.
  - It sets the Jabber Detect bit (bit 1.1 in the Status Register, and mirrored as bit 17.2 in the QuickPoll Detailed Status Register) to logic one.

Bit 1.1 is a latching high (LH) bit. (For more information on latching high and latching low bits, see Section 8.1.4.1, “Latching High Bits” and Section 8.1.4.2, “Latching Low Bits”.)

8.3.13 Extended Capability (bit 1.0)

The STA reads bit 1.0 to determine if the ICS1892 has an extended register set. In the ICS1892 this bit is always logic one, indicating that it has extended registers.

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8.4 Register 2: PHY Identifier Register

Table 8-7 lists the bits for PHY Identifier Register (Register 2), which is one of two PHY Identifier Registers that are part of a set defined by the ISO/IEC specification. As a set, the PHY Identifier Registers (Registers 2 and 3) include a unique, 32-bit PHY Identifier composed from the following:

- Organizationally Unique Identifier (OUI), discussed in this section
- Manufacturer's PHY Model Number, discussed in Section 8.5, "Register 3: PHY Identifier Register"
- Manufacturer's PHY Revision Number, discussed in Section 8.5, "Register 3: PHY Identifier Register"

All of the bits in the two PHY Identifier Registers are Command Override Write bits. An STA can read them at any time without condition. However, an STA can modify these register bits only when the Command Register Override bit (bit 16.15) is enabled with a logic one.

Note: For an explanation of acronyms used in Table 8-5, see Chapter 1, "Abbreviations and Acronyms".

Table 8-7. PHY Identifier Register (Register 2 [0x02])

Bit	Definition	When Bit = 0	When Bit = 1	Access	Special Function	Default	Hex
2.15	OUI bit 3 | c	N/A	N/A	CW	–	0	0
2.14	OUI bit 4 | d	N/A	N/A	CW	–	0	
2.13	OUI bit 5 | e	N/A	N/A	CW	–	0	
2.12	OUI bit 6 | f	N/A	N/A	CW	–	0	
2.11	OUI bit 7 | g	N/A	N/A	CW	–	0	0
2.10	OUI bit 8 | h	N/A	N/A	CW	–	0	
2.9	OUI bit 9 | I	N/A	N/A	CW	–	0	
2.8	OUI bit 10 | j	N/A	N/A	CW	–	0	
2.7	OUI bit 11 | k	N/A	N/A	CW	–	0	1
2.6	OUI bit 12 | l	N/A	N/A	CW	–	0	
2.5	OUI bit 13 | m	N/A	N/A	CW	–	0	
2.4	OUI bit 14 | n	N/A	N/A	CW	–	1	
2.3	OUI bit 15 | o	N/A	N/A	CW	–	0	5
2.2	OUI bit 16 | p	N/A	N/A	CW	–	1	
2.1	OUI bit 17 | q	N/A	N/A	CW	–	0	
2.0	OUI bit 18 | r	N/A	N/A	CW	–	1	

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IEEE-Assigned Organizationally Unique Identifier (OUI)

For each manufacturing organization, the IEEE assigns an 3-octet OUI. For Integrated Circuit Systems, Inc. the IEEE-assigned 3-octet OUI is 00A0BEh.

The binary representation of an OUI is formed by expressing each octet as a sequence of eight bits, from least significant to most significant, and from left to right. Table 8-8 provides the ISO/IEC-defined mapping of the OUI (in IEEE Std 802-1990 format) to Management Registers 2 and 3.

Table 8-8. IEEE-Assigned Organizationally Unique Identifier

First Octet								**Second Octet**								**Third Octet**							
0				0				0				A				E				B			
a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	t	u	v	w	x
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	1	1	1	0	1

0		0		1		5		F		1	
2.15:12		2.11:8		2.7:4		2.3:0		3.15:12		3.11:10	
Register 2								Register 3			

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8.5 Register 3: PHY Identifier Register

Table 8-9 lists the bits for PHY Identifier Register (Register 3), which is one of two PHY Identifier Registers that are part of a set defined by the ISO/IEC specification. This register stores the following:

- Part of the OUI [see the text in Section 8.4, "Register 2: PHY Identifier Register"]
- Manufacturer's PHY Model Number
- Manufacturer's PHY Revision Number

All of the bits in the two PHY Identifier Registers are Command Override Write bits. An STA can read them at any time without condition. However, An STA can modify these register bits only when the Command Register Override bit (bit 16.15) is enabled with a logic one.

Note: For an explanation of acronyms used in Table 8-5, see Chapter 1, "Abbreviations and Acronyms".

Table 8-9. PHY Identifier Register (Register 3 [0x03])

Bit	Definition	When Bit = 0	When Bit = 1	Access	Special Function	Default	Hex
3.15	OUI bit 19 ⏐ s	N/A	N/A	CW	–	1	F
3.14	OUI bit 20 ⏐ t	N/A	N/A	CW	–	1	
3.13	OUI bit 21 ⏐ u	N/A	N/A	CW	–	1	
3.12	OUI bit 22 ⏐ v	N/A	N/A	CW	–	1	
3.11	OUI bit 23 ⏐ w	N/A	N/A	CW	–	0	4
3.10	OUI bit 24 ⏐ x	N/A	N/A	CW	–	1	
3.9	Manufacturer's Model Number bit 5	N/A	N/A	CW	–	0	
3.8	Manufacturer's Model Number bit 4	N/A	N/A	CW	–	0	
3.7	Manufacturer's Model Number bit 3	N/A	N/A	CW	–	0	3
3.6	Manufacturer's Model Number bit 2	N/A	N/A	CW	–	0	
3.5	Manufacturer's Model Number bit 1	N/A	N/A	CW	–	1	
3.4	Manufacturer's Model Number bit 0	N/A	N/A	CW	–	1	
3.3	Revision Number bit 3	N/A	N/A	CW	–	0	0
3.2	Revision Number bit 2	N/A	N/A	CW	–	0	
3.1	Revision Number bit 1	N/A	N/A	CW	–	0	
3.0	Revision Number bit 0	N/A	N/A	CW	–	0	

8.5.1 OUI bits 19-24 (bits 3.15:10)

The most significant 6 bits of register 3 (that is, bits 3.15:10) include OUI bits 19 through 24. OUI bit 19 is stored in bit 3.15, while OUI bit 24 is stored in bit 3.10.

8.5.2 Manufacturer's Model Number (bits 3.9:4)

The model number for the ICS1892 is 3 (decimal). It is stored in bit 3.9:4 as 00011b.

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8.5.3 Revision Number (bits 3.3:0)

Table 8-10 lists the valid ICS1892 revision numbers, which are 4-bit binary numbers stored in bits 3.3:0.

Table 8-10. ICS1892 Revision Number

Decimal	Bits 3.3:0	Description
0	0000	ICS First Release

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8.6 Register 4: Auto-Negotiation Register

Table 8-11 lists the bits for the Auto-Negotiation Register. An STA uses this register to select the ICS1892 capabilities that it wants to advertise to its remote link partner. During the auto-negotiation process, the ICS1892 advertises (that is, exchanges) capability data with its remote link partner by using a pre-defined Link Code Word. The Link Code Word is embedded in the Fast Link Pulses exchanged between PHYs, when the ICS1892 has its Auto-Negotiation sublayer enabled. The value of the Link Control Word is established based on the value of the bits in this register.

Note: For an explanation of acronyms used in Table 8-5, see Chapter 1, "Abbreviations and Acronyms".

Table 8-11. Auto-Negotiation Advertisement Register (register 4 [0x04])

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
4.15	Next Page	Next page not supported	Next page supported	R/W	–	0	0
4.14	IEEE reserved	Always 0	N/A	CW	–	0†	
4.13	Remote fault	Locally, no faults detected	Local fault detected	R/W	–	0	
4.12	IEEE reserved	Always 0	N/A	CW	–	0†	
4.11	IEEE reserved	Always 0	N/A	CW	–	0†	1
4.10	IEEE reserved	Always 0	N/A	CW	–	0†	
4.9	100Base-T4	Always 0. (Not supported.)	N/A	CW	–	0	
4.8	100Base-TX, full duplex	Do not advertise ability	Advertise ability	Note 1	–	1	
4.7	100Base-TX, half duplex	Do not advertise ability	Advertise ability	Note 1	–	1	E
4.6	10Base-T, full duplex	Do not advertise ability	Advertise ability	Note 1	–	1	
4.5	10Base-T half duplex	Do not advertise ability	Advertise ability	Note 1	–	1	
4.4	Selector Field bit S4	IEEE 802.3-specified default	N/A	CW	–	0	
4.3	Selector Field bit S3	IEEE 802.3-specified default	N/A	CW	–	0	1
4.2	Selector Field bit S2	IEEE 802.3-specified default	N/A	CW	–	0	
4.1	Selector Field bit S1	IEEE 802.3-specified default	N/A	CW	–	0	
4.0	Selector Field bit S0	N/A	IEEE 802.3-specified default	CW	–	1	

† As per the IEEE Std 802.3u, during any write operation to any bit in this register, the STA must write the default value to all Reserved bits.

Note 1:

- In Hardware mode (that is, HW/SW pin is logic zero), this bit is a Read-Only bit.
- In Software mode (that is, HW/SW pin is logic one), this bit is a Command Override Write bit.

8.6.1 Next Page (bit 4.15)

This bit indicates whether the ICS1892 uses the Next Page Mode functions during the auto-negotiation process. If bit 4.15 is logic:

- Zero, then the ICS1892 indicates to its remote link partner that these features are disabled. (Although the default value of this bit is logic zero, the ICS1892 does support the Next Page function.)
- One, then the ICS1892 advertises to its remote link partner that this feature is enabled.

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8.6.2 IEEE Reserved Bit (bit 4.14)

The ISO/IEC specification reserves this bit for future use. However, the ISO/IEC Standard also defines bit 4.14 as the Acknowledge bit.

When this reserved bit is read by an STA, the ICS1892 returns a logic zero. However, whenever an STA writes to this reserved bit, it must use the default value specified in this data sheet. ICS uses some of these reserved bits to invoke auxiliary functions. To ensure proper operation of the ICS1892, an STA must maintain the default value of these bits. Therefore, ICS recommends that an STA always write the default value of any reserved bits during all management register write operations.

Reserved bit 4.14 is a Command Override Write (CW) bit. Whenever bit 16.15 (the Command Register Override bit) is logic:

- Zero, the ICS1892 isolates all STA writes to bit 4.14.
- One, an STA can modify the value of bit 4.14.

8.6.3 Remote Fault (bit 4.13)

When the ICS1892 Auto-Negotiation sublayer is enabled, the ICS1892 transmits the Remote Fault bit 4.13 to its remote link partner during the auto-negotiation process. The Remote Fault bit is part of the Link Code Word that the ICS1892 exchanges with its remote link partner. The ICS1892 sets this bit to logic one whenever it detects a problem with the link, locally. This data is sent to the remote link partner to inform it of the potential problem. If the ICS1892 does not detect a link fault, it clears bit 4.13 to logic zero.

Whenever the ICS1892:

- Does not detect a link fault, the ICS1892 clears bit 4.13 to logic zero.
- Detects a problem with the link, during the auto-negotiation process, this bit is set. As a result, the data on this bit is sent to the remote link partner to inform it of the potential problem.

8.6.4 Technology Ability Field (bits 4.12:5)

When its Auto-Negotiation sublayer is enabled, the ICS1892 transmits its link capabilities to its remote link partner during the auto-negotiation process. The Technology Ability Field (TAF) bits 4.12:5 determine the specific abilities that the ICS1892 advertises. The ISO/IEC specification defines the TAF technologies in Annex 28B.

The ISO/IEC specification reserves bits 4.12:10 for future use. When each of these reserved bits is:

- Read by an STA, the ICS1892 returns a logic zero
- Written to by an STA, the STA must use the default value specified in this data sheet.

ICS uses some of these reserved bits to invoke auxiliary functions. To ensure proper operation of the ICS1892, an STA must maintain the default value of these bits. Therefore, ICS recommends that an STA always write the default value of any reserved bits during all management register write operations.

Reserved bits 4.12:10 are Command Override Write (CW) bits. Whenever bit 16.15 (the Command Register Override bit) is logic: See para 8.1.2

- Zero, the ICS1892 isolates all STA writes to CW bits, including bits 4.12:10.
- One, an STA can modify the value of bits 4.12:10

Each of the bits 4.9:5 in the TAF represent a specific technology capability. When one of these bits is logic:

- Zero, it indicates to the remote link partner that the local device cannot support the technology represented by the bit.
- One, it indicates to the remote link partner that the local device can support the technology.

With the exception of bit 4.9, the default settings of the TAF bits depend on the ICS1892 operating mode. Bit 4.9 is always logic zero, indicating that the ICS1892 cannot support 100Base-T4 operations.

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8.6.4.1 Technology Ability Field: Hardware Mode

When the ICS1892 is operating in Hardware mode (that is, the HW/SW pin is logic zero), these TAF bits are Read Only bits. The default value of these bits depends on the signal level on the HW/SW pin and whether the Auto-Negotiation sublayer is enabled.

In Hardware mode, with the ANSEL pin pulled:

- Low to a disabled state, the ICS1892 does not execute the auto-negotiation process. Upon completion of the initialization sequence, the port proceeds to the idle state and begins 'sending idles' according to the technology mode selected by the 10/100SEL pin and the DPXSEL pin. In this mode, the value of the TAF bits (bits 4.8:5) are undefined.
- High to an enabled state, the ICS1892 executes the auto-negotiation process and advertises its capabilities to the remote link partner. The 10/100SEL and DPXSEL input pins determine the single capability that the ICS1892 advertises. The ICS1892 updates the Auto-Negotiation Advertisement Register TAF field to indicate the pin selection. The ICS1892 sets only one of these four bits to logic one. The other three are a logic zero.

Note: The ICS1892 does not alter the value of the Status Register bits. Although the ICS1892 is advertising only one technology, the ISO/IEC definitions for the Status Register bits require these bits to indicate all the capabilities of the ICS1892.

8.6.4.2 Technology Ability Field: Software Mode

In Software mode (that is, the HW/SW pin is logic one), these TAF bits are Command Override Write bits. The default value of these bits depends on the signal level on the HW/SW pin and whether the Auto-Negotiation sublayer is enabled.

In Software mode, with the Auto-Negotiation Enable bit (bit 0.12) set to logic:

- Zero (that is, disabled), the ICS1892 does not execute the auto-negotiation process. Upon completion of the initialization sequence, the port proceeds to the idle state and begins transmitting idles. Two Control Register bits – the Data Rate Select bit (bit 0.13), and the Duplex Select bit (bit 0.8) – determine the technology mode that the ICS1892 uses for data transmission and reception. In this mode, the values of the TAF bits (bits 4.8:5), are undefined.
- One (that is, enabled), the ICS1892 executes the auto-negotiation process and advertises its capabilities to the remote link partner. The TAF bits (bits 4.8:5), determine the capabilities that the ICS1892 advertises to its remote link partner. For the ICS1892, all of these bits 4.8:5 are set to logic one, indicating the ability of the ICS1892 to provide these technologies.

Note:

1. The ICS1892 does not alter the value of the Status Register bits based on the TAF bits in register 4, as the ISO/IEC definitions for the Status Register bits require these bits to indicate all the capabilities of the ICS1892.
2. In this mode, an STA can alter the default TAF bit settings, 4.12:5, and subsequently issue an Auto-Negotiation Restart.

8.6.5 Selector Field (Bits 4.4:0)

When its Auto-Negotiation Sublayer is enabled, the ICS1892 transmits its link capabilities to its remote Link Partner during the auto-negotiation process. The Selector Field is transmitted based on the value of bits 4.4:0. These bits indicate to the remote link partner the type of message being sent during the auto-negotiation process. The ICS1892 supports IEEE Std 802.3, represented by a value of 00001b in bits 4.4:0. The ISO/IEC 8802-3 standard defines the Selector Field technologies in Annex 28A.

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8.7 Register 5: Auto-Negotiation Link Partner Ability Register

Table 8-12 lists the bits for the Auto-Negotiation Link Partner Ability Register. An STA uses this register to determine the capabilities being advertised by the remote link partner. During the auto-negotiation process, the ICS1892 advertises (that is, exchanges) the capability data with its remote link partner using a pre-defined Link Code Word. The value of the Link Control Word received from its remote link partner establishes the value of the bits in this register.

Note:

1. For an explanation of acronyms used in Table 8-12, see Chapter 1, "Abbreviations and Acronyms".
2. The values in this register are valid only when the auto-negotiation process is complete, as indicated by bit 1.5 or bit 17.4.

Table 8-12. Auto-Negotiation Link Partner Ability Register (register 5 [0x05])

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
5.15	Next Page	Next Page disabled	Next Page enabled	RO	–	0	0
5.14	Acknowledge	Always 0	N/A	RO	–	0	
5.13	Remote fault	No faults detected	Remote fault detected	RO	–	0	
5.12	IEEE reserved	Always 0	N/A	RO	–	0†	
5.11	IEEE reserved	Always 0	N/A	RO	–	0†	0
5.10	IEEE reserved	Always 0	N/A	RO	–	0†	
5.9	100Base-T4	Always 0. (Not supported.)	N/A	RO	–	0	
5.8	100Base-TX, full duplex	Link partner is not capable	Link partner is capable	RO	–	0	
5.7	100Base-TX, half duplex	Link partner is not capable	Link partner is capable	RO	–	0	0
5.6	10Base-T, full duplex	Link partner is not capable	Link partner is capable	RO	–	0	
5.5	10Base-T, half duplex	Link partner is not capable	Link partner is capable	RO	–	0	
5.4	Selector Field bit S4	IEEE 802.3 defined. Always 0.	N/A	RO	–	0	
5.3	Selector Field bit S3	IEEE 802.3 defined. Always 0.	N/A	CW	–	0	0
5.2	Selector Field bit S2	IEEE 802.3 defined. Always 0.	N/A	CW	–	0	
5.1	Selector Field bit S1	IEEE 802.3 defined. Always 0.	N/A	CW	–	0	
5.0	Selector Field bit S0	N/A	IEEE 802.3 defined. Always 1.	CW	–	0	

† As per the IEEE Std 802.3u, during any write operation to any bit in this register, the STA must write the default value to all Reserved bits.

8.7.1 Next Page (bit 5.15)

If bit 5.15 is logic:

- Zero, then the remote link partner is indicating that this is the last page being transmitted.
- One, then the remote link partner is indicating that additional pages follow.

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8.7.2 Acknowledge (bit 5.14)

The ISO/IEC specification defines bit 5.14 as the Acknowledge bit. When this bit is a:

- Zero, it indicates that the remote link partner has not received the ICS1892 Link Control Word.
- One, it indicates to the ICS1892 / STA that the remote link partner has acknowledged reception of the ICS1892 Link Control Word.

8.7.3 Remote Fault (bit 5.13)

The ISO/IEC specification defines bit 5.13 as the Remote Fault bit. This bit is set based on the Link Control Word received from the remote link partner. When this bit is a logic:

- Zero, it indicates that the remote link partner does not have a Link Fault.
- One, it indicates to the ICS1892 / STA that the remote link partner detects a Link Fault.

8.7.4 Technology Ability Field (bits 5.12:5)

The Technology Ability Field (TAF) bits (bits 5.12:5), determine the specific abilities that the remote link partner is advertising. These bits are set based upon the Link Code Word received from the remote link partner during the auto-negotiation process. The ISO/IEC specification defines the TAF technologies in Annex 28B.

The ISO/IEC specification reserves bits 5.12:10 for future use. When each of these reserved bits is:

- Read by an STA, the ICS1892 returns a logic zero.
- Written to by an STA, the STA must use the default value specified in this data sheet.

ICS uses some of these reserved bits to invoke auxiliary functions. To ensure proper operation of the ICS1892, an STA must maintain the default value of these bits. Therefore, ICS recommends that an STA always write the default value of any reserved bits during all management register write operations.

To ensure proper operation of the ICS1892, an STA must maintain the default value of these bits. Therefore, ICS recommends that an STA always write the default value of any reserved bits during all management register write operations.

8.7.5 Selector Field (bits 5.4:0)

The Selector Field bits indicate the technology or encoding that the remote link partner is using for the Auto-Negotiation message. The ICS1892 supports only IEEE Std 802.3, represented by a value of 00001b in bits 5.4:0. The ISO/IEC standard defines the Selector Field technologies in Annex 28A. Presently, the IEEE standard defines the following two valid codes:

- 00001b (IEEE Std 802.3)
- 00010b (IEEE Std 802.9)

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8.8 Register 6: Auto-Negotiation Expansion Register

Table 8-13 lists the bits for the Auto-Negotiation Expansion Register, which indicates the status of the Auto-Negotiation process.

Note: For an explanation of acronyms used in Table 8-13, see Chapter 1, "Abbreviations and Acronyms".

Table 8-13. Auto-Negotiation Expansion Register (register 6 [0x06])

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
6.15	IEEE reserved	Always 0	N/A	CW	–	0†	0
6.14	IEEE reserved	Always 0	N/A	CW	–	0†	
6.13	IEEE reserved	Always 0	N/A	CW	–	0†	
6.12	IEEE reserved	Always 0	N/A	CW	–	0†	
6.11	IEEE reserved	Always 0	N/A	CW	–	0†	0
6.10	IEEE reserved	Always 0	N/A	CW	–	0†	
6.9	IEEE reserved	Always 0	N/A	CW	–	0†	
6.8	IEEE reserved	Always 0	N/A	CW	–	0†	
6.7	IEEE reserved	Always 0	N/A	CW	–	0†	0
6.6	IEEE reserved	Always 0	N/A	CW	–	0†	
6.5	IEEE reserved	Always 0	N/A	CW	–	0†	
6.4	Parallel detection fault	No Fault	Multiple technologies detected	RO	LH	0	
6.3	Link partner Next Page able	Link partner is not Next Page able	Link partner is Next Page able	RO	–	0	4
6.2	Next Page able	Local device is not Next Page able	Local device is Next Page able	RO	–	1	
6.1	Page received	Next Page not received	Next Page received	RO	LH	0	
6.0	Link partner Auto-Negotiation able	Link partner is not Auto-Negotiation able	Link partner is Auto-Negotiation able	RO	–	0	

† As per the IEEE Std 802.3u, during any write operation to any bit in this register, the STA must write the default value to all Reserved bits.

8.8.1 IEEE Reserved Bits (bits 6.15:5)

The ISO/IEC specification reserves these bits for future use. When an STA:

- Reads a reserved bit, the ICS1892 returns a logic zero.
- Writes to a reserved bit, the STA must use the default value specified in this data sheet.

ICS uses some of these reserved bits to invoke auxiliary functions. To ensure proper operation of the ICS1892, an STA must maintain the default value of these bits. Therefore, ICS recommends that an STA always write the default value of any reserved bits during all management register write operations.

Reserved bits 5.15:5 are Command Override Write (CW) bits. When the Command Register Override bit (bit 16.15) is logic:

- Zero, the ICS1892 isolates all STA writes to CW bits.
- One, an STA can modify the value of these bits

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8.8.2 Parallel Detection Fault (bit 6.4)

The ICS1892 sets this bit to a logic one if a parallel detection fault is encountered. A parallel detection fault occurs when the ICS1892 cannot disseminate the technology being used by its remote link partner.

Bit 6.4 is a latching high (LH) status bit. (For more information on latching high and latching low bits, see Section 8.1.4.1, “Latching High Bits” and Section 8.1.4.2, “Latching Low Bits”.)

8.8.3 Link Partner Next Page Able (bit 6.3)

Bit 6.3 is a status bit that reports the capabilities of the remote link partner to support the Next Page features of the auto-negotiation process. The ICS1892 sets this bit to a logic one if the remote link partner sets the Next Page bit in its Link Control Word.

8.8.4 Next Page Able (bit 6.2)

Bit 6.2 is a status bit that reports the capabilities of the ICS1892 to support the Next Page features of the auto-negotiation process. The ICS1892 sets this bit to a logic one to indicate that it is capable of supporting these features.

8.8.5 Page Received (bit 6.1)

The ICS1892 sets this bit to a logic one if a parallel detection fault is encountered. A parallel detection fault occurs when the ICS1892 cannot disseminate the technology being used by its remote link partner.

Bit 6.1 is a latching high (LH) status bit. (For more information on latching high and latching low bits, see Section 8.1.4.1, “Latching High Bits” and Section 8.1.4.2, “Latching Low Bits”.)

8.8.6 Link Partner Auto-Negotiation Able (bit 6.0)

If the ICS1892:

- Does not receive Fast Link Pulse bursts from its remote link partner, then this bit remains a logic zero.
- Receives valid FLP bursts from its remote link partner (thereby indicating that it can participate in the auto-negotiation process), then the ICS1892 sets this bit to a logic one.

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8.9 Register 7: Auto-Negotiation Next Page Transmit Register

Table 8-14 lists the bits for the Auto-Negotiation Next Page Transmit Register, which establishes the contents of the Next Page Link Control Word that is transmitted during Next Page Operations. This table is compliant with the ISO/IEC specification.

Note: For an explanation of acronyms used in Table 8-14, see Chapter 1, "Abbreviations and Acronyms".

Table 8-14. Auto-Negotiation Next Page Transmit Register (register 7 [0x07])

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
7.15	Next Page	Last Page	Additional Pages follow	RW	–	0	2
7.14	IEEE reserved	Always 0	N/A	RO	–	0†	
7.13	Message Page	Unformatted Page	Message Page	RW	–	1	
7.12	Acknowledge 2	Cannot comply with Message	Can comply with Message	RW	–	0	
7.11	Toggle	Previous Link Code Word was zero	Previous Link Code Word was one	RO	–	0	0
7.10	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	
7.9	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	
7.8	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	
7.7	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	0
7.6	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	
7.5	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	
7.4	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	
7.3	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	1
7.2	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	
7.1	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	
7.0	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	1	

† As per the IEEE Std 802.3u, during any write operation to any bit in this register, the STA must write the default value to all Reserved bits.

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8.9.1 Next Page (bit 7.15)

This bit is used by a PHY/STA to enable the transmission of Next Pages following the base Link Control Word as long as the remote link partner supports the Next Page features of Auto-Negotiation.

This bit is used to establish the state of the Next Page (NP) bit of the Next Page Link Control Word (that is, the NP bit of the Next Page Link Control Word tracks this bit). During a Next Page exchange, if the NP bit is logic:

- Zero, it indicates to the remote link partner that this is the last Message or Page.
- One, it indicates to the remote link partner that additional Pages follow this Message.

8.9.2 IEEE Reserved Bit (bit 7.14)

The ISO/IEC specification reserves this bit for future use. When this reserved bits is:

- Read by an STA, the ICS1892 returns a logic zero.
- Written to by an STA, the STA must use the default value specified in this data sheet.

ICS uses some of these reserved bits to invoke auxiliary functions. To ensure proper operation of the ICS1892, an STA must maintain the default value of these bits. Therefore, ICS recommends that an STA always write the default value of any reserved bits during all management register write operations.

8.9.3 Message Page (bit 7.13)

The Message Page (MP) bit (bit 7.13) is used to determine the format or type of Page being transmitted. The value of this bit establishes the state of the MP bit in the Next Page Link Control Word.

If this bit is set to logic:

- Zero, it indicates that the Page is an Unformatted Page.
- One, it indicates to the remote link partner that the Page being transmitted is a Message Page.

8.9.4 Acknowledge 2 (bit 7.12)

This bit is used to indicate the ability of the ICS1892 to comply with a message.

The value of this bit establishes the state of the Ack2 bit in the Next Page Link Control Word. If this bit is set to logic:

- Zero, it indicates that the ICS1892 cannot comply with the message.
- One, it indicates to the remote link partner that the ICS1892 can comply with the message.

8.9.5 Toggle (bit 7.11)

The Toggle (T) bit (bit 7.11) is used to synchronize the transmission of Next Page messages with the remote link partner. The value of this bit establishes the state of the Toggle bit in the Next Page Link Control Word. This bit toggles with each transmitted Link Control Word.

If the previous Next Page Link Control Word Toggle bit has a value of logic:

- Zero, then the Toggle bit is set to logic one.
- One, then the Toggle bit is set to logic zero.

The initial Next Page Link Control Word Toggle bit is set to the inverse of the base Link Control Word bit 11.

8.9.6 Message Code Field / Unformatted Code Field (bits 7.10:0)

Bits 7.10:0 represent either the Message Code field M[10:0] or the Unformatted Code field U[10:0] bits. The value of these bits establish the state of the M[10:0] / U[10:0] bits in the Next Page Link Control Word.

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8.10 Register 8: Auto-Negotiation Next Page Link Partner Ability Register

Table 8-15 lists the bits for the Auto-Negotiation Next Page Link Partner Ability Register, which establishes the contents of the Next Page Link Control Word that is transmitted during Next Page Operations. This table is compliant with the ISO/IEC specification.

Note: For an explanation of acronyms used in Table 8-15, see Chapter 1, "Abbreviations and Acronyms".

Table 8-15. Auto-Negotiation Next Page Link Partner Ability Register (register 8 [0x08])

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
8.15	Next Page	Last Page	Additional Pages follow	RO	–	0	0
8.14	IEEE reserved	Always 0	N/A	RO	–	0†	
8.13	Message Page	Unformatted Page	Message Page	RO	–	0	
8.12	Acknowledge 2	Cannot comply with Message	Can comply with Message	RO	–	0	
8.11	Toggle	Previous Link Code Word was zero	Previous Link Code Word was one	RO	–	0	0
8.10	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	
8.9	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	
8.8	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	
8.7	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	0
8.6	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	
8.5	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	
8.4	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	
8.3	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	0
8.2	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	
8.1	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	
8.0	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	

† As per the IEEE Std 802.3u, during any write operation to any bit in this register, the STA must write the default value to all Reserved bits.

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8.10.1 Next Page (bit 8.15)

This bit is used by a PHY/STA to enable the transmission of Next Pages following the base Link Control Word as long as the remote link partner supports the Next Page features of Auto-Negotiation.

This bit is used to establish the state of the Next Page (NP) bit of the Next Page Link Control Word (that is, the NP bit of the Next Page Link Control word tracks this bit). During a Next Page exchange, if the NP bit is logic:

- Zero, it indicates to the remote link partner that this is the last Message or Page.
- One, it indicates to the remote link partner that additional Pages follow this Message.

8.10.2 IEEE Reserved Bit (bit 8.14)

The ISO/IEC specification reserves this bit for future use. When this reserved bits is:

- Read by an STA, the ICS1892 returns a logic zero.
- Written to by an STA, the STA must use the default value specified in this data sheet.

ICS uses some of these reserved bits to invoke auxiliary functions. To ensure proper operation of the ICS1892, an STA must maintain the default value of these bits. Therefore, ICS recommends that an STA always write the default value of any reserved bits during all management register write operations.

8.10.3 Message Page (bit 8.13)

The Message Page (MP) bit (bit 8.13) is used to determine the format or type of Page being transmitted. The value of this bit establishes the state of the MP bit in the Next Page Link Control Word.

If this bit is set to logic:

- Zero, it indicates that the Page is an Unformatted Page.
- One, it indicates to the remote link partner that the Page being transmitted is a Message Page.

8.10.4 Acknowledge 2 (bit 8.12)

This bit is used to indicate the ability of the ICS1892 to comply with a message.

The value of this bit establishes the state of the Ack2 bit in the Next Page Link Control Word. If this bit is set to logic:

- Zero, it indicates that the ICS1892 cannot comply with the message.
- One, it indicates to the remote link partner that the ICS1892 can comply with the message.

If the previous Next Page Link Control Word Toggle bit has a value of logic:

- Zero, then the Toggle bit is set to logic one.
- One, then the Toggle bit is set to logic zero.

The initial Next Page Link Control Word Toggle bit is set to the inverse of the base Link Control Word bit 11.

8.10.5 Message Code Field / Unformatted Code Field (bits 8.10:0)

Bits 8.10:0 represent either the Message Code field M[10:0] or the Unformatted Code field U[10:0] bits. The value of these bits establish the state of the M[10:0] / U[10:0] bits in the Next Page Link Control Word.

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8.11 Register 16: Extended Control Register

Table 8-16 lists the bits for the Extended Control Register, which the ICS1892 provides to allow an STA to customize the operations of the device.

Note:

1. For an explanation of acronyms used in Table 8-16, see Chapter 1, "Abbreviations and Acronyms".
2. During any write operation to any bit in this register, the STA must write the default value to all Reserved bits.

Table 8-16. Extended Control Register (register 16 [0x10])

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
16.15	Command Override Write enable	Disabled	Enabled	RW	SC	0	–
16.14	ICS reserved	Read unspecified	Read unspecified	RW/0	–	0	
16.13	ICS reserved	Read unspecified	Read unspecified	RW/0	–	0	
16.12	ICS reserved	Read unspecified	Read unspecified	RW/0	–	0	
16.11	ICS reserved	Read unspecified	Read unspecified	RW/0	–	0	–
16.10	PHY Address Bit 4	For a detailed explanation of this bit's operation, see Section 6.9, "Status Interface".		RO	–	P4RD†	
16.9	PHY Address Bit 3	For a detailed explanation of this bit's operation, see Section 6.9, "Status Interface".		RO	–	P3TD†	
16.8	PHY Address Bit 2	For a detailed explanation of this bit's operation, see Section 6.9, "Status Interface".		RO	–	P2LI†	
16.7	PHY Address Bit 1	For a detailed explanation of this bit's operation, see Section 6.9, "Status Interface".		RO	–	P1CL†	–
16.6	PHY Address Bit 0	For a detailed explanation of this bit's operation, see Section 6.9, "Status Interface".		RO	–	P0AC†	
16.5	Stream Cipher Test Mode	Normal operation	Test mode	RW	–	0	
16.4	ICS reserved	Read unspecified	Read unspecified	RW/0	–	–	
16.3	NRZ/NRZI encoding	NRZ encoding	NRZI encoding	RW	–	1	8
16.2	Transmit invalid codes	Disabled	Enabled	RW	–	0	
16.1	ICS reserved	Read unspecified	Read unspecified	RW/0	–	0	
16.0	Stream Cipher disable	Stream Cipher enabled	Stream Cipher disabled	RW	–	0	

† The default is the state of this pin at reset.

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8.11.1 Command Override Write Enable (bit 16.15)

The Command Override Write Enable bit provides an STA the ability to alter the Command Override Write (CW) bits located throughout the MII Register set. A two-step process is required to alter the value of a CW bit:

1. Step one is to issue a Command Override, that is, bit 16.15 is set to logic one.
2. Step two immediately follows, which is a write to the CW bit that you wish to change. (The Command Override Write Enable bit is a Self-Clearing bit that is automatically reset to logic zero after the next MII write, thereby allowing only one subsequent write to alter a CW bit.)

8.11.2 ICS Reserved (bits 16.14:11)

ICS is reserving these bits for future use. Functionally, these bits are equivalent to IEEE Reserved bits. When one of these reserved bits is:

- Read by an STA, the ICS1892 returns a logic zero.
- Written to by an STA, the STA must use the default value specified in this data sheet.

ICS uses some of these reserved bits to invoke auxiliary functions. To ensure proper operation of the ICS1892, an STA must maintain the default value of these bits. Therefore, ICS recommends that an STA always write the default value of any reserved bits during all management register write operations.

8.11.3 PHY Address (bits 16.10:6)

These five bits hold the Serial Management Port Address of the ICS1892. During either a hardware reset or a power-on reset, the PHY address is read from the LED interface. (For information on the LED interface, see Section 6.9, “Status Interface” and Section 9.2.2, “Multi-Function (Multiplexed) Pins: PHY Address and LED Pins”). The PHY address is then latched into this register. (The value of each of the PHY Address bits is unaffected by a software reset.)

8.11.4 Stream Cipher Scrambler Test Mode (bit 16.5)

The Stream Cipher Scrambler Test Mode bit is used to force the ICS1892 to lose LOCK, thereby requiring the Stream Cipher Scrambler to resynchronize.

8.11.5 ICS Reserved (bit 16.4)

See Section 8.11.2, “ICS Reserved (bits 16.14:11)”, the text for which also applies here.

8.11.6 NRZ/NRZI Encoding (bit 16.3)

This bit allows an STA to control whether NRZ (Not Return to Zero) or NRZI (Not Return to Zero, Invert on One) encoding is applied to the serial transmit data stream in 100Base-TX mode. When this bit is logic:

- Zero, the ICS1892 encodes the serial transmit data stream using NRZ encoding.
- One, the ICS1892 encodes the serial transmit data stream using NRZI encoding.

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8.11.7 Invalid Error Code Test (bit 16.2)

The Invalid Error Code Test bit allows an STA to force the ICS1892 to transmit symbols that are typically classified as invalid. The purpose of this test bit is to permit thorough testing of the 4B/5B encoding and the serial transmit data stream by allowing generation of bit patterns that are considered invalid by the ISO/IEC 4B/5B definition.

When this bit is logic:

- Zero, the ISO/IEC defined 4B/5B translation takes place.
- One – and the TXER signal is asserted by the MAC/repeater – the MII input nibbles are translated according to Table 8-17.

Table 8-17. Invalid Error Code Translation Table

Symbol	Meaning	MII Input Nibble	Translation
V	Invalid Code	0000	00000
V	Invalid Code	0001	00001
V	Invalid Code	0010	00010
V	Invalid Code	0011	00011
H	Error	0100	00100
V	Invalid Code	0101	00101
V	Invalid Code	0110	00110
R	ESD	0111	00111
V	Invalid Code	1000	00000
T	ESD	1001	01101
V	Invalid Code	1010	01100
K	SSD	1011	10001
V	Invalid Code	1100	10000
V (S)	Invalid Code	1101	11001
J	SSD	1110	11000
I	Idle	1111	11111

8.11.8 ICS Reserved (bit 16.1)

See Section 8.11.2, “ICS Reserved (bits 16.14:11)”, the text for which also applies here.

8.11.9 Stream Cipher Disable (bit 16.0)

The Stream Cipher Disable bit allows an STA to control whether the ICS1892 employs the Stream Cipher Scrambler in the transmit and receive data paths. When this bit is set to logic:

- Zero, the Stream Cipher Encoder and Decoder are both enabled for normal operations.
- One, the Stream Cipher Encoder and Decoder are disabled. This action results in an unscrambled data stream (for example, the ICS1892 transmits unscrambled IDLES, and so forth.

Note: The Stream Cipher Scrambler can be used only for 100-MHz operations.

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8.12 Register 17: Quick Poll Detailed Status Register

Table 8-18 lists the bits for the Quick-Poll Detailed Status Register. This register is a 16-bit read-only register used to provide an STA with detailed status of the ICS1892 operations. During reset, it is initialized to pre-defined default values.

Note:

1. For an explanation of acronyms used in Table 8-18, see Chapter 1, "Abbreviations and Acronyms".
2. Most of this register's bits are latching high or latching low, which allows the ICS1892 to capture and save the occurrence of an event for an STA to read. (For more information on latching high and latching low bits, see Section 8.1.4.1, "Latching High Bits" and Section 8.1.4.2, "Latching Low Bits".)
3. Although some of these status bits are redundant with other management registers, the ICS1892 provides this group of bits to minimize the number of Serial Management Cycles required to collect the status data.
4. During any write operation to any bit in this register, the STA must write the default value to all Reserved bits.

Table 8-18. Quick Poll Detailed Status Register (register 17 [0x11])

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
17.15	Data rate	10 Mbps	100 Mbps	RO	–	–	–
17.14	Duplex	Half duplex	Full duplex	RO	–	–	
17.13	Auto-Negotiation Progress Monitor Bit 2	Reference Decode Table	Reference Decode Table	RO	LMX	0	
17.12	Auto-Negotiation Progress Monitor Bit 1	Reference Decode Table	Reference Decode Table	RO	LMX	0	
17.11	Auto-Negotiation Progress Monitor Bit 0	Reference Decode Table	Reference Decode Table	RO	LMX	0	0
17.10	100Base-TX signal lost	Valid signal	Signal lost	RO	LH	0	
17.9	Phase-Locked Loop locked	PLL locked	PLL failed to lock	RO	LH	0	
17.8	False Carrier detect	Normal Carrier or Idle	False Carrier	RO	LH	0	
17.7	Invalid symbol detected	Valid symbols observed	Invalid symbol received	RO	LH	0	0
17.6	Halt Symbol detected	No Halt Symbol received	Halt Symbol received	RO	LH	0	
17.5	Premature End detected	Normal data stream	Stream contained two IDLE symbols	RO	LH	0	
17.4	Auto-Negotiation complete	Auto-Negotiation in process	Auto-Negotiation complete	RO	–	0	
17.3	100Base-TX signal detect	No signal present	Signal present	RO	–	0	0
17.2	Jabber detect	No jabber detected	Jabber detected	RO	LH	0	
17.1	Remote fault	No remote fault detected	Remote fault detected	RO	LH	0	
17.0	Link Status	Link is not valid	Link is valid	RO	LL	0	

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8.12.1 Data Rate (bit 17.15)

The Data Rate bit indicates the ‘selected technology’. If the ICS1892 is in:

- Hardware mode, the value of this bit is determined by the 10/100SEL input pin.
- Software mode, the value of this bit is determined by the Data Rate bit 0.13.

When bit 17.15 is logic:

- Zero, it indicates that 10-MHz operations are selected.
- One, the ICS1892 is indicating that 100-MHz operations are selected.

Note: This bit does not imply any link status.

8.12.2 Duplex (bit 17.14)

The Duplex bit indicates the ‘selected technology’. If the ICS1892 is in:

- Hardware mode, the value of this bit is determined by the DPXSEL input pin.
- Software mode, the value of this bit is determined by the Duplex Mode bit 0.8.

When bit 17.14 is logic:

- Zero, it indicates that half-duplex operations are selected.
- One, the ICS1892 is indicating that full-duplex operations are selected.

Note: This bit does not imply any link status.

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8.12.3 Auto-Negotiation Progress Monitor (bits 17.13:11)

The Auto-Negotiation Progress Monitor consists of the Auto-Negotiation Complete bit (bit 17.4) and the three Auto-Negotiation Monitor bits (bits 17.13:11). The Auto-Negotiation Progress Monitor continually examines the state of the Auto-Negotiation Process State Machine and reports the status of Auto-Negotiation using the three Auto-Negotiation Monitor bits. Therefore, the value of these three bits provides the status of the Auto-Negotiation Process.

These three bits are initialized to logic zero in one of the following ways:

- A reset (see Section 5.1, “Reset Operations”)
- Disabling Auto-Negotiation [see Section 8.2.4, “Auto-Negotiation Enable (bit 0.12)”]
- Restarting Auto-Negotiation [see Section 8.2.7, “Restart Auto-Negotiation (bit 0.9)”]

If Auto-Negotiation is enabled, these bits continually latch the highest state that the Auto-Negotiation State Machine achieves. That is, they are updated only if the binary value of the next state is greater than the binary value of the present state as outlined in Table 8-19.

Note: An MDIO read of these bits provides a history of the greatest progress achieved by the auto-negotiation process. In addition, the MDIO read latches the present state of the Auto-Negotiation State Machine for a subsequent read.

Table 8-19. Auto-Negotiation State Machine (Progress Monitor)

Auto-Negotiation State Machine	Auto-Negotiation Progress Monitor			
	Auto-Negotiation Complete Bit (Bit 17.4)	Auto-Negotiation Monitor Bit 2 (Bit 17.13)	Auto-Negotiation Monitor Bit 1 (Bit 17.12)	Auto-Negotiation Monitor Bit 0 (Bit 17.11)
Idle	0	0	0	0
Parallel Detected	0	0	0	1
Parallel Detection Failure	0	0	1	0
Ability Matched	0	0	1	1
Acknowledge Match Failure	0	1	0	0
Acknowledge Matched	0	1	0	1
Consistency Match Failure	0	1	1	0
Consistency Matched	0	1	1	1
Auto-Negotiation Completed Successfully	1	0	0	0

8.12.4 100Base Receive Signal Lost (bit 17.10)

The 100Base Receive Signal Lost bit indicates to an STA whether the ICS1892 has lost its 100Base Receive Signal. If this bit is set to a logic:

- Zero, it indicates the Receive Signal has remained valid since the last read of this register.
- One, it indicates the Receive Signal was lost after the last read of this register.

This bit is a latching high bit. (For more information on latching high and latching low bits, see Section 8.1.4.1, “Latching High Bits” and Section 8.1.4.2, “Latching Low Bits”.)

Note: This bit has no definition in 10Base-T mode.

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8.12.5 PLL Lock Error (bit 17.9)

The Phase Locked Loop (PLL) Lock Error bit indicates to an STA whether the ICS1892 has ever experienced a PLL Lock Error. A PLL Lock Error occurs when a the PLL fails to lock onto the incoming 100Base data stream. If this bit is set to a logic:

- Zero, it indicates that a PLL Lock Error has not occurred since the last read of this register.
- One, it indicates that a PLL Lock Error has occurred after the last read of this register.

This bit is a latching high bit. (For more information on latching high and latching low bits, see Section 8.1.4.1, “Latching High Bits” and Section 8.1.4.2, “Latching Low Bits”.)

Note: This bit has no definition in 10Base-T mode.

8.12.6 False Carrier (bit 17.8)

The False Carrier bit indicates to an STA the detection of a False Carrier by the ICS1892 in 100Base mode.

A False Carrier occurs when the ICS1892 begins evaluating potential data on the incoming 100Base data stream, only to learn that it was not a valid /J/K/. If this bit is set to a logic:

- Zero, it indicates that a False Carrier has not been detected since the last read of this register.
- One, it indicates that a False Carrier was detected since the last read of this register.

This bit is a latching high bit. (For more information on latching high and latching low bits, see Section 8.1.4.1, “Latching High Bits” and Section 8.1.4.2, “Latching Low Bits”.)

Note: This bit has no definition in 10Base-T mode.

8.12.7 Invalid Symbol (bit 17.7)

The Invalid Symbol bit indicates to an STA the detection of an Invalid Symbol in a 100Base data stream by the ICS1892.

During reception of a valid packet, the ICS1892 examines each Symbol to ensure that the data being passed to the MAC/Repeater Interface is error free. If an error occurs, the ICS1892 indicates this condition to the MAC/repeater. An Invalid Symbol occurs when the ICS1892 evaluates a valid packet and finds an Invalid Symbol in the data.

If this bit is set to a logic:

- Zero, it indicates an Invalid Symbol has not been detected since the last read of this register.
- One, it indicates an Invalid Symbol was detected since the last read of this register.

This bit is a latching high bit. (For more information on latching high and latching low bits, see Section 8.1.4.1, “Latching High Bits” and Section 8.1.4.2, “Latching Low Bits”.)

Note: This bit has no definition in 10Base-T mode.

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8.12.8 Halt Symbol (bit 17.6)

The Halt Symbol bit indicates to an STA the detection of an Halt Symbol in a 100Base data stream by the ICS1892.

During reception of a valid packet, the ICS1892 examines each symbol to ensure that the data being passed to the MAC/Repeater Interface is error free. In addition, it looks for special symbols such as the Halt Symbol. If a Halt Symbol is encountered, the ICS1892 indicates this condition to the MAC/repeater.

If this bit is set to a logic:

- Zero, it indicates a Halt Symbol has not been detected since the last read of this register.
- One, it indicates a Halt Symbol was detected in the packet since the last read of this register.

This bit is a latching high bit. (For more information on latching high and latching low bits, see Section 8.1.4.1, “Latching High Bits” and Section 8.1.4.2, “Latching Low Bits”.)

Note: This bit has no definition in 10Base-T mode.

8.12.9 Premature End (bit 17.5)

The Premature End bit indicates to an STA the detection of two consecutive Idles in a 100Base data stream by the ICS1892.

During reception of a valid packet, the ICS1892 examines each symbol to ensure that the data being passed to the MAC/Repeater Interface is error free. If two consecutive Idles are encountered it indicates this condition to the MAC/repeater by setting this bit.

If this bit is set to a logic:

- Zero, it indicates a Premature End condition has not been detected since the last read of this register.
- One, it indicates a Premature End condition was detected in the packet since the last read of this register.

This bit is a latching high bit. (For more information on latching high and latching low bits, see Section 8.1.4.1, “Latching High Bits” and Section 8.1.4.2, “Latching Low Bits”.)

Note: This bit has no definition in 10Base-T mode.

8.12.10 Auto-Negotiation Complete (bit 17.4)

The Auto-Negotiation Complete bit is used to indicate to an STA the completion of the Auto-Negotiation process. When this bit is set to logic:

- Zero, it indicates that the auto-negotiation process is either not complete or is disabled by the Control Register’s Auto-Negotiation Enable bit (bit 0.12)
- One, it indicates that the ICS1892 has completed the auto-negotiation process and that the contents of Management Registers 4, 5, and 6 are valid.

8.12.11 100Base-TX Signal Detect (bit 17.3)

The 100Base-TX Signal Detect bit indicates either the presence or absence of a signal on the Twisted-Pair Receive pins (TP_RXP and TP_RXN) in 100Base-TX mode. This bit is logic:

- Zero when no signal is detected on the Twisted-Pair Receive pins and logic.
- One when a signal is present on these pins.

8.12.12 Jabber Detect (bit 17.2)

Bit 17.2 is functionally identical to bit 1.1. The Jabber Detect bit indicates whether a jabber condition has occurred. This bit is a 10Base-T function.

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8.12.13 Remote Fault (bit 17.1)

Bit 17.1 is functionally identical to bit 1.4.

8.12.14 Link Status (bit 17.0)

Bit 17.0 is functionally identical to bit 1.2.

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8.13 Register 18: 10Base-T Operations Register

The 10Base-T Operations Register provides an STA with the ability to monitor and control the ICS1892 activity while the ICS1892 is operating in 10Base-T mode.

Note:

1. For an explanation of acronyms used in Table 8-20, see Chapter 1, “Abbreviations and Acronyms”.
2. During any write operation to any bit in this register, the STA must write the default value to all Reserved bits.

Table 8-20. 10Base-T Operations Register (register 18 [0x12])

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
18.15	ICS reserved	Read unspecified	Read unspecified	RW/0	SC	0	–
18.14	Polarity reversed	Normal polarity	Polarity reversed	RO	LH	0	
18.13	ICS reserved	Read unspecified	Read unspecified	RW/0	–	–	
18.12	ICS reserved	Read unspecified	Read unspecified	RW/0	–	–	
18.11	ICS reserved	Read unspecified	Read unspecified	RW/0	–	–	–
18.10	ICS reserved	Read unspecified	Read unspecified	RW/0	–	–	
18.9	ICS reserved	Read unspecified	Read unspecified	RW/0	–	–	
18.8	ICS reserved	Read unspecified	Read unspecified	RW/0	–	–	
18.7	ICS reserved	Read unspecified	Read unspecified	RW/0	–	–	–
18.6	ICS reserved	Read unspecified	Read unspecified	RW/0	–	–	
18.5	Jabber inhibit	Normal Jabber behavior	Jabber Check disabled	RW	–	0	
18.4	ICS reserved	Read unspecified	Read unspecified	RW/1	–	1	
18.3	Auto polarity inhibit	Polarity automatically corrected	Polarity not automatically corrected	RW	–	0	0
18.2	SQE test inhibit	Normal SQE test behavior	SQE test disabled	RW	–	0	
18.1	Link Loss inhibit	Normal Link Loss behavior	Link Always = Link Pass	RW	–	0	
18.0	Squelch inhibit	Normal squelch behavior	No squelch	RW	–	0	

8.13.1 ICS Reserved (bit 18.15)

ICS reserves this bit for future use. Functionally, this bit is equivalent to an IEEE Reserved bit. When this reserved bits is:

- Read by an STA, the ICS1892 returns a logic zero.
- Written to by an STA, the STA must use the default value specified in this data sheet.

In general, ICS uses some reserved bits to invoke auxiliary functions. To ensure proper operation of the ICS1892, an STA must maintain the default value of these bits. Therefore, ICS recommends that an STA always write the default value of any reserved bits during all management register write operations.

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8.13.2 Polarity Reversed (bit 18.14)

The Polarity Reversed bit is used to inform an STA whether the ICS1892 has detected that the signals on the Twisted-Pair Receive Pins (TP_RXP and TP_RXN) are reversed. When the signal polarity is:

- Correct, the ICS1892 sets bit 18.14 to a logic zero.
- Reversed, the ICS1892 sets bit 18.14 to logic one.

Note: The ICS1892 can detect this situation and perform all its operations normally, independent of the reversal.

8.13.3 ICS Reserved (bits 18.13:6)

See Section 8.13.1, “ICS Reserved (bit 18.15)”, the text for which also applies here.

8.13.4 Jabber Inhibit (bit 18.5)

The Jabber Inhibit bit allows an STA to disable Jabber Detection. When an STA sets this bit to:

- Zero, the ICS1892 enables 10Base-T Jabber checking.
- One, the ICS1892 disables its check for a Jabber condition during data transmission.

8.13.5 ICS Reserved (bit 18.4)

See Section 8.13.1, “ICS Reserved (bit 18.15)”, the text for which also applies here.

8.13.6 Auto Polarity Inhibit (bit 18.3)

The Auto Polarity Inhibit bit allows an STA to prevent the automatic correction of a polarity reversal on the Twisted-Pair Receive pins (TP_RXP and TP_RXN). If an STA sets this bit to logic:

- Zero (the default), the ICS1892 automatically corrects a polarity reversal on the Twisted-Pair Receive pins.
- One, the ICS1892 either disables or inhibits the automatic correction of reversed Twisted-Pair Receive pins.

Note: This bit is also used to correct a reversed signal polarity for 100Base-TX operations.

8.13.7 SQE Test Inhibit (bit 18.2)

The SQE Test Inhibit bit allows an STA to prevent the generation of the Signal Quality Error pulse. When an STA sets this bit to logic:

- Zero, the ICS1892 enables its SQE Test generation.
- One, the ICS1892 disables its SQE Test generation.

The SQE Test provides the ability to verify that the Collision Logic is active and functional. A 10Base-T SQE test is performed by pulsing the Collision signal for a short time after each packet transmission completes, that is, after TXEN goes inactive.

Note:

1. The SQE Test is automatically inhibited in full-duplex and repeater modes, thereby disabling the functionality of this bit.
2. This bit is a control bit and not a status bit. Therefore, it is not updated to indicate this automatic inhibiting of the SQE test in full-duplex mode or repeater mode.

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8.13.8 Link Loss Inhibit (bit 18.1)

The Link Loss Inhibit bit allows an STA to prevent the ICS1892 from dropping the link in 10Base-T mode. When an STA sets this bit to logic:

- Zero, the state machine behaves normally and the link status is based on the signaling detected Twisted-Pair Receiver inputs.
- One, the ICS1892 10Base-T Link Integrity Test state machine is forced into the 'Link Passed' state regardless of the Twisted-Pair Receiver input conditions.

8.13.9 Squelch Inhibit (bit 18.0)

The Squelch Inhibit bit allows an STA to control the ICS1892 Squelch Detection in 10Base-T mode. When an STA sets this bit to logic:

- Zero, before the ICS1892 can establish a valid link, the ICS1892 must receive valid 10Base-T data.
- One, before the ICS1892 can establish a valid link, the ICS1892 must receive both valid 10Base-T data followed by an IDL.

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8.14 Register 19: Extended Control Register 2

The Extended Control Register provides more refined control of the internal ICS1892 operations.

Note:

1. For an explanation of acronyms used in Table 8-20, see Chapter 1, “Abbreviations and Acronyms”.
2. During any write operation to any bit in this register, the STA must write the default value to all Reserved bits.

Table 8-21. Extended Control Register (register [0x13])

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
19.15	Node/Repeater Mode	Node mode	Repeater mode	RO	–	NOD/ REP†	–
19.14	Hardware/Software Mode	Hardware mode	Software mode	RO	–	HW/ SW†	
19.13	Remote Fault	No faults detected	Remote fault detected	RO	–	0	
19.12	ICS reserved	Read unspecified	Read unspecified	RW	–	0	
19.11	ICS reserved	Read unspecified	Read unspecified	RW	–	0	0
19.10	ICS reserved	Read unspecified	Read unspecified	RO	–	0	
19.9	ICS reserved	Read unspecified	Read unspecified	RW	–	0	
19.8	ICS reserved	Read unspecified	Read unspecified	RW	–	0	
19.7	ICS reserved	Read unspecified	Read unspecified	RW	–	0	0
19.6	ICS reserved	Read unspecified	Read unspecified	RW	–	0	
19.5	ICS reserved	Read unspecified	Read unspecified	RW	–	0	
19.4	ICS reserved	Read unspecified	Read unspecified	RW	–	0	
19.3	ICS reserved	Read unspecified	Read unspecified	RW	–	0	3
19.2	ICS reserved	Read unspecified	Read unspecified	RW	–	0	
19.1	Automatic 10Base-T Power Down	Do not automatically power down	Power down automatically	RW	–	1	
19.0	Automatic 100Base-TX Power Down	Do not automatically power down	Power down automatically	RW	–	1	

† The default is the state of this pin at reset.

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8.14.1 Node/Repeater Configuration (bit 19.15)

The Node/Repeater Configuration bit directly indicates the state of the NOD/REP input pin. When this bit is logic:

- Zero, the NOD/REP input pin is pulled down, which instructs the operation code to operate in Node mode.
- One, the NOD/REP input pin is pulled up, which instructs the ICS1892 to operate in Repeater mode.

There are two primary differences between Node mode and Repeater mode.

- In Node mode:
  - The SQE Test default setting is enabled.
  - The Carrier Sense signal (CRS) is asserted in response to either transmit or receive activity.
- In Repeater mode:
  - The SQE Test default setting is disabled.
  - The Carrier Sense signal (CRS) is asserted in response only to receive activity.

8.14.2 Hardware/Software Priority Status (bit 19.14)

The Hardware/Software Priority Status bit directly indicates the state of the HW/SW pin. When this bit is logic:

- Zero, the hardware pins have priority over the (software) register bits for establishing the ICS1892 configuration.
- One, the (software) register bits have priority over the hardware pins for establishing the ICS1892 configuration.

8.14.3 Remote Fault (bit 19.13)

The ISO/IEC specification defines bit 5.13 as the Remote Fault bit, and bit 19.13 is functionally identical to bit 5.13. The Remote Fault bit is set based on the Link Control Word received from the remote link partner. When this bit is a logic:

- Zero, it indicates the remote link partner does not detect a Link Fault.
- One, it indicates to the ICS1892/STA that the remote link partner detects a Link Fault.

8.14.4 ICS Reserved (bits 19.12:2)

ICS reserves these bits for future use. Functionally, these bits are equivalent to an IEEE Reserved bit. When each of these reserved bits is:

- Read by an STA, the ICS1892 returns a logic zero.
- Written to by an STA, the STA must use the default value specified in this data sheet.

In general, ICS uses some reserved bits to invoke auxiliary functions. To ensure proper operation of the ICS1892, an STA must maintain the default value of these bits. Therefore, ICS recommends that an STA always write the default value of any reserved bits during all management register write operations.

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8.14.5 Automatic 10Base-T Power-Down (bit 19.1)

The Automatic 10Base-T Power Down bit provides an STA the means of enabling the ICS1892 to automatically shut down 10Base-T support functions when 100Base-TX operations are being employed. When this bit is set to logic:

- Zero, the 10Base-T Transceiver does not power down automatically in 100Base-TX mode.
- One, and the ICS1892 is operating in 100Base-TX mode, the 10Base-T Transceiver automatically turns off to reduce the overall power consumption of the ICS1892.

Note: There are other means of powering down the 10Base-T Transceiver (for example, when the entire device is isolated, using bit 0:10).

8.14.6 Automatic 100Base-TX Power-Down (bit 19.0)

The Automatic 100Base-TX Power Down bit provides an STA with the means of enabling the ICS1892 to automatically shut down 100Base-TX support functions when 10Base-T operations are being employed. When this bit is set to logic:

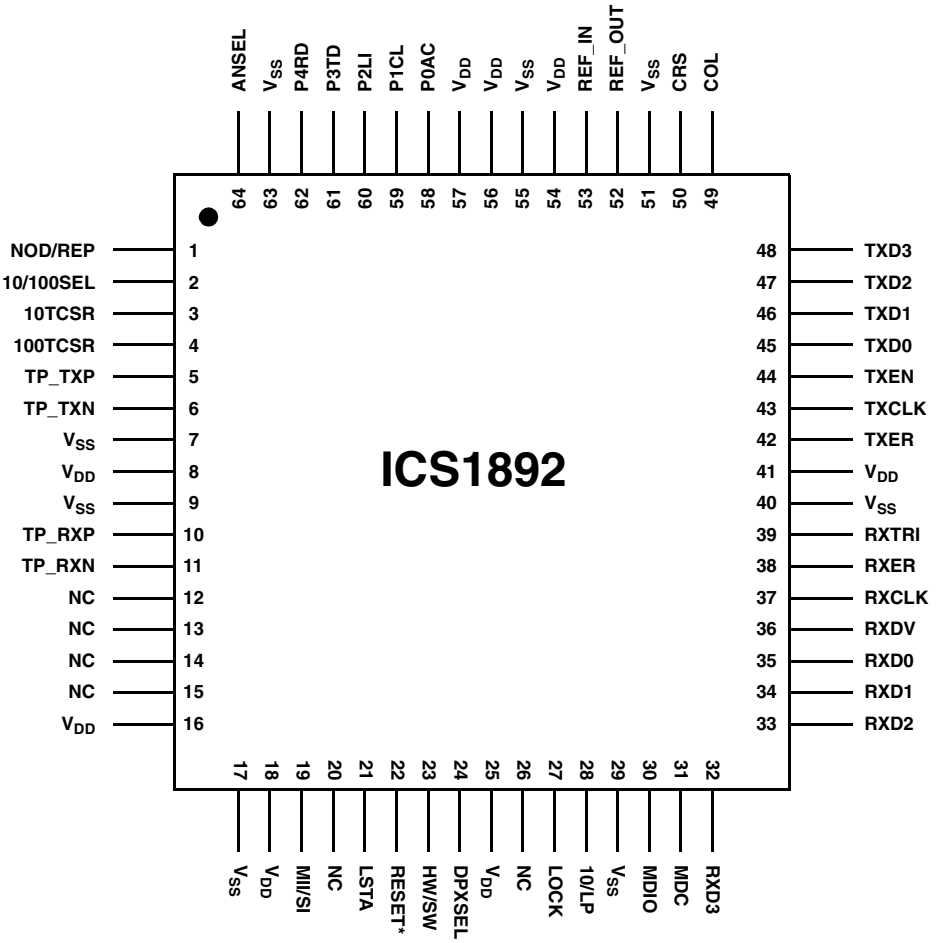
- Zero, the 100Base-TX Transceiver does not power down automatically in 100Base-TX mode.
- One, and the ICS1892 is operating in 10Base-T mode, the 100Base-TX Transceiver automatically turns off to reduce the overall power consumption of the ICS1892.

Note: There are other means of powering down the 100Base-TX Transceiver (for example, when the entire device is isolated using bit 0:10).

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Chapter 9 Pin Diagram, Listings, and Descriptions

9.1 ICS1892 Pin Diagram



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9.1.1 Pin Listing by Pin Number

Table 9-1 lists the ICS1892 pins by pin number.

Table 9-1. ICS1892 Pins, by Pin Number

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	NOD/REP	17	V_{SS}	33	RXD2	49	COL
2	10/100SEL	18	V_{DD}	34	RXD1	50	CRS
3	10TCSR	19	MII/SI	35	RXD0	51	V_{SS}
4	100TCSR	20	NC	36	RXDV	52	REF_OUT
5	TP_TXP	21	LSTA	37	RXCLK	53	REF_IN
6	TP_TXN	22	RESET*	38	RXER	54	V_{DD}
7	V_{SS}	23	HW/SW	39	RXTRI	55	V_{SS}
8	V_{DD}	24	DPXSEL	40	V_{SS}	56	V_{DD}
9	V_{SS}	25	V_{DD}	41	V_{DD}	57	V_{DD}
10	TP_RXP	26	NC	42	TXER	58	P0AC
11	TP_RXN	27	LOCK	43	TXCLK	59	P1CL
12	NC	28	10/LP	44	TXEN	60	P2LI
13	NC	29	V_{SS}	45	TXD0	61	P3TD
14	NC	30	MDIO	46	TXD1	62	P4RD
15	NC	31	MDC	47	TXD2	63	V_{SS}
16	V_{DD}	32	RXD3	48	TXD3	64	ANSEL

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9.1.2 Pin Listings by Alphabetical Pin Name

Table 9-2 lists the ICS1892 pins alphabetically by pin name.

Table 9-2. ICS1892 Pins, by Alphabetical Pin Name

Pin Name	Pin Number
10/100SEL	2
10/LP	28
10TCSR	3
100TCSR	4
ANSEL	64
COL	49
CRS	50
DPXSEL	24
HW/SW	23
LOCK	27
LSTA	21
MDC	31
MDIO	30
MII/SI	19
NC	12
NC	13
NC	14
NC	15
NC	20
NC	26
NOD/REP	1
P0AC	58
P1CL	59
P2LI	60

Pin Name	Pin Number
P3TD	61
P4RD	62
REF_IN	53
REF_OUT	52
RESET*	22
RXCLK	37
RXD0	35
RXD1	34
RXD2	33
RXD3	32
RXDV	36
RXER	38
RXTRI	39
TP_RXN	11
TP_RXP	10
TP_TXN	6
TP_TXP	5
TXCLK	43
TXD0	45
TXD1	46
TXD2	47
TXD3	48
TXEN	44

Pin Name	Pin Number
TXER	42
V_{DD}	8
V_{DD}	16
V_{DD}	18
V_{DD}	25
V_{DD}	41
V_{DD}	54
V_{DD}	56
V_{DD}	57
V_{SS}	7
V_{SS}	17
V_{SS}	29
V_{SS}	40
V_{SS}	51
V_{SS}	55
V_{SS}	63
V_{SS}	63
V_{SS}	9

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9.2 ICS1892 Pin Descriptions

The tables in this section list the ICS1892 pins by their functional grouping.

9.2.1 Transformer Interface Pins

Table 9-3 lists the pins for the transformer interface group of pins.

Table 9-3. Transformer Interface Pins

Pin Name	Pin Number	Pin Type	Pin Description
TP_RXN	11	Input	**Twisted-Pair Receive (Data) Negative.** Within this table, see the description at pin 10, TP_RXP.
TP_RXP	10	Input	**Twisted-Pair Receive (Data) Positive.** Data reception of differential analog signals occurs over the TP_RXN and TP_RXP pair of differential-signal pins. Together these pins receive the serial bit stream from the UTP cable through an isolation transformer. Depending on the operating mode of the remote link partner, the received data is one of the following types of signals: • Two-level (10Base-T, that is, Manchester encoded) signals • Three-level (100Base-TX, that is, MLT-3 encoded) signals These signals interface directly to an isolation transformer, which in turn, interfaces with the UTP cable.
TP_TXN	6	Output	**Twisted-Pair Transmit (Data) Negative.** Within this table, see the description at pin 5, TP_TXP.
TP_TXP	5	Output	**Twisted-Pair Transmit (Data) Positive.** Differential analog signal transmission occurs over the TP_TXN and TP_TXP pair of pins. Together these pins drive the serial bit stream over the UTP cable. Depending on the operating mode of the ICS1892 MDI, the current-driven differential driver produces one of the following types of signals: • Two-level (10Base-T, that is, Manchester encoded) signals • Three-level (100Base-TX, that is, MLT-3 encoded) signals These signals interface directly to an isolation transformer, which in turn, drives the UTP cable.

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9.2.2 Multi-Function (Multiplexed) Pins: PHY Address and LED Pins

Table 9-4 lists the pins for the multifunction group of pins (that is, the multiplexed PHY Address / LED pins).

Note:

1. During either a power-on reset or a hardware reset, each multi-function configuration pin is an input that is sampled when the ICS1892 exists the reset state. After sampling is complete, these pins are output pins that can drive status LEDs.
2. A software reset does not affect the state of a multi-function configuration pin. During a software reset, all multi-function configuration pins are outputs.
3. Each multi-function configuration pin must be pulled either up or down with a resistor to establish the address of the ICS1892. LEDs placed in series with these resistors provide a designated status indicator.

Caution: All pins listed inTable 9.4 must not float.

4. As outputs, the asserted state of a multi-function configuration pin is the inverse of the sense sampled during reset. This inversion provides a signal that can illuminate an LED during an asserted state. For example, if a multi-function configuration pin is pulled down to ground through an LED and a current-limiting resistor, then the sampled sense of the input is low. To illuminate an LED for the asserted state requires the output to be high.

Caution: PHY Address 00 will tri-state the MII interface.

Note: Each of these pins monitor the data link by providing signals that directly drive LEDs.

Table 9-4. PHY Address and LED Pins

Pin Name	Pin Number	Pin Type	Pin Description
P0AC, P1CL, P2LI, P3TD, P4RD	58, 59, 60, 61, 62	Input or Output	**PHY (Address Bit) 0 / Activity LED.** **PHY (Address Bit) 1 / Collision LED.** **PHY (Address Bit) 2 / Link Integrity LED.** **PHY (Address Bit) 3 / Transmit Data LED.** **PHY (Address Bit) 4 / Receive Data LED.** The ‘Pin Type’ for these multiplexed pins depends on the where the ICS1892 is in its reset cycle. • During a reset of the ICS1892, these pins act as inputs. • After a reset of the ICS1892, these pins latch the state of the inputs into their respective PHY Address bits. (See Table 8-16.) The ICS1892 then converts the pin signal to an output that can drive the respective LED directly. For more information, see Section 6.9, “Status Interface”.

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9.2.3 Configuration Pins

Table 9-5 lists the configuration pins.

Table 9-5. Configuration Pins

Pin Name	Pin Number	Pin Type	Pin Description
10/100SEL	2	Input or Output	**10Base-T / 100Base-TX Select.** The 'Pin Type' for this pin depends on the setting for the HW/SW pin (pin 23). When the HW/SW pin is set for: • Hardware mode, this pin acts as an input. In this case, when the signal on this pin is logic: – Low, this pin selects 10Base-T operations. – High, this pin selects 100Base-TX operations. • Software mode, this pin acts as an output that indicates the current status of this pin. In this case, when the signal on this pin is logic: – Low, this pin indicates 10Base-T operations are selected. – High, this pin indicates 100Base-TX operations are selected.
10/LP	28	Input	**10M Serial / Link Pulse (Stream Interface).** • For this pin to have any affect on the MAC/Repeater Interface: – The 10/100SEL pin must be logic zero (that is, 10-MHz mode). – The MII/SI pin must be logic one (that is, Stream Interface mode). • When both the 10/100 SEL and MII/SI pins are set as required, then this 10/LP pin selects between the 10M Serial Interface and the Link Pulse Interface for the MAC/Repeater Interface. When the signal on this pin is logic: – Low, this pin selects the 10M Serial Interface. – High, this pin selects the Link Pulse Interface.
10TCSR	3	Input	**10M Transmit Current Set Resistor.** • A resistor, connected between this pin and ground, is required to establish the value of the transmit current used in 10Base-T mode. • The value and tolerance of this resistor is specified in Section 10.3, "Recommended Component Values".
100TCSR	4	Input	**100M Transmit Current Set Resistor.** • A resistor, connected between this pin and ground, is required to establish the value of the transmit current used in 100Base-TX mode. • The value and tolerance of this resistor is specified in Section 10.3, "Recommended Component Values".
ANSEL	64	Input or Output	**Auto-Negotiation Select.** The 'Pin Type' for this pin depends on the setting for the HW/SW pin (pin 23). When the HW/SW pin is set for: • Hardware mode, this pin acts as an input. In this case, when the signal on this pin is logic: – Low, this pin does not select Auto-Negotiation operations. – High, this pin selects Auto-Negotiation operations. • Software mode, this pin acts as an output that indicates the current status of this pin. In this case, when the signal on this pin is logic: – Low, this pin indicates that Auto-Negotiation is disabled. – High, this pin indicates that Auto-Negotiation is enabled.

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Table 9-5. Configuration Pins (*Continued*)

Pin Name	Pin Number	Pin Type	Pin Description
DPXSEL	24	Input or Output	**Half-Duplex / Full-Duplex Select.** The 'Pin Type' for this pin depends on the setting for the HW/SW pin (pin 23). When the HW/SW pin is set for: • Hardware mode, this pin acts as an input. In this case, when the signal on this pin is logic: – Low, this pin selects half-duplex operations. – High, this pin selects full-duplex operations. • Software mode, this pin acts as an output that indicates the current status of this pin. In this case, when the signal on this pin is logic: – Low, this pin indicates that it is set for half-duplex operations. – High, this pin indicates that it is set for full-duplex operations.
HW/SW	23	Input	**Hardware/Software (Select).** When the signal on this pin is logic: • Low, this pin selects Hardware mode operations. • High, this pin selects Software mode operations.
LOCK	27	Output	**(Stream Cipher) Lock (Acquired).** When the signal on this pin is logic: • Low, the ICS1892 does not have a lock on the data stream. • High, the 1892 has a lock on the data stream.
LSTA	21	Output	**Link Status.** This pin is used to report the status of the link segment. When the signal on this pin is logic: • Low, there is no link established. • High, there is a link established. This pin is mapped according to the interface for which the ICS1892 is mapped. For the: • Media Independent Interface (MII), the LSTA is mapped as LSTA. • 100M Symbol Interface, the LSTA is mapped as SD. • 10M Serial Interface, the LSTA is mapped as LSTA. • Link Pulse Interface, the LSTA is mapped as SD.
MII/SI	19	Input	**Media Independent Interface / Stream Interface (Select).** This pin is used in combination with the 10/LP and 10/100SEL pins to configure the ICS1892 MAC/Repeater Interface. When the signal on this pin is logic: • Low, this pin configures the MAC/Repeater Interface as a Media Independent Interface. • High, this pin configures the MAC/Repeater Interface as a Stream Interface.
NOD/REP	1	Input	**Node/Repeater (Select).** This selection on this pin affects both the SQE test and the Carrier Sense (CSR) signal. When the signal on this pin is logic: • Low, this pin enables the ICS1892 to default to node operations. • High, this pin enables the ICS1892 to default to repeater operations.

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Table 9-5. Configuration Pins (*Continued*)

Pin Name	Pin Number	Pin Type	Pin Description
REF_IN	53	Input	**(Frequency) Reference Input.** This pin can be connected to either of the following frequency reference sources: • A 25-MHz crystal • A 25-MHz oscillator For the tolerance of the clock that is used, see Section 10.5.1, "Timing for Clock Reference In (REF_IN) Pin".
REF_OUT	52	Input	**(Frequency) Reference Output.** When the frequency reference source used is a: • A 25-MHz crystal, this pin is used in combination with the REF_IN pin. • A 25-MHz oscillator, this pin is left unconnected.
RESET*	22	Input	**(System) Reset (*Active Low*).** • When the signal on this active-low pin is logic: – Low, the ICS1892 is in hardware reset. – High, the ICS1892 is operational. • For more information on hardware resets, see the following: – Section 5.1.2.1, "Hardware Reset" – Section 10.5.17, "Reset: Hardware Reset and Power-Down"

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9.2.4 MAC/Repeater Interface Pins

This section lists pin descriptions for each of the following interfaces

- Section 9.2.4.1, “MAC/Repeater Interface Pins for Media Independent Interface”
- Section 9.2.4.2, “MAC/Repeater Interface Pins for 100M Symbol Interface”
- Section 9.2.4.3, “MAC/Repeater Interface Pins for 10M Serial Interface”
- Section 9.2.4.4, “MAC/Repeater Interface Pins for Link Pulse Interface”

9.2.4.1 MAC/Repeater Interface Pins for Media Independent Interface

Table 9-6 lists the MAC/Repeater Interface pin descriptions for the MII.

Table 9-6. MAC/Repeater Interface Pins: Media Independent Interface (MII)

Pin Name	Pin Number	Pin Type	Pin Description
COL	49	Output	**Collision (Detect).** The ICS1892 asserts a signal on the COL pin when the ICS1892 detects receive activity while transmitting (that is, while the TXEN signal is asserted by the MAC/repeater, that is, when transmitting). When the mode is: • 10Base-T, the ICS1892 detects receive activity by monitoring the un-squelched MDI receive signal. • 100Base-TX, the ICS1892 detects receive activity when there are two non-contiguous zeros in any 10-bit symbol derived from the MDI receive data stream. **Note:** 1. The signal on the COL pin is not synchronous to either RXCLK or TXCLK. 2. In full-duplex mode, the COL signal is disabled and always remains low. 3. The COL signal is asserted as part of the signal quality error (SQE) test. This assertion can be suppressed with the SQE Test Inhibit bit (bit 18.2).
CRS	50	Output	**Carrier Sense.** • In half-duplex mode, the ICS1892 asserts a signal on the CRS pin when the ICS1892 detects either receive or transmit activity. • In full-duplex mode and Repeater mode, the ICS1892 asserts a signal on the CRS pin only when the ICS1892 detects receive activity. **Note:** The signal on the CRS pin is not synchronous to either RXCLK or TXCLK.
MDC	31	Input	**Management Data Clock.** The ICS1892 uses the signal on the MDC pin to synchronize the transfer of management information between the ICS1892 and the Station Management Entity (STA), using the serial MDIO data line. The MDC signal is sourced by the STA.

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Table 9-6. MAC/Repeater Interface Pins: Media Independent Interface (MII) (*Continued*)

<table>
<tr><th>Pin Name</th><th>Pin Number</th><th>Pin Type</th><th>Pin Description</th></tr>
<tr><td>MDIO</td><td>30</td><td>Input/ Output</td><td>Management Data Input/Output.
This pin's signal is a tri-statable line driven by one of the following:
• Station management (STA), to transfer command information
• The ICS1892, to transfer status information.
All transfers and sampling are synchronous with the signal on the MDC pin.
Note: If the ICS1892 is to be used in an application that uses the mechanical MII specification, MDIO must have a 1.5 kΩ ±5% pull-up resistor at the ICS1892 end and a 2 kΩ ±5% pull-down resistor at the station management end. (These resistors enable the station management to determine if the connection is intact.)</td></tr>
<tr><td>RXCLK</td><td>37</td><td></td><td>Receive Clock.
The ICS1892 sources the RXCLK to the MAC/repeater. The ICS1892 uses RXCLK to synchronize the signals on the following pins: RXD0–3, RXDV, and RXER. The following table contrasts the behavior on the RXCLK pin when the mode for the ICS1892 is either 10Base-T or 100Base-TX.
<table>
<tr><th>10Base-T</th><th>100Base-TX</th></tr>
<tr><td>The RXCLK frequency is 2.5 MHz.</td><td>The RXCLK frequency is 25 MHz.</td></tr>
<tr><td>The ICS1892 generates RXCLK from the MDI data stream using a digital PLL. When the MDI data stream terminates, the PLL continues to operate, synchronously referenced to the last packet received.</td><td>The ICS1892 generates RXCLK from the MDI data stream while there is a valid link (that is, either data or IDLEs). In the absence of a link, the ICS1892 uses the REFIN clock to generate the RXCLK.</td></tr>
<tr><td>The ICS1892 switches between clock sources during the period between when CRS is being asserted and RXDV is being asserted. While the ICS1892 locks onto the incoming data stream, a clock phase change of up to 360 degrees can occur.</td><td>The ICS1892 switches between clock sources during the period between when CRS is being asserted and RXDV is being asserted. While the ICS1892 is bringing up a link, a clock phase change of up to 360 degrees can occur.</td></tr>
</table>
Note: The signal on the RXCLK pin is conditioned by RXTRI.</td></tr>
<tr><td>RXD0,
RXD1,
RXD2,
RXD3</td><td>35,
34,
33,
32</td><td></td><td>Receive Data 0–3.
• RXD0 is the least-significant bit and RXD3 is the most-significant bit of the MII receive data nibble.
• While the ICS1892 asserts RXDV, the ICS1892 transfers the receive data signals on the RXD0–RXD3 pins to the MAC/Repeater Interface synchronously on the rising edges of RXCLK.</td></tr>
</table>

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Table 9-6. MAC/Repeater Interface Pins: Media Independent Interface (MII) (*Continued*)

Pin Name	Pin Number	Pin Type	Pin Description
RXDV	36	Output	**Receive Data Valid.** The ICS1892 asserts RXDV to indicate to the MAC/repeater that data is available on the MII Receive Bus (RXD[3:0]). The ICS1892: • Asserts RXDV after it detects and recovers the Start-of-Stream delimiter, /J/K/. (For the timing reference, see Chapter 10.5.6, "MII / 100M Stream Interface: Synchronous Receive Timing".) • De-asserts RXDV after it detects either the End-of-Stream delimiter (/T/R/) or a signal error. **Note:** RXDV is synchronous with the Receive Data Clock, RXCLK.
RXER	38	Output	**Receive Error.** In 100Base-TX mode, the ICS1892 asserts a signal on the RXER pin under two conditions: • When errors are detected during the reception of valid frames. • When a False Carrier is detected. **Note:** 1. The ICS1892 asserts a signal on RXER upon detection of a False Carrier so that repeater applications can prevent the propagation of a False Carrier. 2. RXER always transitions synchronously with RXCLK.
RXTRI	39	Input	**Receive (Interface), Tri-State.** The input on this pin is from a MAC. When the signal on this pin is logic: • Low, the MAC indicates that it is not in a tri-state condition. • High, the MAC indicates that it is in a tri-state condition. In this case, the ICS1892 acts to ensure that only one PHY is active at a time. • PHY address 00 will also act as RXTRI.
TXCLK	43		**Transmit Clock.** The ICS1892 generates this clock signal to synchronize the transfer of data from the MAC/Repeater Interface to the ICS1892. When the mode is: • 10Base-T, the TXCLK frequency is 2.5 MHz. • 100Base-TX, the TXCLK frequency is 25 MHz.
TXD0, TXD1, TXD2, TXD3	45, 46, 47, 48	Input	**Transmit Data 0–3.** • TXD0 is the least-significant bit and TXD3 is the most-significant bit of the MII transmit data nibble received from the MAC/repeater. • While the ICS1892 asserts TXEN, the signals on the TXD0–TXD3 pins are sampled by the ICS1892 synchronously on the rising edges of TXCLK.

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Table 9-6. MAC/Repeater Interface Pins: Media Independent Interface (MII) (*Continued*)

Pin Name	Pin Number	Pin Type	Pin Description
TXEN	44	Input	**Transmit Enable.** The signal on this pin indicates to the ICS1892 that the MAC/repeater is sending valid data nibbles for transmission on the physical media. • Synchronous with the assertion of TXEN, the ICS1892 begins reading the data nibbles on the transmit data lines and transmitting them over the media. • Following the de-assertion of TXEN, the ICS1892 terminates transmission of nibbles.
TXER	42	Input	**Transmit Error.** When the mode is: • 10Base-T, TXER is not required. • 100Base-TX mode: – The assertion of TXER by the MAC/repeater causes the ICS1892 to transmit Invalid Symbols. (The ICS1892 synchronously samples the TXER signal on the rising edges of TXCLK.) – The Invalid Symbol used for this function is the HALT symbol, which is substituted for the transmit nibble received from the MAC/repeater. – When the Invalid Error Code Test bit (bit 16.2) is set to logic one, the 5-bit symbol shown in the Invalid Error Code Translation Table (Table 8-17) is used instead of the normal 4B/5B encoding described in the ISO/IEC specification.

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9.2.4.2 MAC/Repeater Interface Pins for 100M Symbol Interface

Table 9-7 lists the MAC/Repeater Interface pin descriptions for the 100M Symbol Interface.

Table 9-7. MAC/Repeater Interface Pins: 100M Symbol Interface

MII Pin Name	100M Symbol Pin Name	Pin No.	Pin Type	Pin Description
COL	–	49	No Connect	**Collision (Detect).** For the 100M Symbol Interface, this pin is a no connect. For more information, see Table 6-1.
CRS	SCRS	50	Output	**Symbol Carrier Sense.** This pin's description is the same as that given in Table 9-6.
MDC	MDC	31	Input	**Management Data Clock.** This pin's description is the same as that given in Table 9-6.
MDIO	MDIO	30	Input/ Output	**Management Data Input/Output.** This pin's description is the same as that given in Table 9-6.
RXCLK	SRCLK	37		**Symbol Receive Clock.** The ICS1892 sources the SRCLK to the MAC/repeater. The ICS1892 uses SRCLK to synchronize the signals on the SRD0–4 pins. The following table contrasts the behavior on the SRCLK pin when the mode for the ICS1892 is either 10Base-T or 100Base-TX.

100Base-TX
The SRCLK frequency is 25 MHz.
The ICS1892 generates SRCLK from the MDI data stream while there is a valid link (that is, either data or IDLEs). In the absence of a link, the ICS1892 uses the REFIN clock to generate the SRCLK.
The ICS1892 switches between clock sources during the period between when SCRS is being asserted and RXDV is being asserted. While the ICS1892 is bringing up a link, a clock phase change of up to 360 degrees can occur.

Note: The signal on the SRCLK pin is conditioned by RXTRI, that is, the Receive (Interface) Tri-State signal.

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Table 9-7. MAC/Repeater Interface Pins: 100M Symbol Interface (*Continued*)

MII Pin Name	100M Symbol Pin Name	Pin No.	Pin Type	Pin Description
RXD0, RXD1, RXD2, RXD3	SRD0, SRD1, SRD2, SRD3	35, 34, 33, 32		**Symbol Receive Data 0–3.** • SRD0 is the least-significant bit and SRD3 is the most-significant bit of the MII receive data nibble. • While the ICS1892 asserts RXDV, the ICS1892 transfers the receive data signals on the SRD0–SRD3 pins to the MAC/Repeater Interface synchronously on the rising edges of SRCLK.
RXDV	–	36	No Connect	**Receive Data Valid.** For the 100M Symbol Interface, this pin is a no connect. For more information, see Table 6-1.
RXER	SRD4	38	Output	**Symbol Receive Data 4.** This pin's description is the same as that given in Table 9-6.
RXTRI		39	Input	**Receive (Interface), Tri-State.** The input on this pin is from a MAC. When the signal on this pin is logic: • Low, the MAC indicates that it is not in a tri-state condition. • High, the MAC indicates that it is in a tri-state condition. In this case, the ICS1892 acts to ensure that only one PHY is active at a time.
TXCLK	STCLK	43		**Symbol Transmit Clock.** This pin's description is the same as that given in Table 9-6. For 100Base-Tx
TXD0–3	STD0, STD1, STD2, STD3	45, 46, 47, 48	Input	**Symbol Transmit Data 0–3.** • STD0 is the least-significant bit and STD3 is the most-significant bit of the MII transmit data nibble received from the MAC/repeater. • While the ICS1892 asserts TXEN, the signals on the STD0–3 pins are sampled by the ICS1892 synchronously on the rising edges of STCLK.
TXEN	–	44	No Connect	**Transmit Enable.** For the 100M Symbol Interface, this pin is a no connect. For more information, see Table 6-1.
TXER	STD4	42	Input	**Symbol Transmit Data 4.** This pin's description is the same as that given in Table 9-6.

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9.2.4.3 MAC/Repeater Interface Pins for 10M Serial Interface

Table 9-8 lists the MAC/Repeater Interface pin descriptions for the 10M Serial Interface.

Table 9-8. MAC/Repeater Interface Pins: 10M Serial Interface

MII Pin Name	10M Serial Pin Name	Pin No.	Pin Type	Pin Description
COL	10COL	49	Output	**10M (Serial Interface) Collision (Detect).** This pin's description is the same as that given in Table 9-6.
CRS	10CRS	50	Output	**10M (Serial Interface) Carrier Sense.** This pin's description is the same as that given in Table 9-6.
MDC	MDC	31	Input	**Management Data Clock.** This pin's description is the same as that given in Table 9-6.
MDIO	MDIO	30	Input/ Output	**Management Data Input/Output.** This pin's description is the same as that given in Table 9-6.
RXCLK	10RCLK	37		**10M (Serial Interface) Receive Clock.** This pin's description is the same as that given in Table 9-6.
RXCLK	10RCLK	37		**10M (Serial Interface) Receive Clock.** The 10RCLK pin name is the 10M Serial Interface mapping of the MII RXCLK (Receive Clock) pin name. The ICS1892 sources the 10RCLK to the MAC/repeater. The ICS1892 uses 10RCLK to synchronize the signals on the 10RD and 10RXDV pins. The following table contrasts the behavior on the 10RCLK pin when the mode for the ICS1892 is either 10Base-T or 100Base-TX. **10Base-T Serial** The10RCLK frequency is 10 MHz. The ICS1892 generates 10RCLK from the MDI data stream using a digital PLL. When the MDI data stream terminates, the PLL continues to operate, synchronously referenced to the last packet received. The ICS1892 switches between clock sources during the period between when 10CRS is being asserted and 10RXDV is being asserted. While the ICS1892 locks onto the incoming data stream, a clock phase change of up to 360 degrees can occur. **Note:** The signal on the 10RCLK pin is conditioned by RXTRI.

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Table 9-8. MAC/Repeater Interface Pins: 10M Serial Interface (*Continued*)

MII Pin Name	10M Serial Pin Name	Pin No.	Pin Type	Pin Description
RXD0	10RD	35		**10M (Serial Interface) Receive Data.** This pin's description is the same as that given in Table 9-6.
RXD1, RXD2, RXD3	–	34, 33, 32	No Connect	**Receive Data 1–3.** For the 10M Serial Interface, these pins are a no connect. For more information, see Table 6-2.
RXDV	10RXDV	36	Output	**10M (Serial Interface) Receive Data Valid.** The ICS1892 asserts 10RXDV to indicate to the MAC/repeater that data is available on the MII Receive Bus (RXD[3:0]). The ICS1892: • Asserts 10RXDV after it detects and recovers the Start-of-Stream delimiter, /J/K/. (For the timing reference, see Chapter 10.5.6, "MII / 100M Stream Interface: Synchronous Receive Timing".) • De-asserts 10RXDV after it detects either the End-of-Stream delimiter (/T/R/) or a signal error. **Note:** 10RXDV is synchronous with the Receive Data Clock, 10RCLK.
RXER	–	38	No connect	**Receive Error.** For the 10M Serial Interface, this pin is a no connect. For more information, see Table 6-2.
RXTRI		39	Input	**Receive (Interface), Tri-State.** The input on this pin is from a MAC. When the signal on this pin is logic: • Low, the MAC indicates that it is not in a tri-state condition. • High, the MAC indicates that it is in a tri-state condition. In this case, the ICS1892 acts to ensure that only one PHY is active at a time.
TXER	–	42	No connect	**Transmit Error.** For the 10M Serial Interface, this pin is a no connect. For more information, see Table 6-2.
TXCLK	10TCLK	43		**10M (Serial Interface) Transmit Clock.** In 10M Serial TXCLK is 10 MHz.
TXD0	10TD	45	Input	**10M (Serial Interface) Transmit Data.** This pin's description is the same as that given in Table 9-6.
TXD1, TXD2, TXD3	–	46, 47, 48	No connect	**Transmit Data 1–3.** For the 10M Serial Interface, these pins are a no connect. For more information, see Table 6-2.
TXEN	10TXEN	44	Input	**10M (Serial Interface) Transmit Enable.** This pin's description is the same as that given in Table 9-6.
TXER	–	42	No connect	**Transmit Error.** For the 10M Serial Interface, these pins are a no connect. For more information, see Table 6-2.

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9.2.4.4 MAC/Repeater Interface Pins for Link Pulse Interface

Table 9-9 lists the MAC/Repeater Interface pin descriptions for the Link Pulse Interface.

Table 9-9. MAC/Repeater Interface Pins: Link Pulse Interface

MII Pin Name	Link Pluse Pin Name	Pin No.	Pin Type	Pin Description
COL	–	49	No Connect	**Collision (Detect).** For the Link Pulse Interface, this pin is a no connect. For more information, see Table 6-3.
CRS	–	50	No Connect	**Carrier Sense.** For the Link Pulse Interface, this pin is a no connect. For more information, see Table 6-3.
RXER	LPRX	38	Output	**Link Pulse (Interface) Receive Error.** This pin's description is the same as that given in Table 9-6.
RXCLK	LRCLK	37	Output	**Link (Pulse Interface) Receive Clock.** The ICS1892 sources the LRCLK to the MAC/repeater. The ICS1892 uses LRCLK to synchronize the signals on the LPRX pin. The signal on the LRCLK pin is conditioned by RXTRI.
MDC	MDC	31	Input	**Management Data Clock.** This pin's description is the same as that given in Table 9-6.
MDIO	MDIO	30	Input/ Output	**Management Data Input/Output.** This pin's description is the same as that given in Table 9-6.
RXD0, RXD1, RXD2, RXD3	–	35, 34, 33, 32	No Connect	**Receive Data 0–3.** For the Link Pulse Interface, these pins are a no connect. For more information, see Table 6-3.
RXDV	–	36	No Connect	**Receive Data Valid.** For the Link Pulse Interface, this pin is a no connect. For more information, see Table 6-3.
RXER	LPRX	38	Output	**Link Pulse (Interface) Receive Error.** This pin's description is the same as that given in Table 9-6.
RXTRI		39	Input	**Receive (Interface), Tri-State.** The input on this pin is from a MAC. When the signal on this pin is logic: • Low, the MAC indicates that it is not in a tri-state condition. • High, the MAC indicates that it is in a tri-state condition. In this case, the ICS1892 acts to ensure that only one PHY is active at a time.
TXCLK	LTCLK	43		**Link (Pulse Interface) Transmit Clock.** This pin's description is the same as that given in Table 9-6.
TXD0, TXD1, TXD2, TXD3	–	45, 46, 47, 48	No Connect	**Transmit Data 0–3.** For the Link Pulse Interface, these pins are a no connect. For more information, see Table 6-3.

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Table 9-9. MAC/Repeater Interface Pins: Link Pulse Interface (*Continued*)

MII Pin Name	Link Pluse Pin Name	Pin No.	Pin Type	Pin Description
TXEN	–	44	No Connect	**Transmit Enable.** For the Link Pulse Interface, this pin is a no connect. For more information, see Table 6-3.
TXER	LPTX	42	Input	**Link Pulse (Interface) Transmit Error.** This pin's description is the same as that given in Table 9-6.

9.2.5 Reserved Pins

Table 9-10 lists the reserved pins.

Table 9-10. Reserved Pins

Pin Name	Pin Number	Pin Type	Pin Description
NC	12, 13, 14, 15, 20, 26	–	**No Connect.** • These pins are always reserved for use by ICS. • Depending on the interface that is used, other pins can also be no-connects. For pins that are no connects when the interface is the: – 100M Symbol Interface, see Section 9.2.4.2, "MAC/Repeater Interface Pins for 100M Symbol Interface". – 10M Serial Interface, see Section 9.2.4.3, "MAC/Repeater Interface Pins for 10M Serial Interface". – Link Pulse Interface, see Section 9.2.4.4, "MAC/Repeater Interface Pins for Link Pulse Interface". **Caution:** 'No-Connect' pins must not be connected, as connecting them can affect the performance of the ICS1892.

9.2.6 Ground and Power Pins

Table 9-11 lists the ground and power pins.

Table 9-11. Ground and Power Pins

Pin Name	Pin Number	Pin Type	Pin Description
V_{SS}	7	Ground	Analog Domain
V_{SS}	17	Ground	Analog Domain
V_{SS}	29	Ground	Analog Domain
V_{SS}	51	Ground	Analog Domain
V_{SS}	55	Ground	Analog Domain
V_{SS}	40	Ground	Digital Domain
V_{SS}	63	Ground	Digital Domain
V_{SS}	9	Ground	Analog Domain
V_{DD}	8	Power	Analog Domain
V_{DD}	16	Power	Analog Domain

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Table 9-11. Ground and Power Pins

Pin Name	Pin Number	Pin Type	Pin Description
V_{DD}	18	Power	Analog Domain
V_{DD}	25	Power	Analog Domain
V_{DD}	56	Power	Analog Domain
V_{DD}	41	Power	Digital Domain
V_{DD}	54	Power	Digital Domain
V_{DD}	57	Power	Digital Domain

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Chapter 10 DC and AC Operating Conditions

10.1 Absolute Maximum Ratings

Table 10-1 lists the absolute maximum ratings for the ICS1892. Stresses above these ratings can cause permanent damage to the ICS1892. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the ICS1892 at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 10-1. Absolute Maximum Ratings

Item	Rating
V_{DD} (measured to V_{SS})	5.5 V
Digital Inputs / Outputs	V_{SS} -0.5 to V_{DD} +0.5 V
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C
Power Dissipation	See Section 10.4.1, “DC Operating Characteristics for Supply Current”

10.2 Recommended Operating Conditions

Table 10-2 lists the recommended operating conditions for the ICS1892.

Table 10-2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Minimum	Maximum	Units
Ambient Operating Temperature	T_A	–	0	+70	° C
Power Supply Voltage (measured with respect to V_{SS})	V_{DD}	–	+4.75	+5.25	V

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10.3 Recommended Component Values

Table 10-3 lists the recommended component values for the ICS1892.

Table 10-3. Recommended Component Values

Parameter	Minimum	Typical	Maximum	Tolerance	Units
Crystal Frequency	–	25	–	± 50 ppm †	MHz
10TCSR Resistor Value	–	2.0k	–	1%	Ω
100TCSR Resistor Value	–	7.15k	–	1%	Ω
LED Resistor Value	510	1k	10k	–	Ω

Note: Do not put bypass capacitors across the 10TCSR or 100TCSR resistors. The bypass capacitor will cause the bandgap circuit to oscillate.

† There are two IEEE Std 802.3 requirements that drive the tolerance for the frequency of the crystal.

- Clause 22.2.2.1 requires the MII TX_CLK to have an accuracy of ± 100 ppm.
- Clause 24.2.3.4 is more stringent. It requires the code-bit timer to have an accuracy of 0.005% (that is, ±50 ppm).

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10.4 DC Operating Characteristics

This section lists the DC operating characteristics for the ICS1892.

10.4.1 DC Operating Characteristics for Supply Current

Table 10-4 lists the DC operating characteristics for the supply current to the ICS1892.

Note: All V_{DD} measurements are taken with respect to V_{SS} (which equals 0 V).

Table 10-4. DC Operating Characteristics for Supply Current

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Supply Current†	I_{DD}	100Base-TX Mode	V_{DD} = 5.25 V	–	162	180	mA
Supply Current†	I_{DD}	10Base-T Mode	V_{DD} = 5.25 V	–	133	147	mA
Supply Current†	I_{DD}	Auto-Negotiation Mode	V_{DD} = 5.25 V	–	162	180	mA
Supply Current†	I_{DD}	Power-Down Mode	V_{DD} = 5.25 V	–	18	20	mA
Supply Current†	I_{DD}	Reset	V_{DD} = 5.25 V	–	39	43	mA

† These supply current parameters are measured through V_{DD} pins to the ICS1892. The supply current parameters exclude external transformer currents.

10.4.2 DC Operating Characteristics for TTL Inputs and Outputs

Table 10-5 lists the DC operating characteristics of the ICS1892 TTL inputs and outputs.

Note: All V_{DD} measurements are taken with respect to V_{SS} (which equals 0 V).

Table 10-5. DC Operating Characteristics for TTL Inputs and Outputs

Parameter	Symbol	Conditions		Min.	Max.	Units
TTL Input High Voltage	V_{IH}	V_{DD} = 5.25 V	–	2.0	–	V
TTL Input Low Voltage	V_{IL}	V_{DD} = 5.25 V	–	–	0.8	V
TTL Output High Voltage	V_{OH}	V_{DD} = 4.75 V	I_{OH} = –4 mA	2.4	–	V
TTL Output Low Voltage	V_{OL}	V_{DD} = 4.75 V	I_{OL} = +4 mA	–	0.4	V
TTL Driving CMOS, Output High Voltage	V_{OH}	V_{DD} = 4.75 V	I_{OH} = –4 mA	3.68	–	V
TTL Driving CMOS, Output Low Voltage	V_{OL}	V_{DD} = 4.75 V	I_{OL} = +4 mA	–	0.4	V

10.4.3 DC Operating Characteristics for REF_IN

Table 10-6 lists the DC characteristics for the REF_IN pin.

Note: The REF_IN input switch point is 50% of V_{DD}.

Table 10-6. DC Operating Characteristics for REF_IN

Parameter	Symbol	Test Conditions		Min.	Max.	Units
Input High Voltage	V_{IH}	V_{DD} = 5.25 V	V_{SS} = 0 V	3.5	–	V
Input Low Voltage	V_{IL}	V_{DD} = 5.25 V	V_{SS} = 0 V	–	1.5	V

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10.4.4 DC Operating Characteristics for Media Independent Interface

Table 10-7 lists DC operating characteristics for the Media Independent Interface (MII) for the ICS1892.

Table 10-7. DC Operating Characteristics for Media Independent Interface

Parameter	Minimum	Typical	Maximum	Units
MII Input Pin Capacitance	–	8	–	pF
MII Output Pin Capacitance	–	14	–	pF
MII Output Drive Pin Impedance	–	38	–	Ω

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10.5 Timing Diagrams

10.5.1 Timing for Clock Reference In (REF_IN) Pin

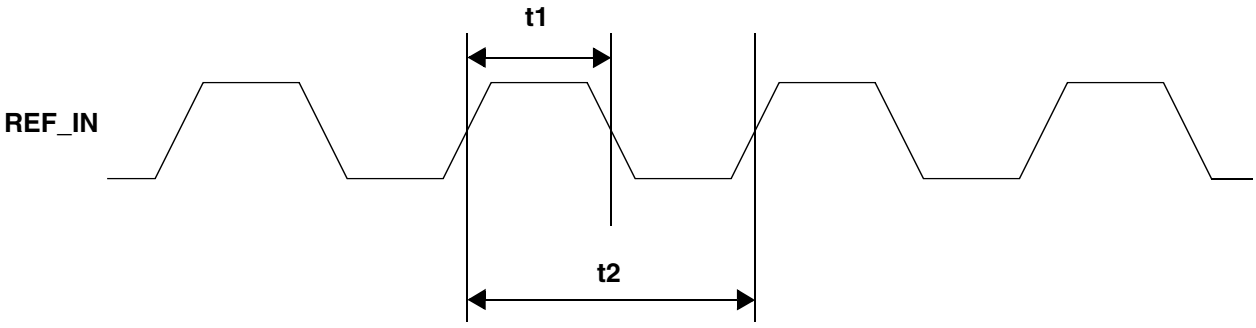
Table 10-8 lists the significant time periods for signals on the clock reference in (REF_IN) pin. Figure 10-1 shows the timing diagram for the time periods.

Note: The REF_IN switching point is 50% of V_{DD}.

Table 10-8. REF_IN Timing

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	REF_IN Duty Cycle	–	45	50	55	%
t2	REF_IN Period	–	–	40	–	ns

Figure 10-1. REF_IN Timing Diagram



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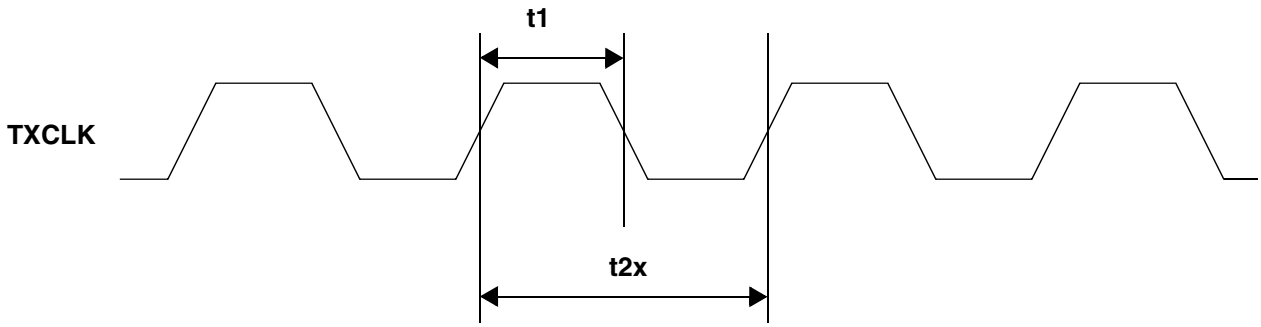
10.5.2 Timing for Transmit Clock (TXCLK) Pin

Table 10-9 lists the significant time periods for signals on the Transmit Clock (TXCLK) pin for the various interfaces. Figure 10-2 shows the timing diagram for the time periods.

Table 10-9. Transmit Clock Timing

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	TXCLK Duty Cycle	–	35	50	65	%
t2a	TXCLK Period	100M MII (100Base-TX)	–	40	–	ns
t2b	TXCLK Period	10M MII (10Base-T)	–	400	–	ns
t2c	TXCLK Period	100M Symbol Interface (100Base-TX)	–	40	–	ns
t2d	TXCLK Period	10M Symbol Interface (10Base-T)	–	100	–	ns

Figure 10-2. Transmit Clock Timing Diagram



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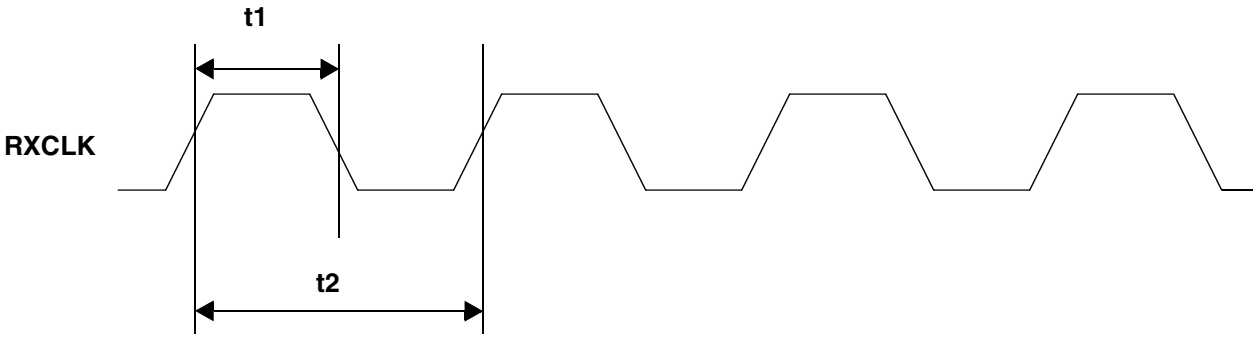
10.5.3 Timing for Receive Clock (RXCLK) Pin

Table 10-10 lists the significant time periods for signals on the Receive Clock (RXCLK) pin for the various interfaces. Figure 10-3 shows the timing diagram for the time periods.

Table 10-10. MII Receive Clock Timing

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	RXCLK Duty Cycle	–	35	50	65	%
t2a	RXCLK Period	100M MII (100Base-TX)	–	40	–	ns
t2b	RXCLK Period	10M MII (10Base-T)	–	400	–	ns
t2c	RXCLK Period	100M Symbol Interface (100Base-TX)	–	40	–	ns
t2d	RXCLK Period	10M Symbol Interface (10Base-T)	–	100	–	ns

Figure 10-3. Receive Clock Timing Diagram



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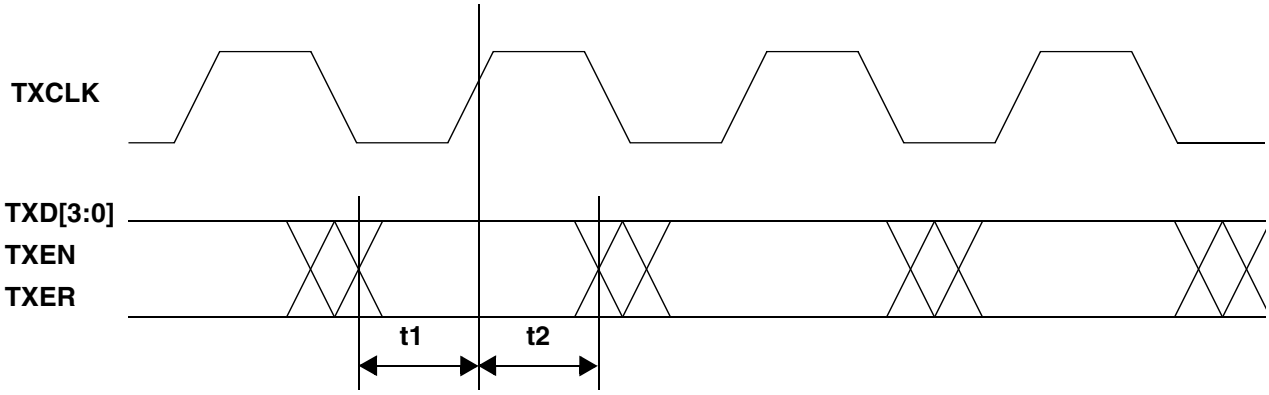
10.5.4 100M MII / 100M Stream Interface: Synchronous Transmit Timing

Table 10-11 lists the significant time periods for the 100M MII / 100M Stream Interface synchronous transmit timing (which consists of timings of signals on the TXD[3:0], TXEN, TXER, and TXCLK pins). Figure 10-4 shows the timing diagram for the time periods.

Table 10-11. 100M MII / 100M Stream Interface: Synchronous Transmit Timing

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	TXD[3:0], TXEN, TXER Setup to TXCLK Rise	–	15	–	–	ns
t2	TXD[3:0], TXEN, TXER Hold after TXCLK Rise	–	0	–	–	ns

Figure 10-4. 100M MII / 100M Stream Interface Synchronous Transmit Timing Diagram



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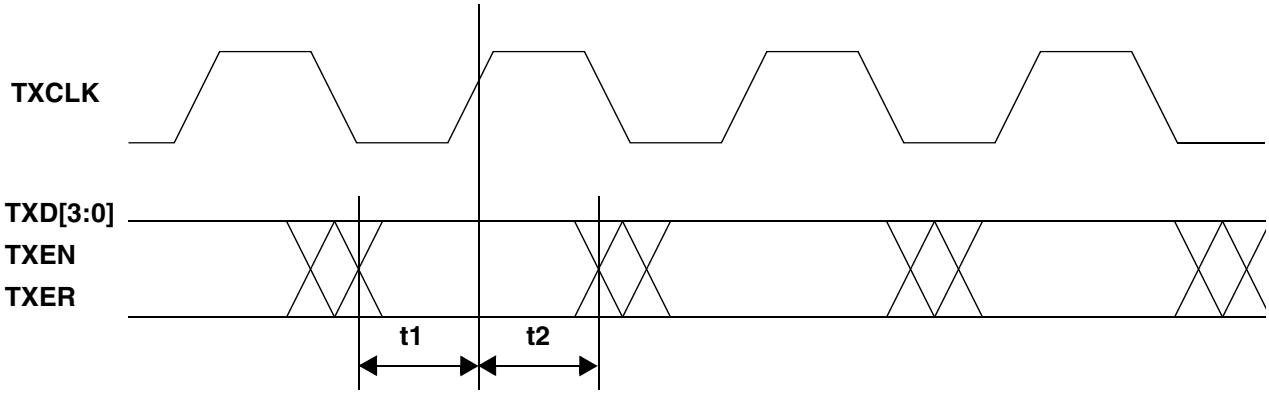
10.5.5 10M MII: Synchronous Transmit Timing

Table 10-12 lists the significant time periods for the 10M MII synchronous transmit timing (which consists of timings of signals on the TXD[3:0], TXEN, TXER, and TXCLK pins). Figure 10-5 shows the timing diagram for the time periods.

Table 10-12. 10M MII: Synchronous Transmit Timing

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	TXD[3:0], TXEN, TXER Setup to TXCLK Rise	–	375	–	–	ns
t2	TXD[3:0], TXEN, TXER Hold after TXCLK Rise	–	0	–	–	ns

Figure 10-5. 10M MII Synchronous Transmit Timing Diagram



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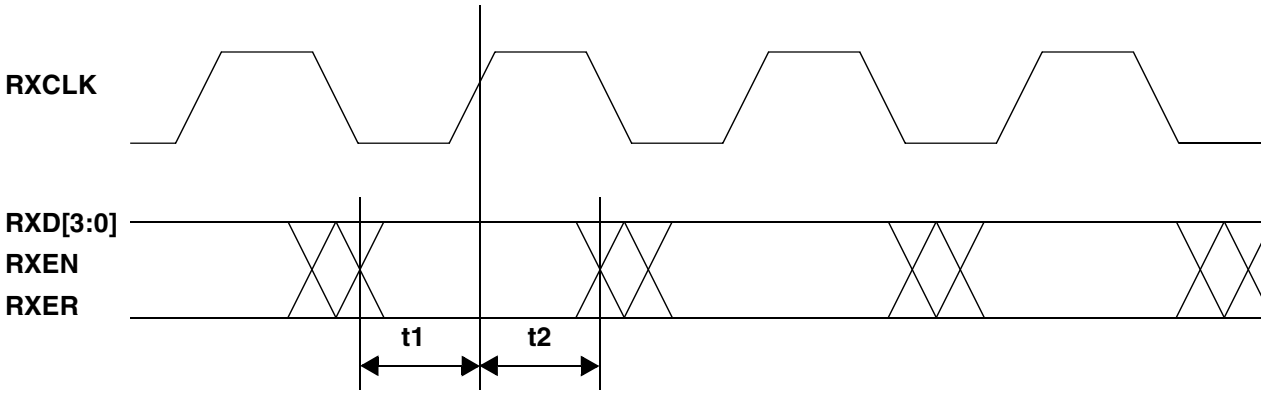
10.5.6 MII / 100M Stream Interface: Synchronous Receive Timing

Table 10-13 lists the significant time periods for the MII / 100M Stream Interface synchronous receive timing (which consists of timings of signals on the RXD[3:0], RXDV, RXER, and RXCLK pins). Figure 10-6 shows the timing diagram for the time periods.

Table 10-13. MII / 100M Stream Interface: Synchronous Receive Timing

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	RXD[3:0], RXDV, RXER Setup to RXCLK Rise	–	10.0	–	–	ns
t2	RXD[3:0], RXDV, RXER Hold after RXCLK Rise	–	10.0	–	–	ns

Figure 10-6. MII / 100M Stream Interface Synchronous Receive Timing Diagram



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10.5.7 MII Management Interface Timing

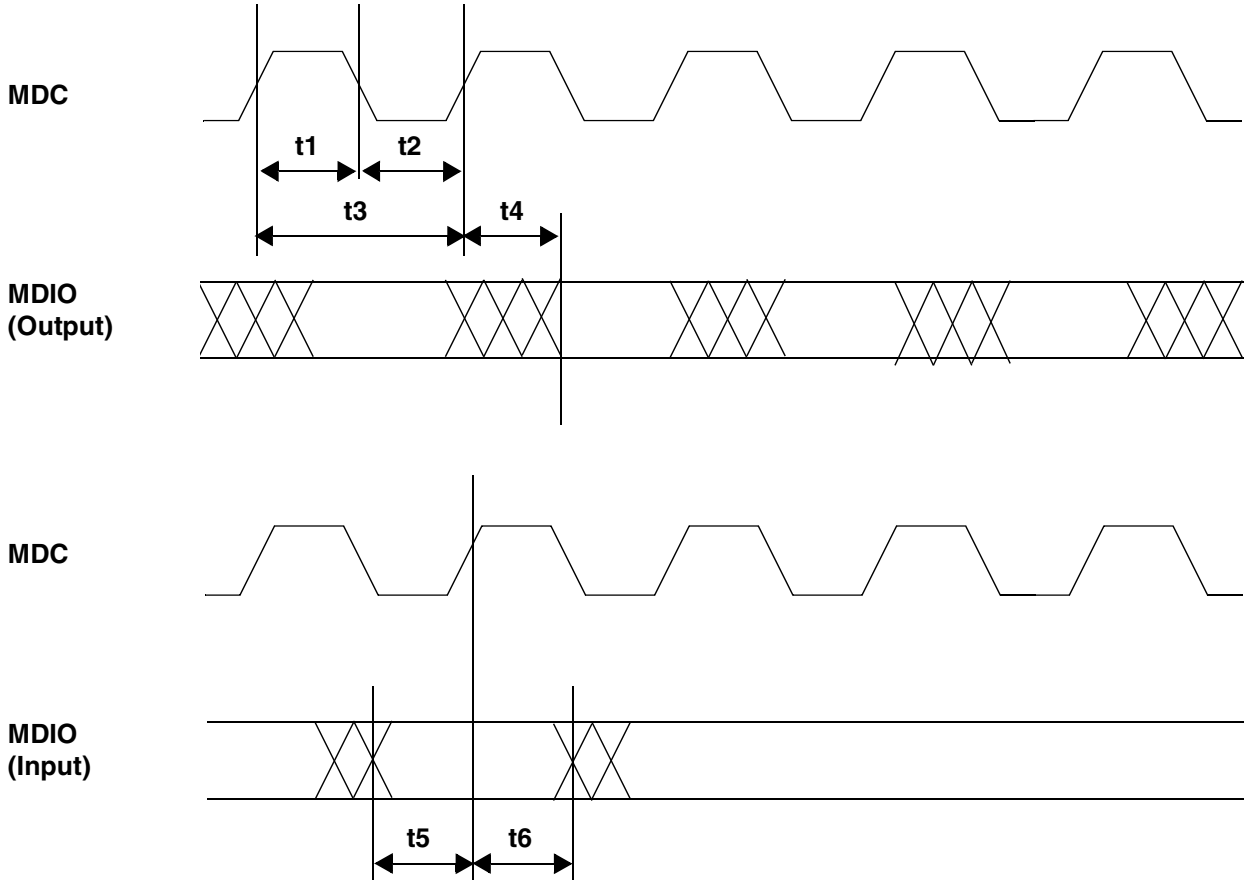
Table 10-14 lists the significant time periods for the MII Management Interface timing (which consists of timings of signals on the MDC and MDIO pins). Figure 10-7 shows the timing diagram for the time periods.

Table 10-14. MII Management Interface Timing

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	MDC Minimum High Time	–	160	–	–	ns
t2	MDC Minimum Low Time	–	160	–	–	ns
t3	MDC Period	–	400†	†	–	ns
t4	MDC Rise Time to MDIO Valid	–	0	–	300	ns
t5	MDIO Setup Time to MDC	–	10	–	–	ns
t6	MDIO Hold Time after MDC	–	10	–	–	ns

† All ICS1892 parts are tested at 25 MHz (a 40-ns period) with a 50-pF load. Designs must account for all board loading of MDC.

Figure 10-7. MII Management Interface Timing Diagram



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10.5.8 10M Serial Interface: Receive Latency

Table 10-15 lists the significant time periods for the 10M Serial Interface timing (which consists of timings of signals on the following pins:

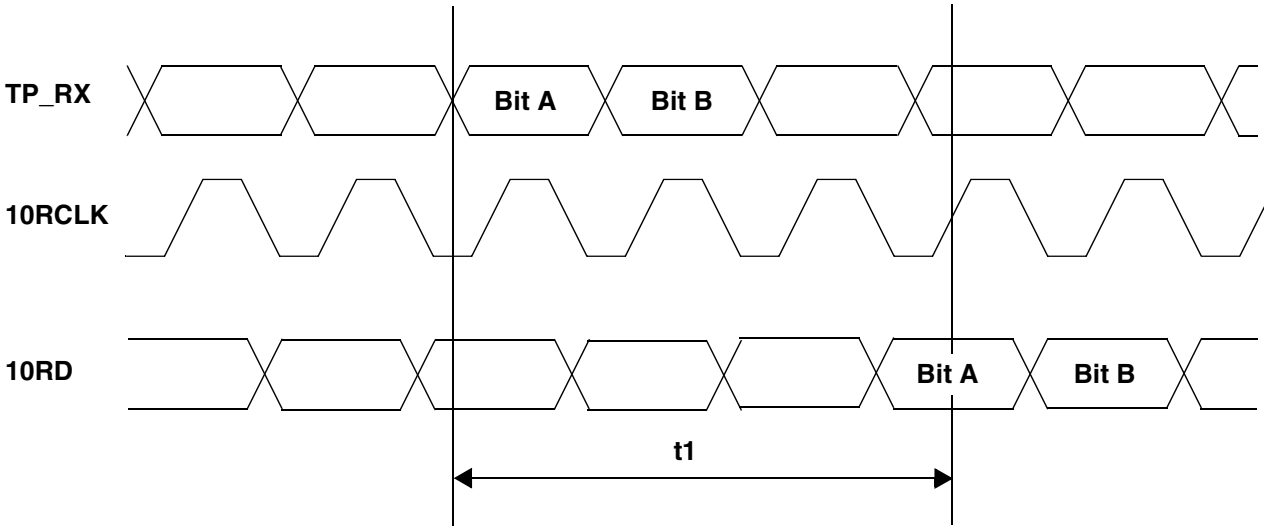
- TP_RX (the MDI mapping of the 10M/100M MII TP_RXP and TP_RXN pins)
- 10RCLK (the 10M Serial Interface mapping of the 10M/100M MII RXCLK pin)
- 10RD (the 10M Serial Interface mapping of the 10M/100M MII RD0 pin)

Figure 10-8 shows the timing diagram for the time periods.

Table 10-15. 10M Serial Interface Receive Latency Timing

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	TP_RX Input to 10RD Delay	10M Serial Interface	–	–	5	Bit times

Figure 10-8. 10M Serial Interface Receive Latency Timing



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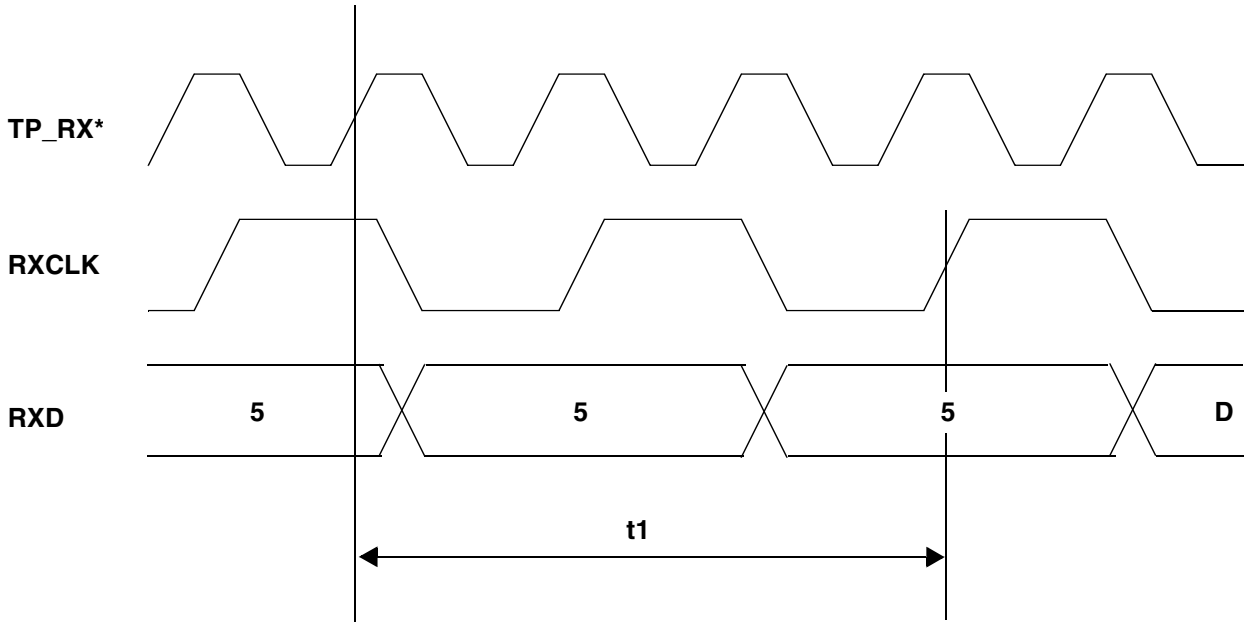
10.5.9 10M Media Independent Interface: Receive Latency

Table 10-16 lists the significant time periods for the 10M MII timing (which consists of timings of signals on the following pins: TP_RX (that is, the MII TP_RXP and TP_RXN pins), RXCLK, and RXD. Figure 10-9 shows the timing diagram for the time periods.

Table 10-16.

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	First Bit of /5/ on TP_RX to /5/D/ on RXD	10M MII	–	7.7	9	Bit times

Figure 10-9. 10M MII Receive Latency Timing Diagram



***Manchester encoding not shown.**

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10.5.10 10M Serial Interface: Transmit Latency

Table 10-17 lists the significant time periods for the 10M Serial Interface transmit latency. The time periods consist of timings of signals on the following pins:

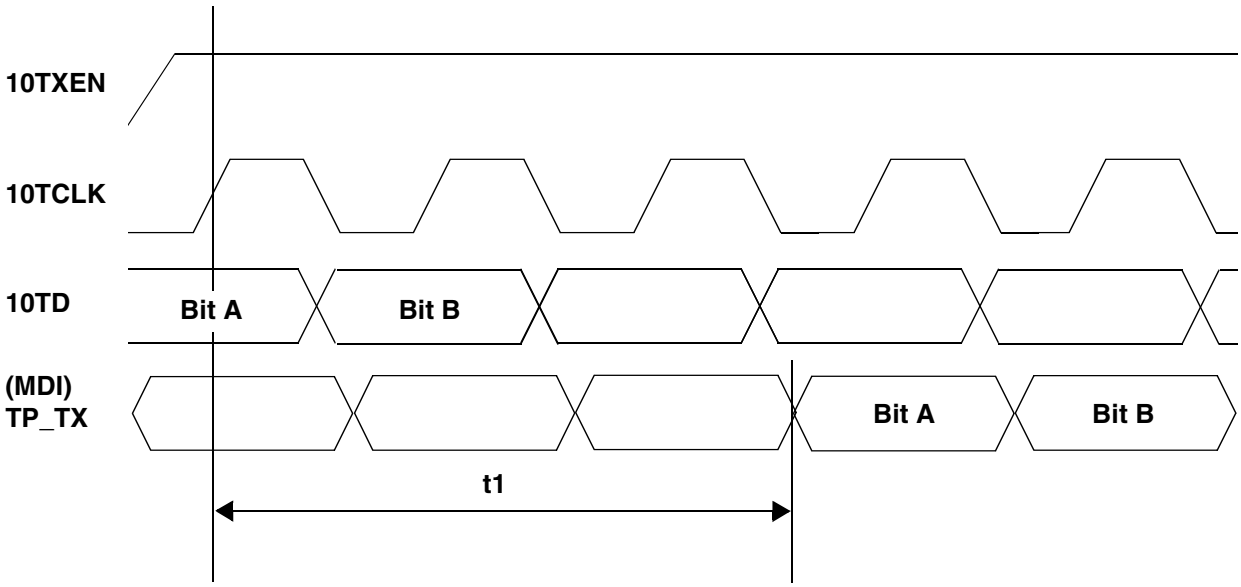
- 10TXEN (the 10M Serial Interface mapping of the 10M/100M MII TXEN pin)
- 10TCLK (the 10M Serial Interface mapping of the 10M/100M MII TXCLK pin)
- 10TD (the 10M Serial Interface mapping of the 10M/100M MII TXD0 pin)
- TP_TX (the MDI mapping of the 10M/100M MII TP_TXP and TP_TXN pins)

Figure 10-10 shows the timing diagram for the time periods.

Table 10-17. 10M Serial Interface Transmit Latency Timing

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	10TD Into TP_TX Out Delay	10M Serial Interface	–	–	2	Bit times

Figure 10-10. 10M Serial Interface Transmit Latency Timing Diagram



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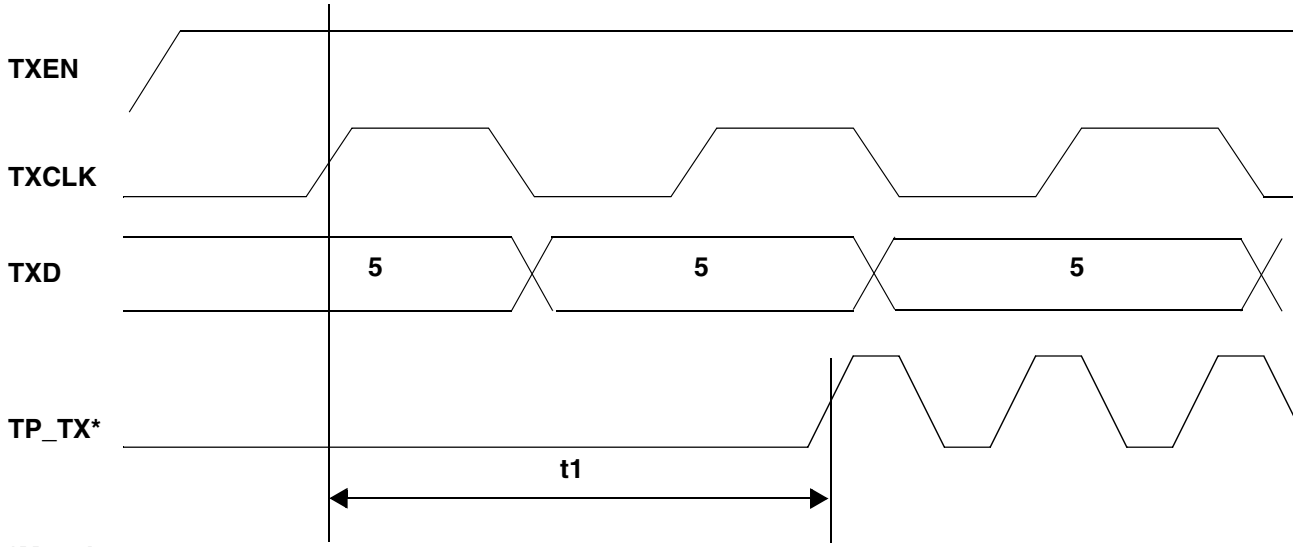
10.5.11 10M Media Independent Interface: Transmit Latency

Table 10-18 lists the significant time periods for the 10M MII transmit latency. The time periods consist of timings of signals on the following pins: TXEN, TXCLK, TXD (that is, TXD[3:0]), and TP_TX (that is, the TP_TXP and TP_TXN pins). Figure 10-11 shows the timing diagram for the time periods.

Table 10-18. 10M MII Transmit Latency Timing

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	TXD Sampled to MDI Output of First Bit	10M MII	–	1.2	2	Bit times

Figure 10-11. 10M MII Transmit Latency Timing Diagram



***Manchester encoding not shown.**

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10.5.12 MII / 100M Stream Interface: Transmit Latency

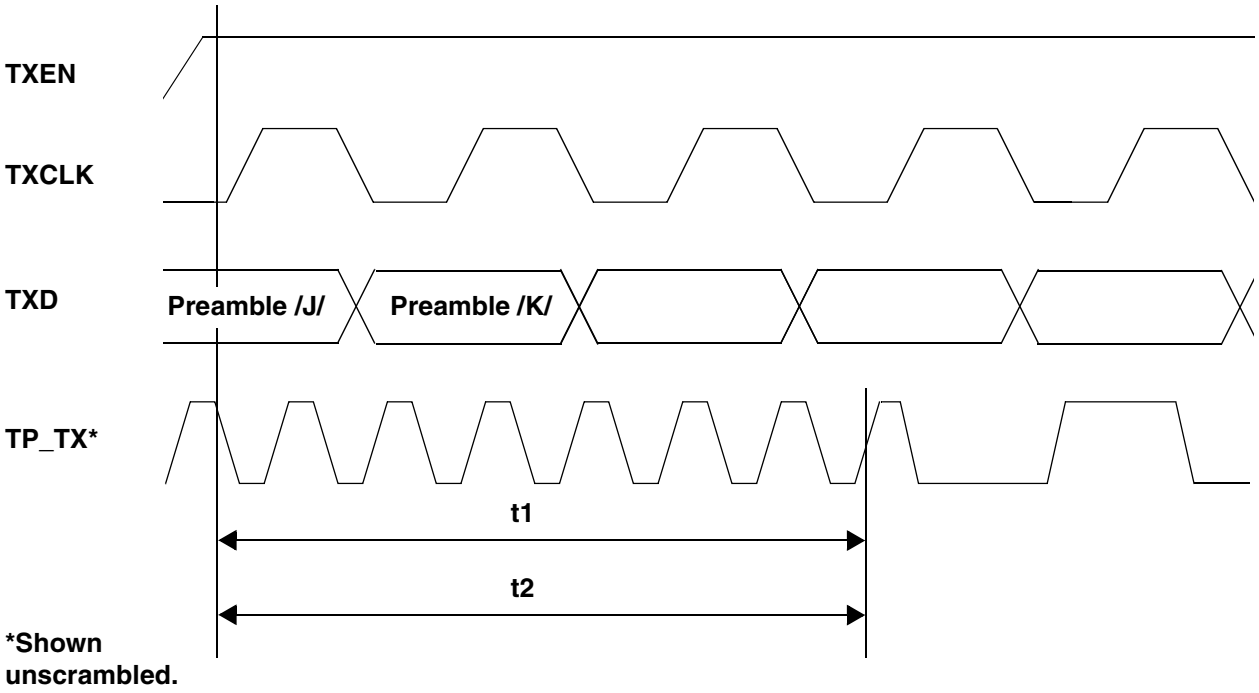
Table 10-19 lists the significant time periods for the MII / 100 Stream Interface transmit latency. The time periods consist of timings of signals on the following pins: TXEN, TXCLK, TXD (that is, TXD[3:0]), and TP_TX (that is, the TP_TXP and TP_TXN pins). Figure 10-12 shows the timing diagram for the time periods.

Table 10-19. MII / 100M Stream Interface Transmit Latency

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	TXEN Sampled to MDI Output of First Bit of /J/ †	MII	–	4	4	Bit times
t2	TXD Sampled to MDI Output of First Bit	100M Stream Interface	–	4	4	Bit times

† The IEEE maximum is 18 bit times.

Figure 10-12. MII / 100M Stream Interface Transmit Latency Timing Diagram



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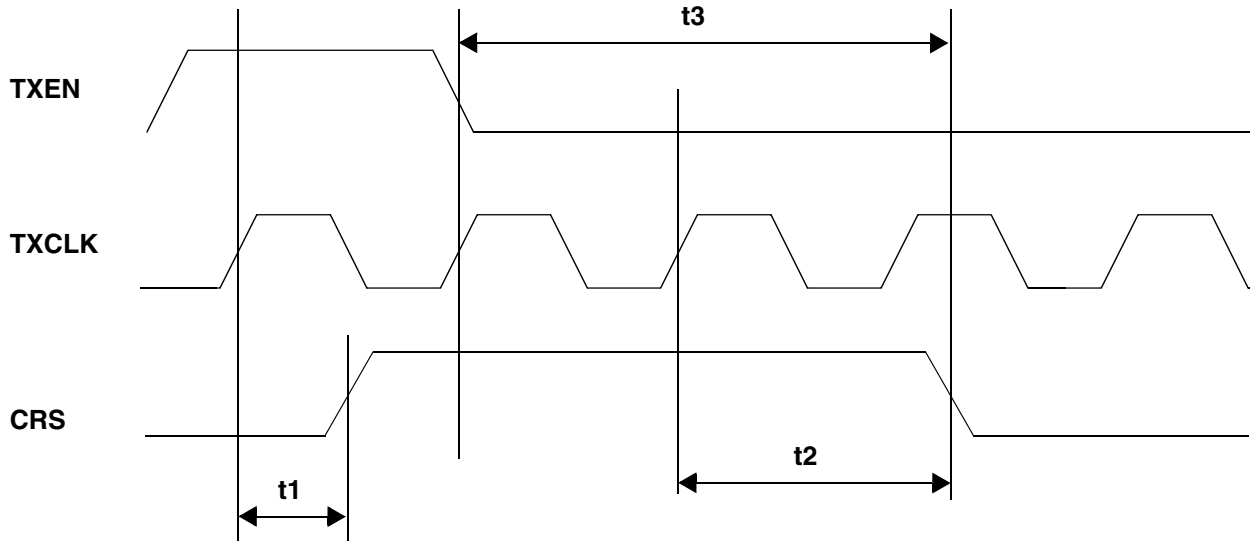
10.5.13 MII: Carrier Assertion/De-Assertion (Half-Duplex Transmission)

Table 10-20 lists the significant time periods for the MII carrier assertion/de-assertion during half-duplex transmission. The time periods consist of timings of signals on the following pins: TXEN, TXCLK, and CRS. Figure 10-13 shows the timing diagram for the time periods.

Table 10-20. MII Carrier Assertion/De-Assertion (Half-Duplex Transmission Only)

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	TXEN Sampled Asserted to CRS Assert	–	–	< 1	1	Bit times
t2	TXEN Sampled De-Asserted to CRS De-Asserted	–	–	< 1	1	
t3	TXEN De-Asserted to CRS De-Asserted	–	–	–	4	

Figure 10-13. MII Carrier Assertion/De-Assertion Timing Diagram (Half-Duplex Transmission Only)



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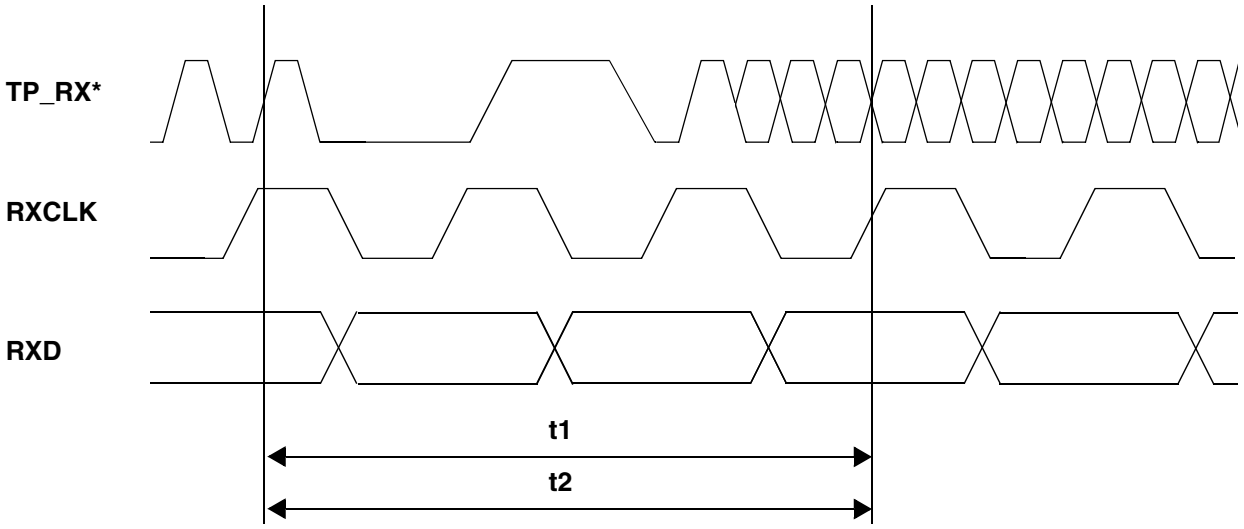
10.5.14 100M MII / 100M Stream Interface: Receive Latency

Table 10-21 lists the significant time periods for the 100M MII / 100M Stream Interface receive latency. The time periods consist of timings of signals on the following pins: TP_RX (that is, TP_RXP and TP_RXN), RXCLK, and RXD (that is, RXD[3:0]). Figure 10-14 shows the timing diagram for the time periods.

Table 10-21. 100M MII / 100M Stream Interface Receive Latency Timing

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	First Bit of /J/ into TP_RX to /J/ on RXD	100M MII	–	16.9	17	Bit times
t2	First Bit of /J/ into TP_RX to /J/ on RXD	100M Stream Interface	–	TBD	12.5	Bit times

Figure 10-14. 100M MII / 100M Stream Interface: Receive Latency Timing Diagram



***Shown unscrambled.**

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10.5.15 Media Dependent Interface: Input-to-Carrier Assertion/De-Assertion

Table 10-22 lists the significant time periods for the MDI input-to-carrier assertion/de-assertion. The time periods consist of timings of signals on the following pins: CRS, COL, and TP_RX (that is, the TP_RXP and TP_RXN pins). Figure 10-15 shows the timing diagram for the time periods.

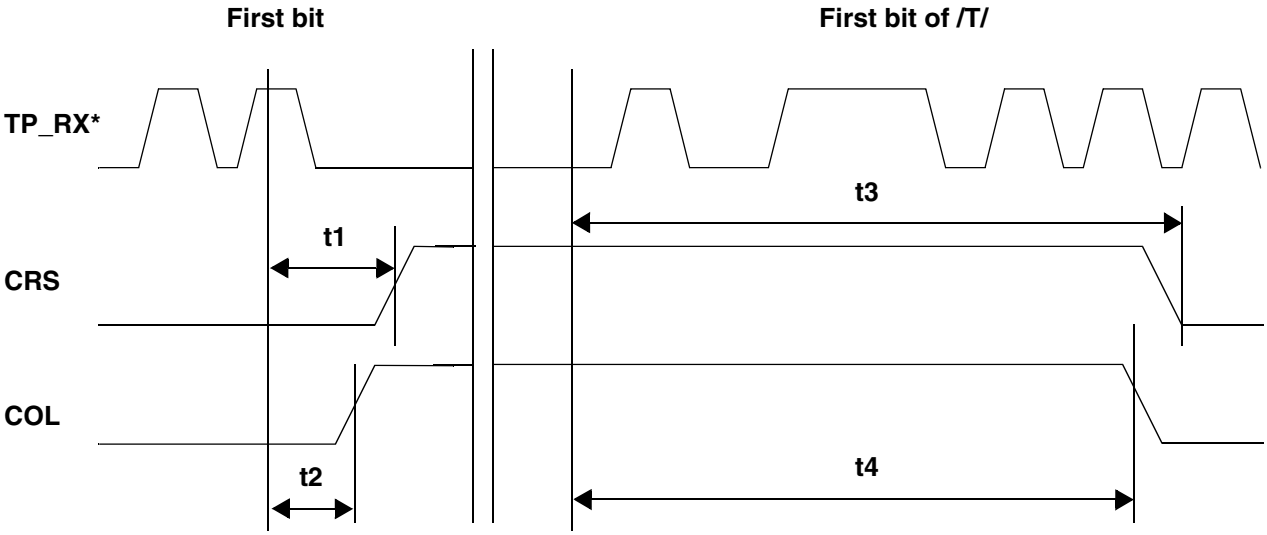
Table 10-22. MDI Input-to-Carrier Assertion/De-Assertion Timing

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	First Bit of /J/ into TP_RX to CRS Assert †	–	9	–	13	Bit times
t2	First Bit of /J/ into TP_RX while Transmitting Data to COL Assert †	Half-Duplex Mode	9	–	13	Bit times
t3	First Bit of /T/ into TP_RX to CRS De-Assert ‡	–	13	–	17	Bit times
t4	First Bit of /T/ Received into TP_RX to COL De-Assert ‡	Half-Duplex Mode	–	–	14	Bit times

† The IEEE maximum is 20 bit times.

‡ The IEEE minimum is 13 bit times, and the maximum is 24 bit times.

Figure 10-15. MDI Input to Carrier Assertion / De-Assertion Timing Diagram



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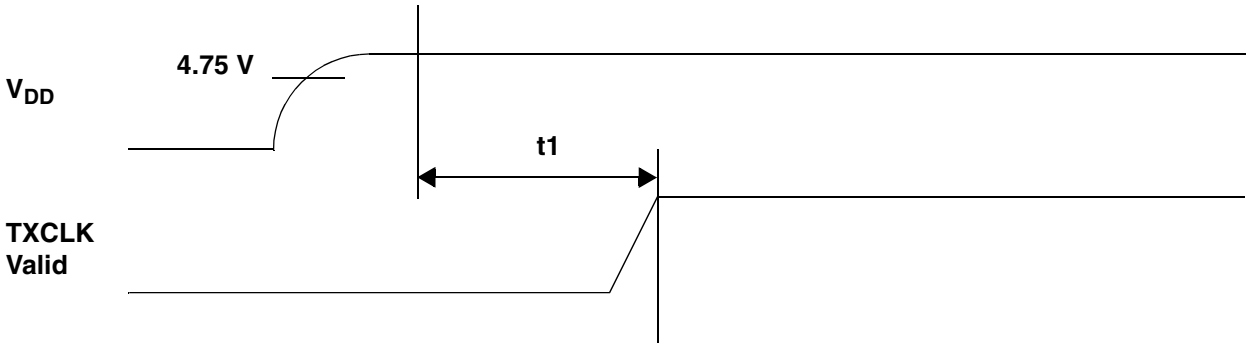
10.5.16 Reset: Power-On Reset

Table 10-23 lists the significant time periods for the power-on reset (which consists of timings of signals on the V_{DD} and TXCLK pins). Figure 10-16 shows the timing diagram for the time periods.

Table 10-23. Power-On Reset Timing

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	$V_{DD} \geq 4.75$ V to Reset Complete	–	109	–	200	ms

Figure 10-16. Power-On Reset Timing Diagram



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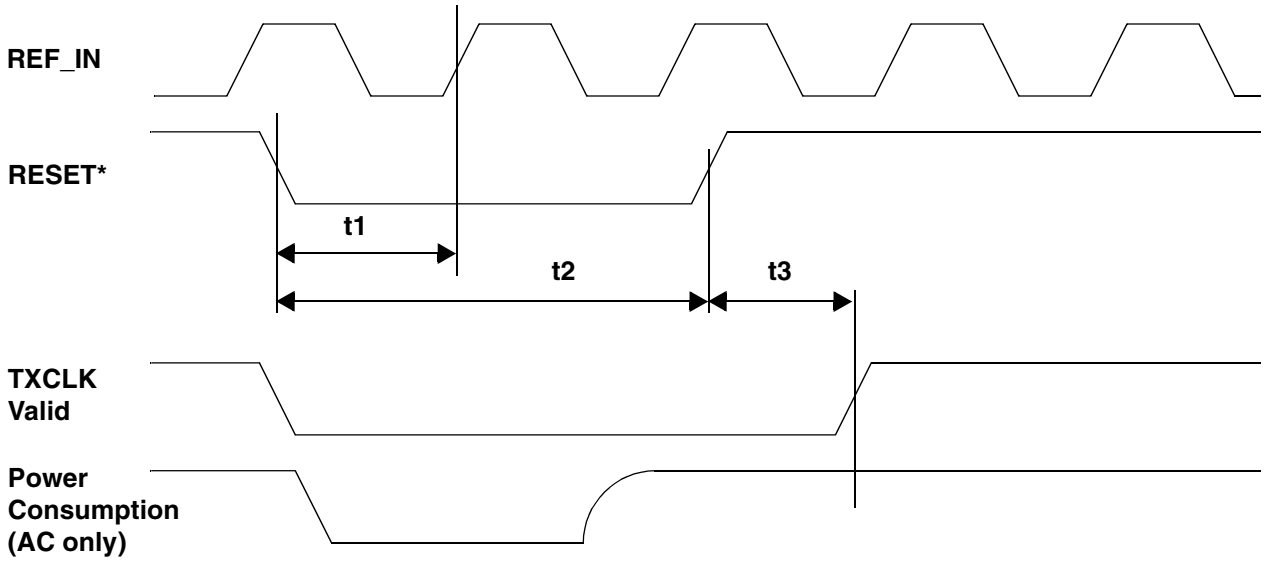
10.5.17 Reset: Hardware Reset and Power-Down

Table 10-24 lists the significant time periods for the hardware reset and power-down reset (which consists of timings of signals on the REF_IN, RESET*, and TXCLK pins). Figure 10-17 shows the timing diagram for the time periods.

Table 10-24. Hardware Reset and Power-Down Timing

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	RESET* Active to Device Isolation and Initialization	–	–	65	–	ns
t2	Minimum RESET* Pulse Width	–	200	–	–	ns
t3	RESET* Released to TXCLK Valid	–	–	53	200	ms

Figure 10-17. Hardware Reset and Power-Down Timing Diagram



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10.5.18 10Base-T: Heartbeat Timing (SQE)

Table 10-25 lists the significant time periods for the 10Base-T heartbeat (that is, the Signal Quality Error, which consists of timings of signals on the TXEN, TXCLK, and COL pins). Figure 10-18 shows the timing diagram for the time periods.

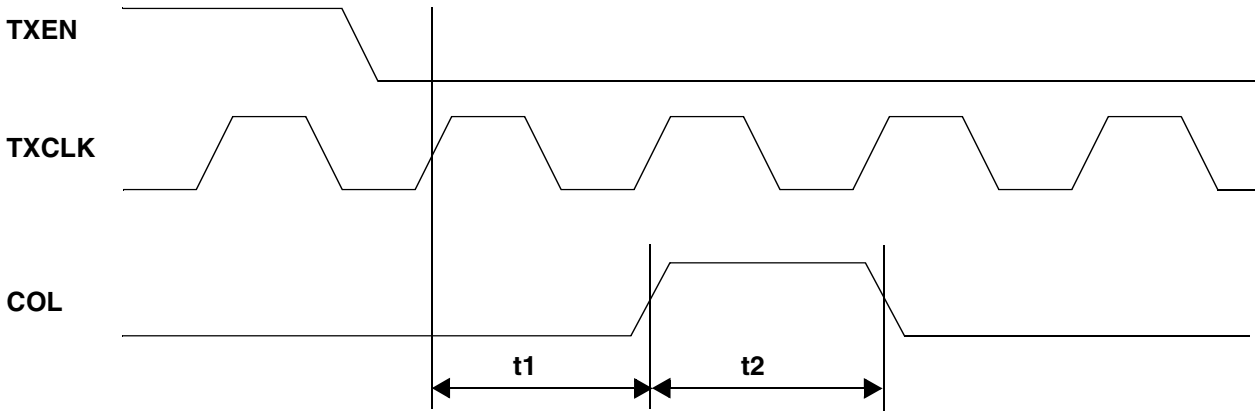
Note:

1. For more information on 10Base-T SQE operations, see Section 7.5.10, "10Base-T Operation: SQE Test".
2. In 10Base-T mode, one bit time = 100 ns.

Table 10-25. 10Base-T Heartbeat (SQE) Timing

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	COL Heartbeat Assertion Delay from TXEN De-Assertion	10Base-T Half Duplex	–	840	1600	ns
t2	COL Heartbeat Assertion Duration	10Base-T Half Duplex	–	1000	1500	ns

Figure 10-18. 10Base-T Heartbeat (SQE) Timing Diagram



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10.5.19 10Base-T: Jabber Timing

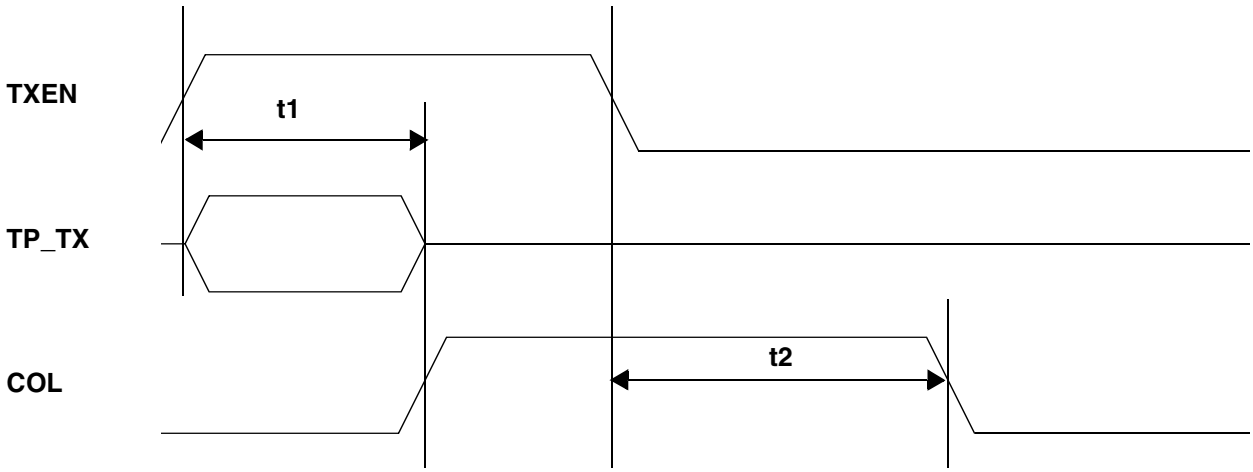
Table 10-26 lists the significant time periods for the 10Base-T jabber. The time periods consist of timings of signals on the following pins: TXEN, COL, and TP_TX (that is, the TP_TXP and TP_TXN pins). Figure 10-19 shows the timing diagram for the time periods.

Note: For more information on 10Base-T jabber operations, see Section 7.5.9, "10Base-T Operation: Jabber".

Table 10-26. 10Base-T Jabber Timing

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	Jabber Activation Time	10Base-T Half Duplex	21	21	31	ms
t2	Jabber De-Activation Time	10Base-T Half Duplex	315	324	325	ms

Figure 10-19. 10Base-T Jabber Timing Diagram



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10.5.20 10Base-T: Normal Link Pulse Timing

Table 10-27 lists the significant time periods for the 10Base-T Normal Link Pulse (which consists of timings of signals on the TP_TXP pin). Figure 10-20 shows the timing diagram for the time periods.

Table 10-27. 10Base-T Normal Link Pulse Timing

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	Normal Link Pulse Width	10Base-T	–	100	–	ns
t2	COL Heartbeat (SQE) Assertion Duration	10Base-T Half Duplex	8	18	24	ms

Figure 10-20. 10Base-T Normal Link Pulse Timing Diagram



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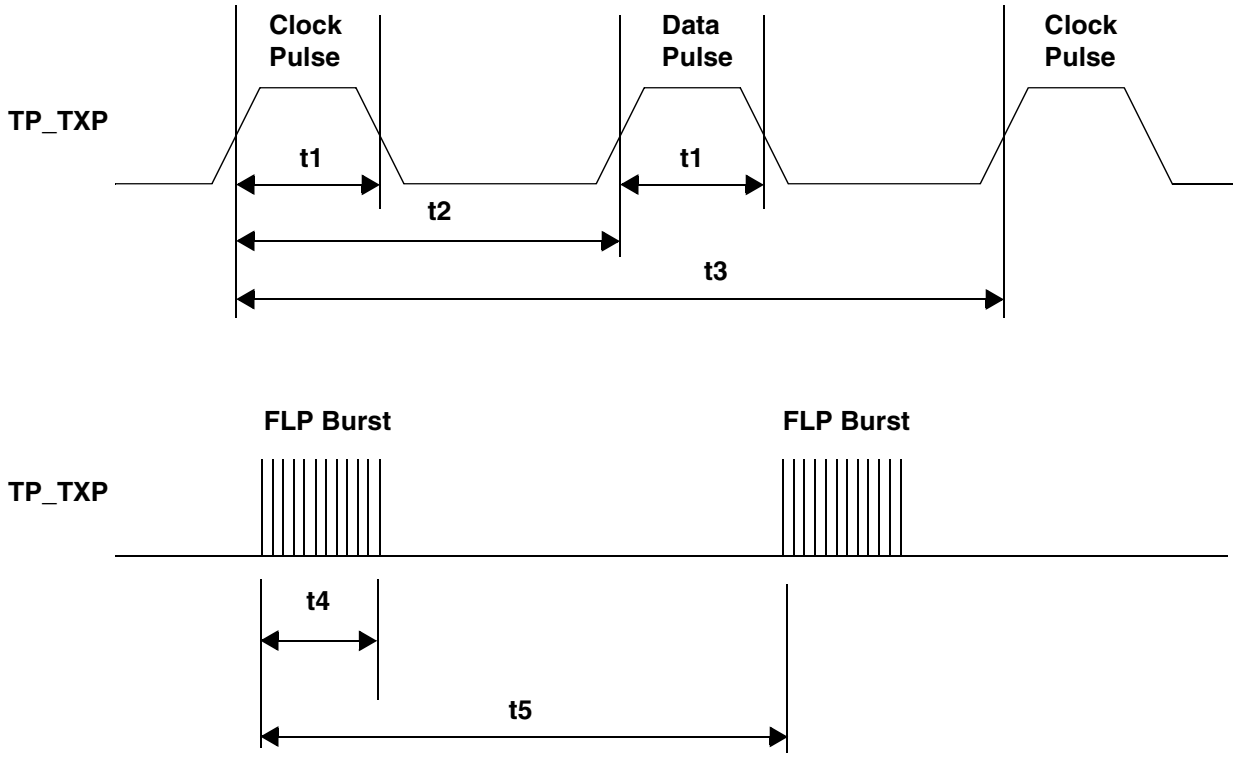
10.5.21 Auto-Negotiation Fast Link Pulse Timing

Table 10-28 lists the significant time periods for the ICS1892 Auto-Negotiation Fast Link Pulse (which consists of timings of signals on the TP_TXP and TP_TXN pins). Figure 10-21 shows the timing diagram for the time periods.

Table 10-28. Auto-Negotiation Fast Link Pulse Timing

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	Clock/Data Pulse Width	–	–	100	–	ns
t2	Clock Pulse-to-Data Pulse Timing	–	55.5	62.5	69.5	µs
t3	Clock Pulse-to-Clock Pulse Timing	–	111	125	139	µs
t4	FLP Burst Width	–	–	2	–	ms
t5	FLP Burst to FLP Burst	–	8	16.8	24	ms
t6	Number of Clock/Data Pulses in a Burst	–	17	–	33	pulses

Figure 10-21. Auto-Negotiation Fast Link Pulse Timing Diagram



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Chapter 11 Physical Dimensions of ICS1892 Package

This section gives the physical dimensions for the various ICS1892 packages.

- The lead count (N) for all packages is 64 leads.
- The nominal footprint (that is the body) for all packages is 2.0 mm.

Table 11-1 lists the ICS1892 physical dimensions, which are shown in Figure 11-1.

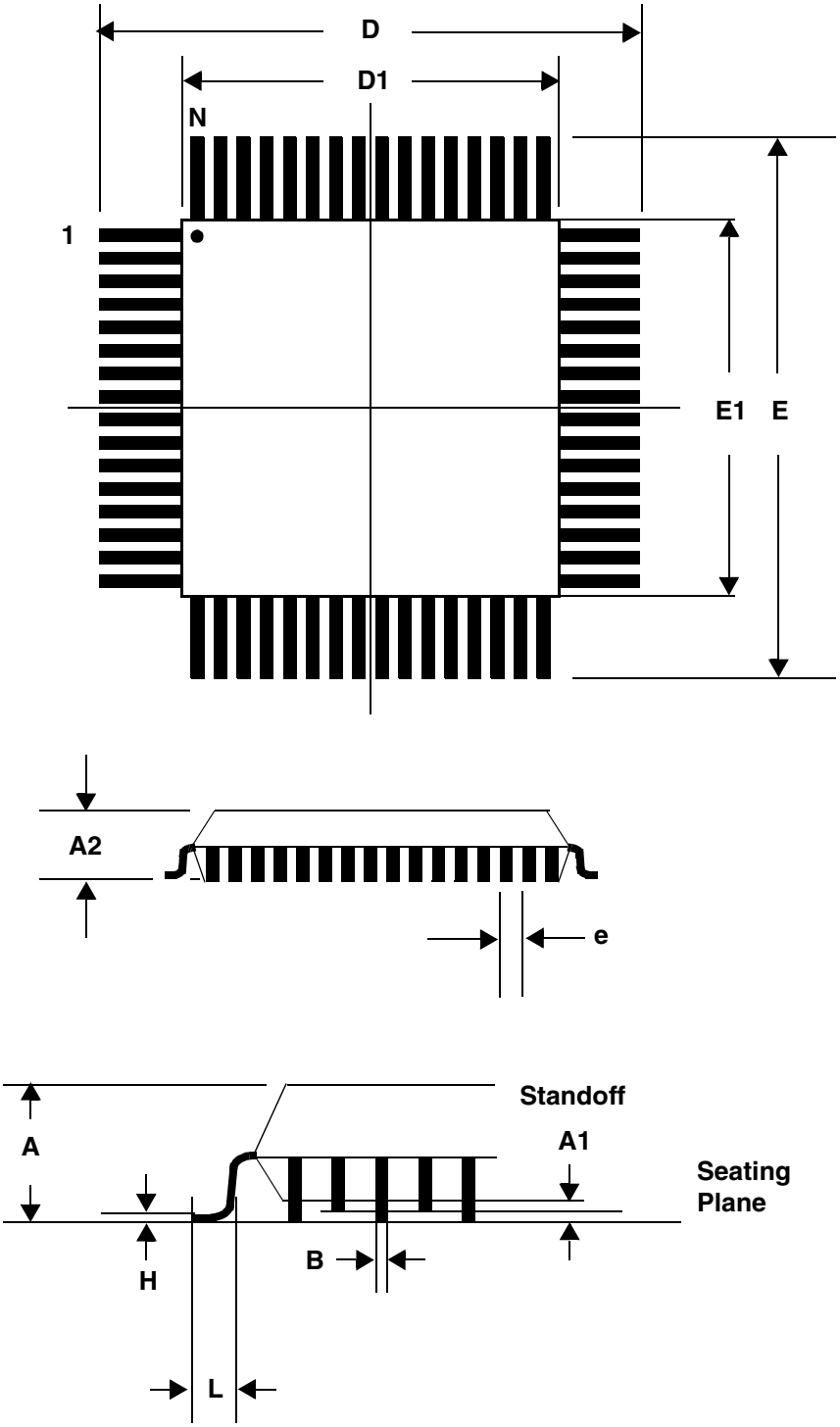
Table 11-1. ICS1892 Physical Dimensions

Dimension		Chip					
		ICS1892Y (MQFP)		ICS1892Y-10 (LQFP)		ICS1892Y-14 (LQFP)	
Symbol	Description	Nominal (mm)	Tolerance (mm)	Nominal (mm)	Tolerance (mm)	Nominal (mm)	Tolerance (mm)
A	Full Package Height	3.00	Maximum	1.60	Maximum	1.60	Maximum
A1	Package Standoff	0.25	Maximum	0.15	Maximum	0.15	Maximum
A2	Package Thickness	2.7	+0.10 / -0.05	1.4	±0.05	1.4	±0.05
B	Lead Width with Plate	0.35	+0.10 / -0.05	0.22	+0.05 / -0.05	0.37	+0.08 / -0.05
D	Tip-to-Tip Width	17.20	±0.25	12.0	Basic	16.0	Basic
D1	Body Width	14.00	±0.10	10.0	Basic	14.0	Basic
E	Tip-to-Tip Width	17.20	±0.25	12.0	Basic	16.0	Basic
E1	Body Width	14.00	±0.10	10.0	Basic	14.0	Basic
e	Lead Pitch	0.80	Basic	0.50	Basic	0.80	Basic
H	Lead Height with Plate	0.23	Maximum	.16	+0.04 / -0.07	.16	+0.04 / -0.07
L	Foot Length	0.88	±0.15	0.60	±0.15	0.60	±0.15

Note: The ICS1892Y-10 (LQFP) package does not have the heat disapation ability of the ICS1892Y or ICS1892Y-14. Special application is required to use this package.

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Figure 11-1. ICS1892 Physical Dimensions



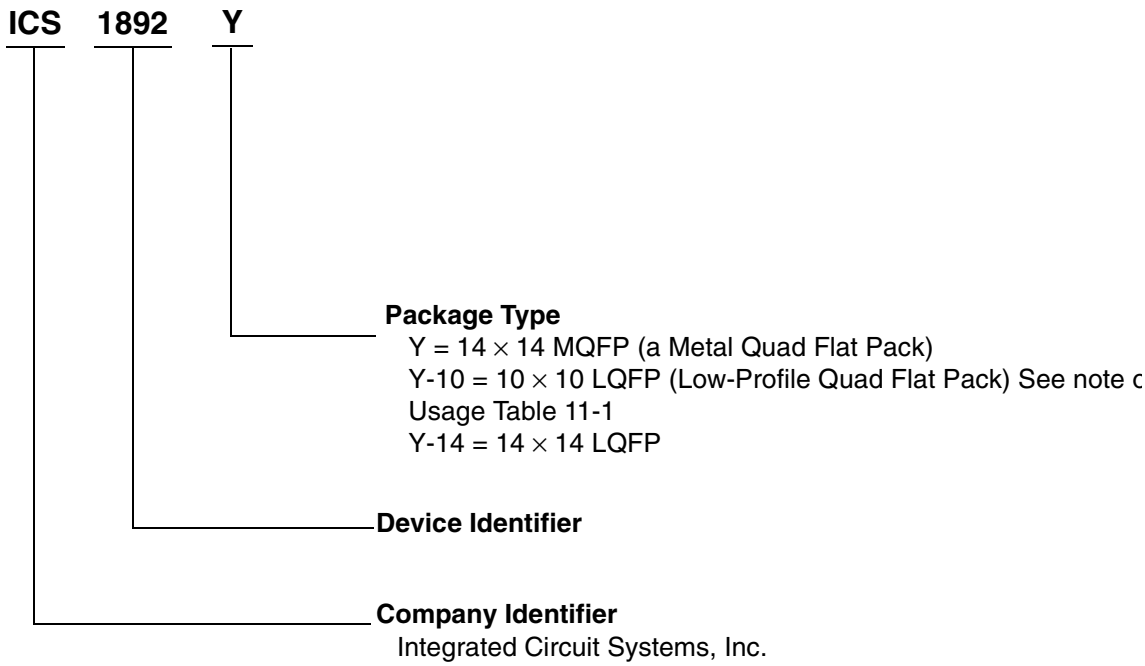
ICS reserves the right to make changes in the device data identified in this publication without further notice. ICS advises its customers to obtain the latest version of all device data to verify that any information being relied upon by the customer is current and accurate.

Chapter 12 Ordering Information

Figure 12-1 shows ordering information for the ICS1892 packages, which include the following:

- ICS1892Y
- ICS1892Y-10
- ICS1892Y-14

Figure 12-1. ICS1892 Ordering Information



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