iC-ML

HALL Position Sensor / Encoder

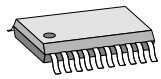
FEATURES

- Linear Hall sensor array for magnetic pole pitch of 2.56 mm
- Non-sensitive to magnetic stray fields due to differential measurement technique
- Interpolator with 8-bit linear resolution of 20 µm
- Linear speed up to 5 m/s
- Buffered I/O stages for signal outputs
- Configuration inputs for operating mode selection
- Analog operation modes:
  - sine/cosine signals controlled to 2 Vpp
  - triange or sawtooth signal with selectable amplitude
- Digital operation modes:
  - A/B quadrature signals with Z index pulse
  - Counter pulses for external binary counters
- Cascading of multiple iC-ML possible for chain operation (Evaluation of independent scales x, y, z)
- Error signal output for detection of low magnetic field strength
- Additional operating modes with reduced power consumption
- Standby modus when not enabled
- Extended temperature range of -40...+125 °C

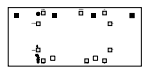
APPLICATIONS

- Analog and digital linear sensors
- Incremental linear encoders
- Pole wheel sensing
- Potentiometer replacement
- Contactless slider/switch
- Commutation of linear motor
- Absolute displacement sensing
- Liquid level meter

PACKAGES

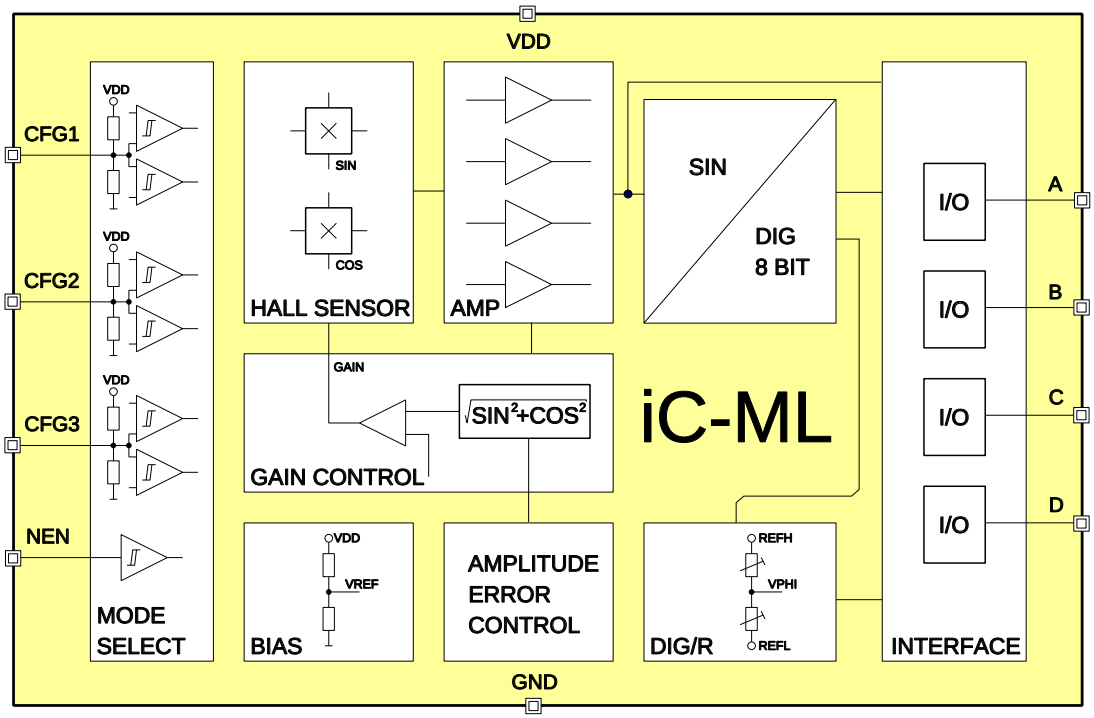


TSSOP20



Die-Size
4.4 mm x 1.9 mm

BLOCK DIAGRAM



Copyright © 2009 iC-Haus

DESCRIPTION

The CMOS device iC-ML consists of four hall sensors arranged in a line and optimized to read out magnetic tapes with 2.56 mm pole spacing. This sensor array permits error-tolerant adjustment of the magnetic tape, reducing assembly efforts. The integrated signal conditioning unit provides a differential sine/cosine signal at the output.

The sensor generates one sine/cosine cycle for each full magnetic periode of 5.12 mm, enabling the travelling distance to be clearly determined. At the same time the internal amplitude control unit produces an regulated output amplitude of 2 Vpp regardless of variations in the magnetic field strength, supply voltage and temperature. Furthermore, signals are provided which enable the sensor amplitude to be assessed and also report any magnetic tape loss.

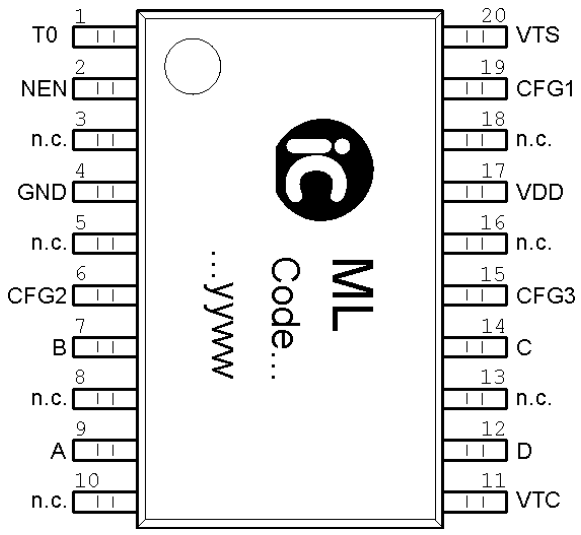
With the aid of the integrated 8-bit sine/digital converter the travelling distance within a magnetic periode is determined from the sine/cosine signals. This is output via an incremental interface in a number of selectable resolutions. The zero position of each periode is indicated by an index pulse. The maximum resolution of 8-bit is maintained up to travelling speeds of 5 m/s.

The absolute position within a magnetic periode can be converted back to a linear analog output signal using the internal D/A converter; here, output voltage limits can be set as required using the external pins. Either a periodic linear signal (sawtooth) or a delta voltage (triangle) can be provided. iC-ML can be easily cascaded in three different modes of chain operation so that several axes of transistion can be scanned. The linear positions of the individual axes can then be read via a common bus.

Used in conjunction with a magnetic tape iC-ML can act as an linear encoder system with an integrated magnetic scanning feature.

PACKAGES TSSOP20

PIN CONFIGURATION - *TSSOP20*



PIN FUNCTIONS

No.	Name	Function
1	T0	Test Pin (connect to GND)
2	NEN	Enable Input, low active
3	n.c.	
4	GND	Ground
5	n.c.	
6	CFG2	Configuration Input 2
7	B	Bidirectional Input/Output B
8	n.c.	
9	A	Bidirectional Input/Output A
10	n.c.	
11	VTC	Test Pin (do not connect)
12	D	Bidirectional Input/Output D
13	n.c.	
14	C	Bidirectional Input/Output C
15	CFG3	Configuration Input 3
16	n.c.	
17	VDD	+5 V Supply Voltage
18	n.c.	
19	CFG1	Configuration Input 1
20	VTS	Test Pin (do not connect)

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Supply voltage		-0.3	6	V
G002	V()	Voltages at A, B, C, D, NEN, CFG1, CFG2	V() < VDD + 0.3 V	-0.3	6	V
G003	Imx(VDD)	Current at VDD		-30	30	mA
G004	Imx(GND)	Current at GND		-30	30	mA
G005	Imx()	Current at A, B, C, D, NEN, CFG1, CFG2		-10	10	mA
G006	Ilu()	Pulse current (Latch-up immunity)	Pulse width < 10 µs	-100	100	mA
G007	Vd()	ESD-Voltage at all pins	HBM, 100 pF discharged over 1.5 kΩ		2	kV
G008	Ts	Storage temperature		-40	150	°C

THERMAL DATA

Operating conditions: VDD = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Ambient temperature		-40		125	°C
T02	Rthja	Thermal resistance chip/ambient	SMD assembly, no additional cooling areas			75	K/W

All voltages are referenced to ground unless otherwise stated.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 5 V ±10 % , Tj = -40 ... 125 °C, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	VDD	Supply voltage		4.5	5	5.5	V
002	I(VDD)	Supply current	open pins, normal operation open pins, power reduction mode (PRM)		14 7	20 10	mA mA
003	I(VDD)sb	Standby supply current	NEN = VDD			200	µA
004	td(VDD)on	Turn on delay	VDD > 4 V, see Fig. 9		10		µs
005	td(VDD)off	Turn off delay	VDD < 2.6 V		10		µs
Hall sensor array							
101	Hext	Requiered external magnetic field strength	at chip surface	20	50	100	kA/m
102	psens	Hall sensor array pitch	see Fig. 1		1.28		mm
103	ysens	Hall sensor array distance to center of die	see Fig. 1		0.7		mm
104	xdis	Lateral displacement of chip to package	in TSSOP20 package, see Fig. 2	-0.2		0.2	mm
105	ydis	Vertical displacement of chip to package	in TSSOP20 package, see Fig. 2	-0.2		0.2	mm
106	Φdis	Angular displacement of chip with reference to package	in TSSOP20 package, see Fig. 2	-3		3	DEG
107	hsens	Distance chip surface to top of package	in TSSOP20 package, see Fig. 2		400		µm
Signal conditioning							
201	Voff	Offset voltage	on output, with external magnetic field amplitude of 20 kA/m	-50		50	mV
202	TC(Voff)	Temperatur coefficient of offset voltage		-50		50	µV/K
203	Vdc	Output mean value		45	50	55	%VDD
204	Ratio	Amplitude ratio of SIN / COS		0.95	1.00	1.05	
205	fhc	Cut off frequency			20		kHz
206	t()settle	Settling time	to 70 % amplitude, Hext = 40 kA/m		80	150	µs
207	V()gain	Gain output voltage		0.05		4.0	V
208	V()ampl	Sine/Cosine amplitude	V()ampl = V()max - Vdc	0.9	1.0	1.1	V
Sine-to-digital converter							
301	AArel	Relative angular error	with reference to one periode, see Fig. 3	-20		20	%
302	f(OSC)	Oscillator frequency		200	256	300	kHz
303	TC(OSC)	Temperature coefficient of oscillator frequency			-0.1		%/K
304	hys	Converter hysteresis			1		LSB
Configuration inputs CFG1, CFG2, CFG3							
401	Vt()hi	Threshold voltage high		60		78	% VDD
402	Vt()lo	Threshold voltage low		25		40	% VDD
403	V0()	Open circuit voltage		43		57	% VDD
404	Ri()	Input resistance		45	150	450	kΩ
Enable input NEN							
501	Vt()hi	Threshold voltage high				2	V
502	Vt()lo	Threshold voltage low		0.8			V
503	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	300			mV
504	Ipu()	Pull-up current	V() = 0...VDD - 1 V	-240	-120	-25	µA
Digital outputs: A, B, C, D							
601	Vs()hi	Saturation voltage high	Vs()hi = VDD - V(), I() = -4 mA			0.4	V
602	Vs()lo	Saturation voltage low	I() = 4 mA			0.4	V
603	tr()	Rise time	CL() = 50 pF			60	ns

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 5 V ±10 % , Tj = -40 ... 125 °C, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
604	tf()	Fall time	CL() = 50 pF			60	ns
605	Ilk()	Leackage current	NEN = high, V() = 0 ... VDD	-5		5	µA
606	Vc()hi	Clamp voltage high	Vc()hi = V() - VDD, NEN = high, I() = 4 mA	0.3		1.6	V
607	Vc()lo	Clamp voltage low	NEN = high, I() = -4 mA	-1.5		-0.3	V
Digital inputs: A, B, C, D							
701	Vt()hi	Threshold voltage high				2	V
702	Vt()lo	Threshold voltage low		0.8			V
703	Vt()hys	Hysterese	Vt()hys = Vt()hi - Vt()lo	300			mV
704	Ipd()	Pull-down current	V() = 1 V...VDD	10	30	50	µA
Analog outputs: A, B, C, D							
801	SR	Slew Rate		2			V/µs
802	fhc()	Cut off frequency		500			kHz
803	I()	Output current		-1		1	mA
804	R()eda	Input resistance DA-converter	between pin B and pin C	6	8	10	kΩ
805	R()ada	Output resistance DA-converter	at pin A		100		kΩ

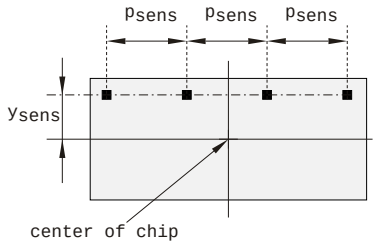


Figure 1: Location of HALL sensors on die

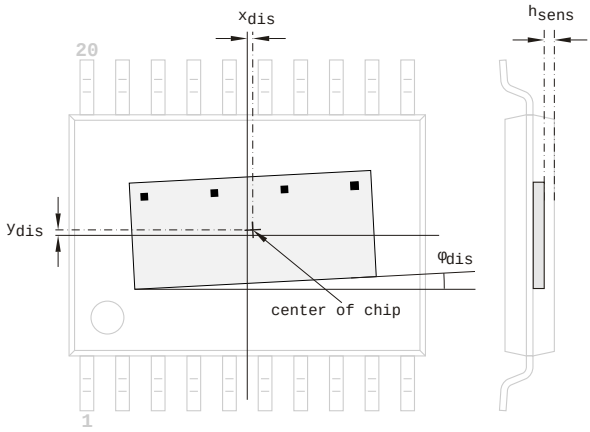


Figure 2: Position of die in TSSOP20 package

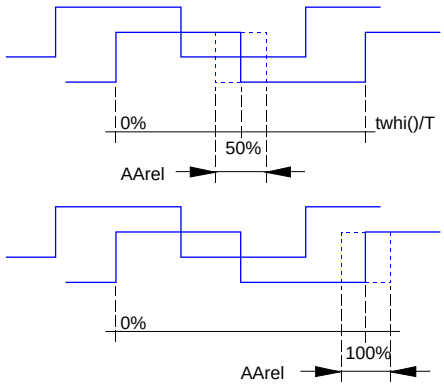


Figure 3: Definition of relative angular error

OPERATING CONDITIONS: Logic

Operating conditions: VDD = 5 V ±10 %, Tj = -40...125 °C, unless otherwise noted
Input level low = 0...0.45 V, high = 2.4 V...VDD, timing according Fig. 4

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
Logic						
I001	ts(NEN)	Setup time NEN	CLK : low → high, see Fig. 15	30		ns
I002	tp(NEN)	Delay time NENO	CLK : high → low, see Fig. 15		30	ns
I003	tp(SIG1)	Delay time SIG1	CL() = 50 pF, see Fig. 15		60	µs
I004	tp(SIG2)	Delay time SIG2	CL() = 50 pF, see Fig. 15		2	µs
I005	tp(CFGx)	Setup time at CFGx, x = 1..3	see Fig. 9		4	µs

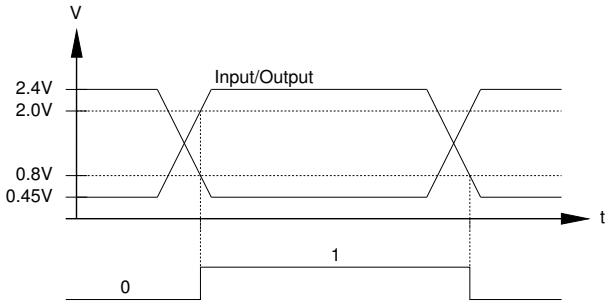


Figure 4: Reference levels for delays

The sensor principle

In conjunction with a magnetic tape iC-ML can be used to create a complete linear encoder system. With a Hall sensor pitch of 1.28 mm, the iC-ML is taylored to work with a magnetic tape having a pole pitch of 2.56 mm (5.12 mm magnetic periode). At a resolution of 8 bit, the digital increment represents a linear distance of 20 µm. In the same way, pole wheels can also be used together with the iC-ML.

Magnetic tapes (or pole wheels) with a smaller pitch than 2.56 mm can be used by skewing the iC-ML with respect to the tape direction and thus adjusting the projected sensor pitch to the tape pitch.

iC-ML has four Hall sensors which are used pairwise to generate sine- and cosine signals. Each Hall sensor pair detects the magnetic tape at a lateral distance of half of a magnetic periode. From the difference of the hall voltages, each Hall sensor pair generates either the sine or the cosine signal. Due to the differential sensing, the resulting signal voltages are insensitve to external homgenious magnetic fields and pole with variations.

From the physical principal, the Hall sensors are also insensitive to magnetic fields parallel to the chip surface.

Arrangement and signal outputs

Figure 5 shows the arrangement of the iC-ML to the magnetic tape. Both chip and magnetic tape are parallel aligned to each other. The coordinate system is defined in the way that the z-coordinate is perpendicularly to the surface of the magnetic tape and the x-direction lies in direction of travel. The four HALL sensors are located at the upper edge of the chip and should be centered to the magnetic tape for optimized magnetic sensing.

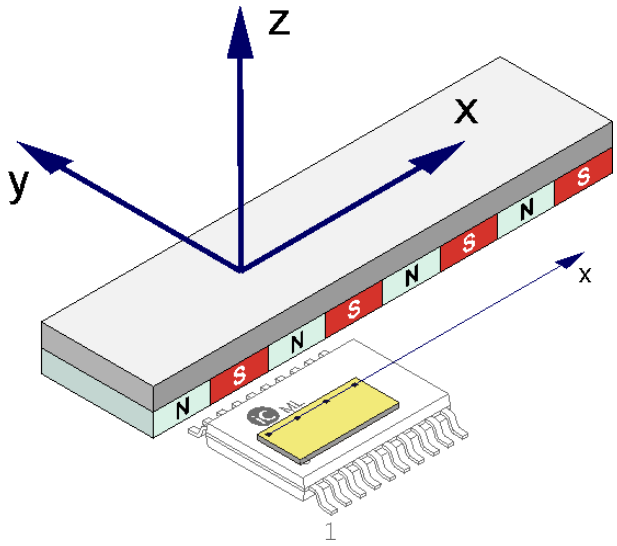


Figure 5: Arrangement of iC-ML to the magnetic tape

Magnet wheels are scanned depending upon their direction of magnetization either on the surface or at the periphery. The sensing radius must be chosen accordingly to match the magnetic pitch to the sensor pitch.

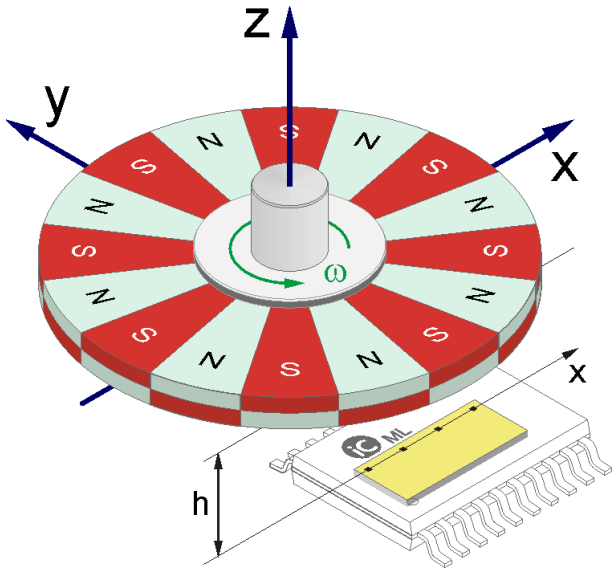


Figure 6: Sensing of a pole wheel at the surface using iC-ML

For further consideration, the reference position of the chip is selected in such a way that the x-position of the outmost left hall sensor coincides with the zero point of the magnetic tape, which is located at the center of an arbritrally chosen north pole of the magnetic tape. Then, as shown in figure 8, the corresponding output signals in the analog operation mode (S-Sensor) will be available as a function of the lateral shift x_d. The electrical signals exhibit the same periodicity as the magnetic field of the magnetic tape, showing extremes at the poles (Vcos) or at the pole gaps (Vsin).

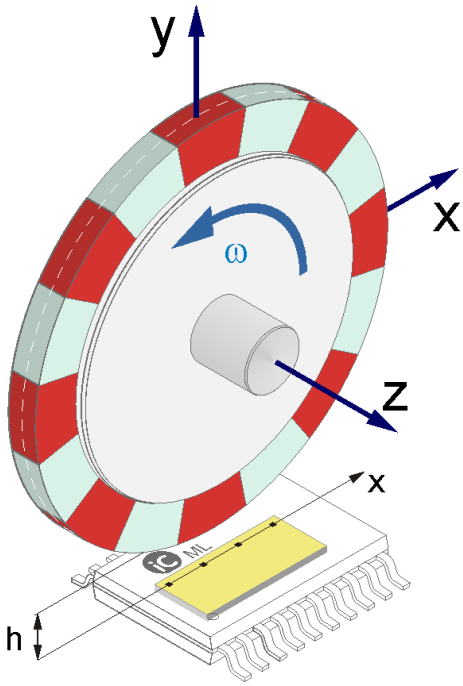


Figure 7: Sensing of a pole wheel at the peripherie using iC-ML

When the Vcos and Vsin signals are displayed as a Lissajou figure, a rotating vector is defined. If the chip is moved in positive x-direction with respect to the tape, this vector rotates counterclockwise (mathematically positive rotation), whereas if the tape is moved in positive x-direction (with respect to the chip), the vector rotates clockwise (mathematically negative rotation).

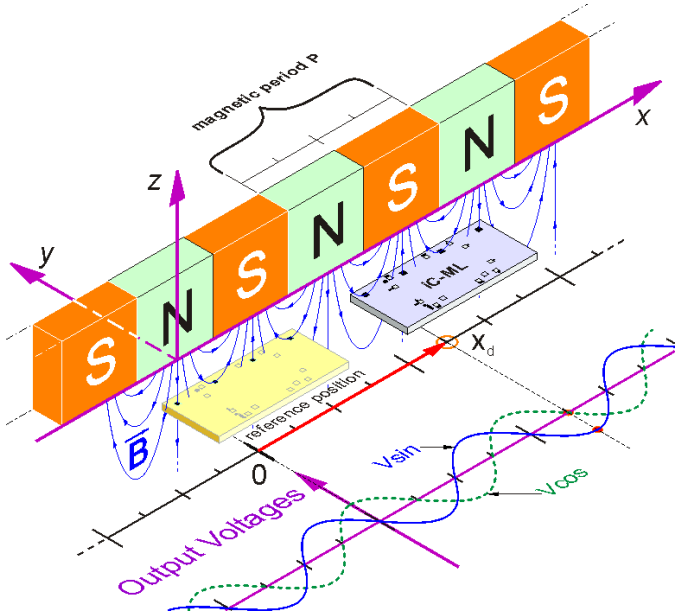


Figure 8: Signal outputs Vsin und Vcos

Programming the configuration

iC-ML has 28 modes of operation (see tables on the following pages). After the device has been switched on or "woken up" from standby mode by a low signal at pin NEN the levels at the configuration inputs CFG1 to CFG3 are assessed. These three-level inputs can be connected to GND (*low*), left open (*open*) or connected to VDD (*high*). For correct identification, a setup time of at least tp(CFGx) = 4 µs must be maintained between programming the configuration and activating the device. While the device is active changes in signal at the configuration inputs are ignored.

If several iC-MLs are connected in series in chain operation (see the description of functions on page 12) it must be ensured that the NEN input of the devices is switched to *low* during the various clock cycles and that the programming default does thus not lie within the active phase of the devices.

In standby all ports are switched to tristate, i.e. high impedance. Only in chain operation modes port D is active *high* so that the devices arranged further behind can also be deactivated.

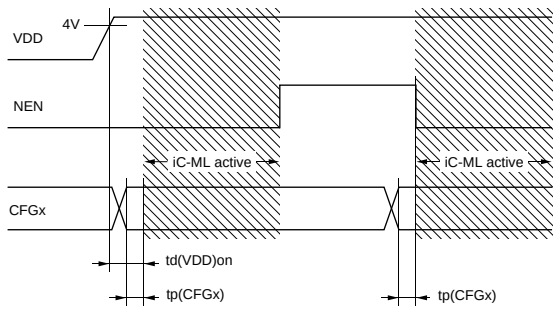


Figure 9: Programming the configuration

Operating modes

Mode	NEN	CFG1	CFG2	CFG3	Port A	Port B	Port C	Port D	Res.	Comments
Analog										
S-Sensor	low	low	low	low	PSIN	VREF	PCOS	GAIN		
D-Sensor	low	open	low	low	PSIN	NSIN	PCOS	NCOS		PRM
D-Sensor	low	high	low	low	PSIN	NSIN	PCOS	NCOS		
Linear output										
R-Sensor	low	low	open	low	VTRI	REFH	MSB	NERR	8	
	low	open	open	low	VTRI	REFH	MSB	GAIN	8	
	low	high	open	low	VSAW	REFH	REFL	NERR	8	
	low	high	open	high	VSAW	REFH	REFL	GAIN	8	
Chain-Mode										
AB-Chain	low	low	high	low	A	CLK	B	NENO	8	
D-Chain	low	open	high	low	PSIN/NSIN	CLK	PCOS/NCOS	NENO		
S-Chain	low	high	high	low	PSIN/VREF	CLK	PCOS/GAIN	NENO		
Incr. ABZ										
ABZ 8-1	low	low	low	open	A	B	Z	NERR	8	AB=1
ABZ 8-0	low	open	low	open	A	B	Z	NERR	8	AB=0
ABZ 7-1	low	low	open	open	A	B	Z	NERR	7	AB=1
ABZ 7-0	low	open	open	open	A	B	Z	NERR	7	AB=0
ABZ 6-1	low	low	high	open	A	B	Z	NERR	6	AB=1
ABZ 6-0	low	open	high	open	A	B	Z	NERR	6	AB=0
ABZ 8-1	low	low	low	high	A	B	Z	NERR	8	AB=1, PRM
ABZ 8-0	low	open	low	high	A	B	Z	NERR	8	AB=0, PRM
ABZ 7-1	low	low	open	high	A	B	Z	NERR	7	AB=1, PRM
ABZ 7-0	low	open	open	high	A	B	Z	NERR	7	AB=0, PRM
ABZ 6-1	low	low	high	high	A	B	Z	NERR	6	AB=1, PRM
ABZ 6-0	low	open	high	high	A	B	Z	NERR	6	AB=0, PRM
Incr. CLK										
CLK 8	low	high	low	open	NCLKUP	NCLKDN	NCLR	NERR	8	
CLK 6	low	high	high	open	NCLKUP	NCLKDN	NCLR	NERR	6	
DIR 8	low	high	low	high	NCLK	DIR	NCLR	NERR	8	
DIR 6	low	high	high	high	NCLK	DIR	NCLR	NERR	6	
Test (for iC-Haus use only)										
Test	low	high	open	open						Test
Standby										
	high	x	x	x	TRI	TRI	TRI	TRI[1]		

[1] In chain operation port D is active *high* so that the backend devices can also be deactivated.

Analog modes of operation

Mode	NEN	CFG1	CFG2	CFG3	Port A	Port B	Port C	Port D	Res.	Comment
Analog										
S-Sensor	low	low	low	low	PSIN	VREF	PCOS	GAIN		
D-Sensor	low	open	low	low	PSIN	NSIN	PCOS	NCOS		PRM
D-Sensor	low	high	low	low	PSIN	NSIN	PCOS	NCOS		

In the analog modes of operation the amplified Hall voltages are available at the output ports. The sine/ cosine output signals are controlled to have stable amplitudes of 1 V and referenced to a DC value equivalent to half of the supply voltage (VREF). Due to the internal signal conditioning unit, no special adjustment is required. An externally connected interpolator can be used if further trimming of the output signals is desired.

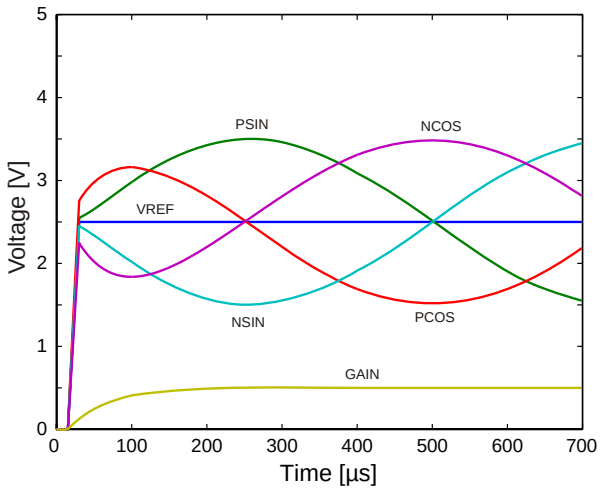


Figure 10: Analog mode output signals after switching on the device

S sensor mode
After the device has been activated via NEN = *low* the sensor is set to its operating point. All signals are referenced to half the supply voltage (VREF). In S sensor mode this potential is available at port B. Ports A and C output the sine and cosine Hall voltages set to 2 Vss. The angle can be calculated from the relation of the sine voltage (difference in voltage PSIN to VREF) to the cosine voltage (difference in voltage PCOS to VREF). The device supplies an angle which remains non-ambiguous over a 360° rotation of the permanent magnet.

Signal GAIN allows conclusions to be drawn as to the operating point of the sensor. This is influenced by the amplitude of the magnetic field, the sensor supply voltage and temperature. The higher the GAIN potential, the greater the necessary amplification of the Hall voltages; the external magnetic field is smaller. Besides recording the direction of magnetization of the permanent magnet the distance between the magnet and sensor may also be assessed using the GAIN signal. If the gain is insufficient to boost the Hall voltages to 2 Vss the amplitude control reaches its upper limit and the output amplitude becomes smaller.

The GAIN signal can be used to adjust the permanent magnet. If the central point of both the magnet and sensor iC-ML are the same the GAIN signal has no harmonics. A misaligned sensor must readjust the operating point depending on the angle; the GAIN signal varies in amplitude. To adjust the sensor to the magnetic tape this must be shifted along its y- and z-axis so that the GAIN signal has to readjust as little as possible.

D sensor mode
In D sensor mode differential sine (pin A and pin B) and cosine (pin C and pin D) signals are supplied at the output; as opposed to S sensor mode inverted Hall signals are now also available at the ports. The advantage of this mode of operation is the doubled signal amplitude of the differential Hall voltages and the lack of dependence on reference voltage VREF. The angle is now calculated via the ratio of the difference between PSIN and NSIN and between PCOS and NCOS.

D sensor mode is also available with a reduced power consumption (PRM or Power Reduced Mode). In this mode the Hall sensor is supplied with current less frequently, reducing the power consumption. Here it must be observed that the maximum rotating frequency also drops by a factor of 2.

Resistor modes of operation

Mode	NEN	CFG1	CFG2	CFG3	Port A	Port B	Port C	Port D	Res.	Comments
Linear output										
R-Sensor	low	low	open	low	VTRI	REFH	MSB	NERR	8	
	low	open	open	low	VTRI	REFH	MSB	GAIN	8	
	low	high	open	low	VSAW	REFH	REFL	NERR	8	
	low	high	open	high	VSAW	REFH	REFL	GAIN	8	

Resistor modes of operation

In R sensor mode the taps of an integrated resistive divider are selected depending on the angular position ("potentiometer replacement"). The value of the absolut angular position acts as a "wiper" and selects one of the 256 taps on the resistor chain.

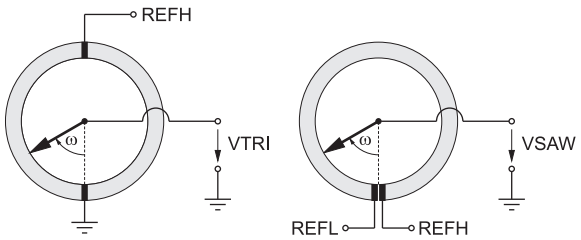


Figure 11: Potentiometer equivalents for resistor mode operations

In modes with a sawtooth voltage VSAW at port A the angle is converted into a linear voltage which lies within thresholds REFH and REFL at ports B and C (see Figure 12). The integrated resistor chain is directly available at the ports so that thresholds REFH and REFL can also be reversed. Depending on the selected mode either a GAIN signal or a NERR error signal are present at port D to monitor the amplitude. If the amplitude is at least 70 %, NERR is *high*; should the amplitude sink to below 50 % of the set amplitude, NERR switches to active *low*.

Modes of operation with a triangular voltage VTRI avoids the discontinuity at the zero angular position. Signal MSB can be used to differentiate between the first and second half rotation. The delta voltage is limited by thresholds REFH and GND. As in VSAW mode both GAIN and NERR signals are available.

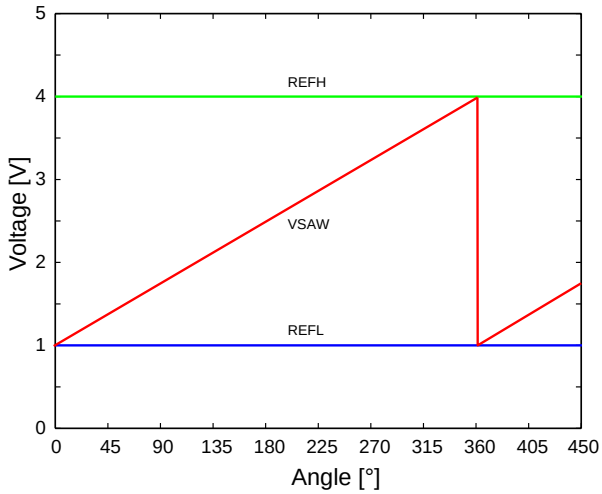


Figure 12: R-Sensor mode with sawtooth output voltage VSAW

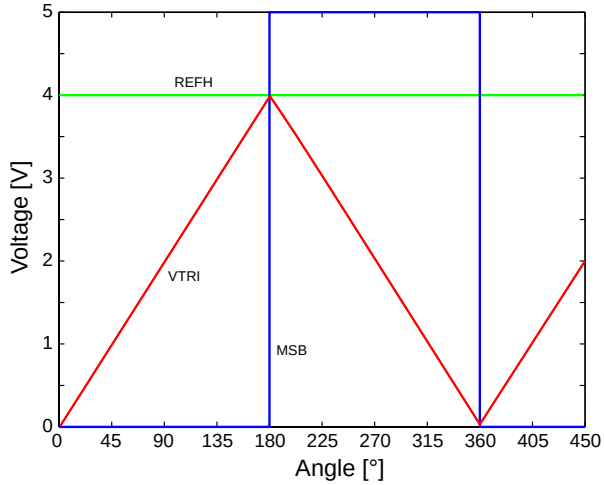


Figure 13: R-Sensor mode with triangular output voltage VTRI

AB chain, D chain and S chain modes

Mode	NEN	CFG1	CFG2	CFG3	Port A	Port B	Port C	Port D	Res.	Comments
Chain operation										
AB chain	low	low	high	low	A	CLK	B	NENO	8	
D chain	low	open	high	low	PSIN/NSIN	CLK	PCOS/NCOS	NENO		
S chain	low	high	high	low	PSIN/VREF	CLK	PCOS/GAIN	NENO		

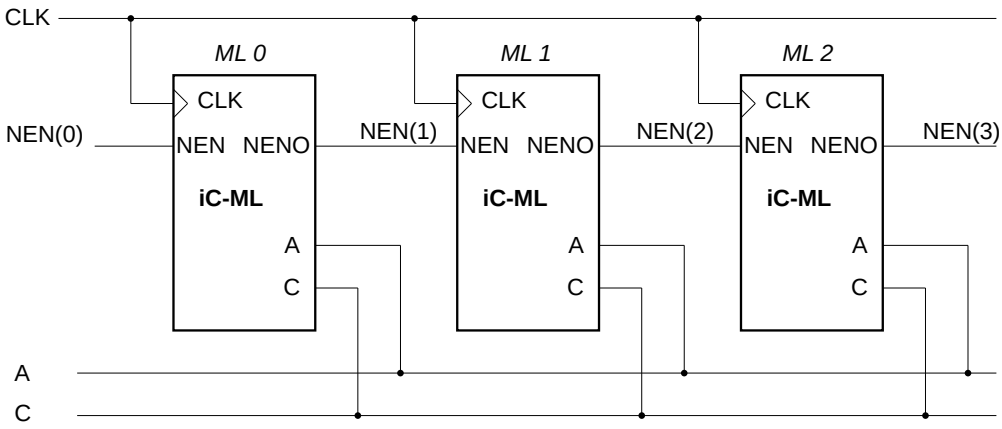


Figure 14: Chain modes for iC-ML

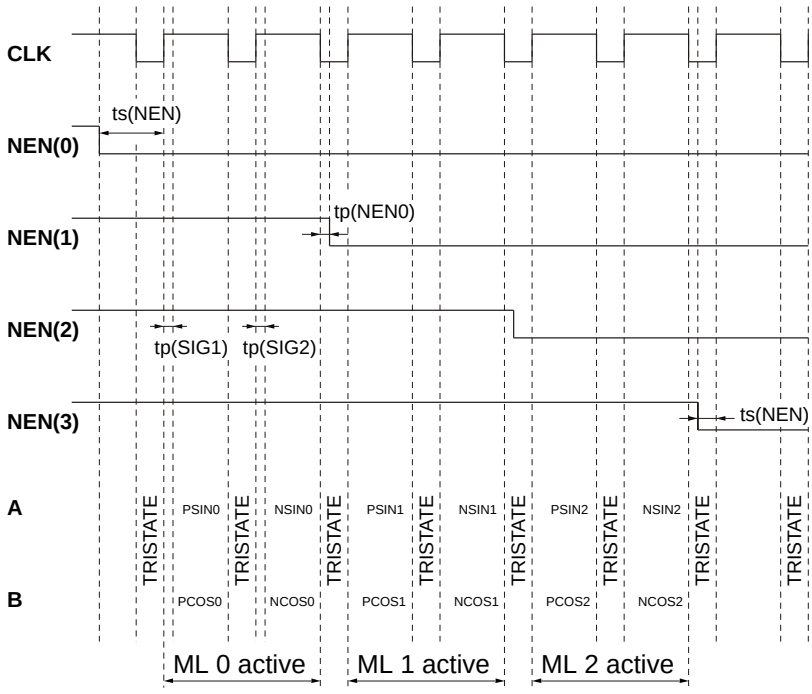


Figure 15: Signal patterns in D chain mode

In the various chain modes multiple iC-MLs can be arranged in a chain (see Figure 14) where all of the devices are connected by a shared CLK line (pin B). The NEN input is evaluated synchronously with the rising CLK edge. If the NEN input is switched to *low*, the device is active during the following CLK cycle(s). To allow the devices to be cascaded a delayed enable signal is generated at output pin NENO (pin D) with which the follow-on device can be activated. If the NEN input of the first device in the chain is reset to high, all devices in the chain are deactivated. Bus lines A (pin A) and C (pin C) are activated by tristate output stages which are high impedance when NEN is high and CLK is *low* and also following the second rising CLK edge.

AB chain mode
In AB chain mode two A/B digital incremental signals are generated at ports A and C. The two square-wave signals are phase shifted at either +90° or -90°, depending on the direction of rotation. Following a CLK pulse the next device in the chain is enabled. Here the falling CLK edge deactivates the current device (e.g. ML 1 in Figure 14) and activates the next device in the chain (ML 2) with a low signal at its NEN input. After a device has been activated the two bus lines A (port A) and B (port C) are first switched to low (see Figure 15). This is then followed by the incremental signals being output, starting at the zero position. In the event of error the bus lines remain low.

D chain mode
In D chain mode differential sine and cosine signals are generated at ports A and C. During the first clock pulse signals PSIN and PCOS are presented to the bus; during the second pulse signals NSIN and NCOS are on the bus (see Figure 15). In this mode each device is thus active for two clock pulses. During the first clock pulse the non-inverted sine (port A) and cosine (port C) signals are first presented to the bus, with the inverted signals following on the positive CLK edge during the second pulse. The falling CLK edge in the second clock pulse deactivates the current device and activates the following device in the chain with a low signal at its NEN input.

S chain mode
In S chain mode the non-inverted sine (port A) and cosine (port C) signals are presented to the bus during the first clock pulse, with the signals VREF (port A) and GAIN (port C) following on the positive CLK edge of the next pulse. Each device is thus active for two clock pulses. The falling CLK edge in the second clock pulse deactivates the current device and activates the following device in the chain with a low signal at its NEN input.

The sine and cosine signals can be assessed using signal VREF. Signal GAIN (pin D) indicates iC-ML's internal amplification (see Electrical Characteristics No. 207) and can be used to estimate the signal amplitude of the internal Hall sensor. The GAIN signal can also be used to adjust the rotary axis of the magnet to the center of the chip.

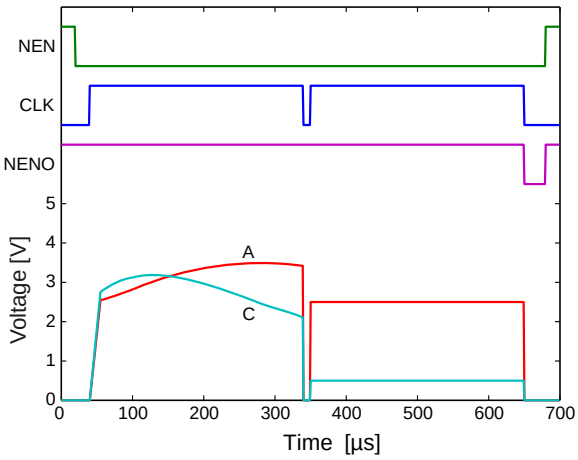


Figure 16: Bus signals and control signals in S chain mode

Incremental ABZ modes

Mode	NEN	CFG1	CFG2	CFG3	Port A	Port B	Port C	Port D	Res.	Comments
Incr. ABZ										
ABZ 8-1	low	low	low	open	A	B	Z	NERR	8	AB=1
ABZ 8-0	low	open	low	open	A	B	Z	NERR	8	AB=0
ABZ 7-1	low	low	open	open	A	B	Z	NERR	7	AB=1
ABZ 7-0	low	open	open	open	A	B	Z	NERR	7	AB=0
ABZ 6-1	low	low	high	open	A	B	Z	NERR	6	AB=1
ABZ 6-0	low	open	high	open	A	B	Z	NERR	6	AB=0
ABZ 8-1	low	low	low	high	A	B	Z	NERR	8	AB=1, PRM
ABZ 8-0	low	open	low	high	A	B	Z	NERR	8	AB=0, PRM
ABZ 7-1	low	low	open	high	A	B	Z	NERR	7	AB=1, PRM
ABZ 7-0	low	open	open	high	A	B	Z	NERR	7	AB=0, PRM
ABZ 6-1	low	low	high	high	A	B	Z	NERR	6	AB=1, PRM
ABZ 6-0	low	open	high	high	A	B	Z	NERR	6	AB=0, PRM

iC-ML has an 8-bit sine/digital converter which can convert the sine/cosine sensor signals into a digitized angle. This angle is made available at the ports as an incremental value. Signal Z is always *high* when the angle is 0°; otherwise the signal is low. In all incremental modes of operation error signal NERR is available so that the plausibility of the counter value can be verified. At an amplitude which is less than 50 % of the set amplitude the error signal switches to *low*; at an amplitude greater than 70 % the error signal is reset, i.e. set to *high*.

Three different quantities regarding the number of edges per rotation of the magnet can be selected. These are a resolution of 6 bits (64 edges per rotation), 7 bits (128 edges) or 8 bits (256 edges). The conversion process is count-safe, i. e. the output of all edges up to the current angle position is guaranteed as long as the input frequency is less than the maximum possible rotation.

All incremental resolutions also have a reduced power consumption mode(PRM). In this mode the Hall sensor is supplied with current intermittently, reducing the power consumption. Here it must be noted that the maximum input frequency drops by a factor of 2.

A distinction can be made between the various modes of operation by studying the level of the AB signals on the Z pulse. In mode AB = 1 signals A and B are both *high*, as is Z at an angle of 0°. In mode AB = 0, however, both signals A and B are *low* when the Z signal is *high*.

Firstly, the behavior of the sensor on switching on the device is described when the magnetic tape moves in the +x-direction (Figure 17). After switching on the sensor via NEN at *low* the sensor looks for its operating point. If 70 % of the set amplitude is achieved the error signal is reset. An error status during this phase is also signaled when signals A and B are *high* and Z *low*. In an error-free state Z is always *high* at zero position. iC-ML continues to search for its operating point by outputting the position of the external magnetic field at maximum count frequency via the incremental interface. Once the actual position has been obtained the device follows a changed input signal in real time. The edge frequency is thus 256 times the frequency of periodical movement of the magnetic tape at a set resolution of 8 bits. If a (rising) edge reaches B before a (rising) edge A, this means that the counter value has risen. If the edge reaches A before B, however, this indicates that the absolute value is lower.

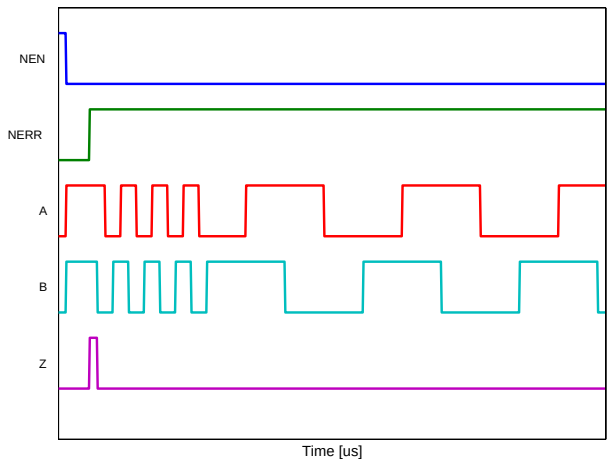


Figure 17: Incremental signals after switching on the device, counting up

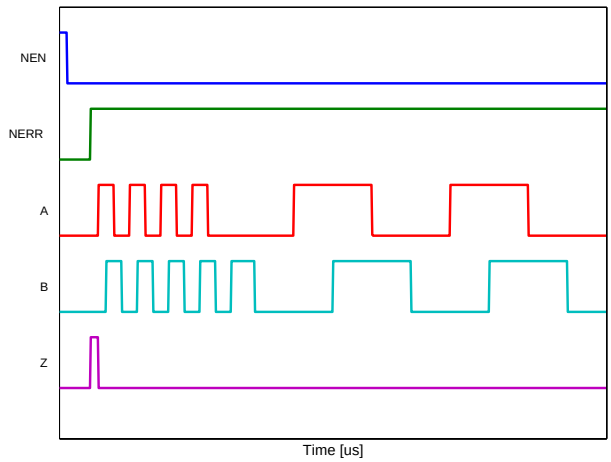


Figure 18: Incremental signals after switching on the device, counting down

Always starting at zero position, the device begins searching for the absolute position, locating it as quickly as possible. If this positon corresponds to an angle between 0° and 180° the device counts up to the operating point; if this angle is between 180° and 360°, it first counts down. Starting when the device is switched on all edges are output until the absolute position is reached. The setup has to wait until a certain time has elapsed; this is dependent on the selected resolution and is the settling time of the sensor until the error bit is deleted plus the time needed to count up or down to the absolute position. With a resolution of 8 bits and an angle of 180°, for example, this period constitutes 100 µs sensor settling time plus 128 times 4 µs until the absolute position has been pinpointed. The absolute position is thus available after a maximum of 612 µs has elapsed.

By way of example Figure 18 illustrates how the incremental interface behaves when the device first counts down to the absolute position and the magnetic tape then moves forwards, with the sensor following with the relevant sequence. The Z signal is synchronous with A and B at *low*.

Incremental CLK modes

Mode	NEN	CFG1	CFG2	CFG3	Port A	Port B	Port C	Port D	Res.	Comments
Inkr. CLK										
CLK 8	low	high	low	open	NCLKUP	NCLKDN	NCLR	NERR	8	
CLK 6	low	high	high	open	NCLKUP	NCLKDN	NCLR	NERR	6	
DIR 8	low	high	low	high	NCLK	DIR	NCLR	NERR	8	
DIR 6	low	high	high	high	NCLK	DIR	NCLR	NERR	6	

CLK-INC mode
In CLK-INC mode two different count signals are provided for the countup and countdown sequences. Depending on the direction of rotation either signal NCLKUP (pin A) is pulsed when the device counts up or signal NCLKDN (pin B) when the device counts down. In each case the remaining signal is *high*. The zero angle is displayed by the NCLR index track which can serve as an asynchronous reset for an external counter.

Figure 19 demonstrates how iC-ML behaves in CLK-INC mode, firstly when it counts up from the zero position and then, following a change in the direction of movement, when it counts back down to zero position.

This mode permits the operation of external binary counter modules (such as 74HC/HCT193, for example), with signal NCLR (pin C) being used to reset the counter. With a rising edge of clock signal NCLKUP and a high at NCLKDN the counter status is incremented; with a rising edge of clock signal NCLKDN and a high at NCLKUP the counter status is decremented. Two 4-bit counters can be cascaded here to create a full 8-bit counter.

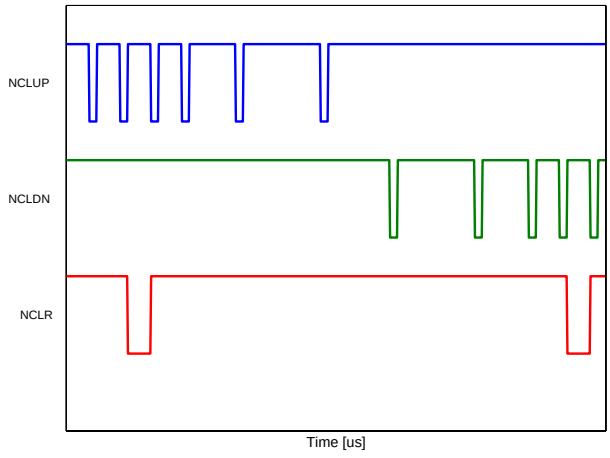


Figure 19: CLK-INC mode

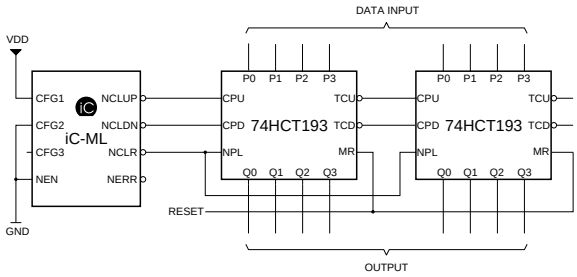


Figure 20: iC-ML with binary counter 74HCT193

DIR-INC mode

In DIR-INC mode a change in angle for both directions of rotation generates an output pulse for signal CLK (pin A). Signal DIR (pin B) gives the direction of rotation. This mode permits the operation of external binary counter modules (such as 74HC/HCT191, for example), with signal NCLR (pin C) being used to reset the external counter. With a rising edge at CLK the counter status is counted up or down, depending on the value of the DIR signal. A low at DIR triggers a countup; a high causes the setup to count down. Figure 17 shows a countup sequence followed by a countdown sequence, both across the zero position.

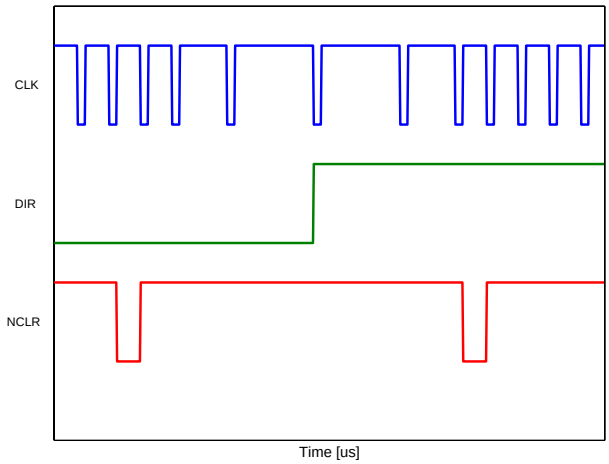


Figure 21: DIR-INC mode

iC-Haus expressly reserves the right to change its products and/or specifications. An Infoletter gives details as to any amendments and additions made to the relevant current specifications on our internet website www.ichaus.de/infoletter; this letter is generated automatically and shall be sent to registered users by email.
Copying – even as an excerpt – is only permitted with iC-Haus approval in writing and precise reference to source.
iC-Haus does not warrant the accuracy, completeness or timeliness of the specification on this site and does not assume liability for any errors or omissions in the materials. The data specified is intended solely for the purpose of product description. No representations or warranties, either express or implied, of merchantability, fitness for a particular purpose or of any other nature are made hereunder with respect to information/specification or the products to which information refers and no guarantee with respect to compliance to the intended use is given. In particular, this also applies to the stated possible applications or areas of applications of the product.
iC-Haus conveys no patent, copyright, mask work right or other trade mark right to this product. iC-Haus assumes no liability for any patent and/or other trade mark rights of a third party resulting from processing or handling of the product and/or any other use of the product.
As a general rule our developments, IPs, principle circuitry and range of Integrated Circuits are suitable and specifically designed for appropriate use in technical applications, such as in devices, systems and any kind of technical equipment, in so far as they do not infringe existing patent rights. In principle the range of use is limitless in a technical sense and refers to the products listed in the inventory of goods compiled for the 2008 and following export trade statistics issued annually by the Bureau of Statistics in Wiesbaden, for example, or to any product in the product catalogue published for the 2007 and following exhibitions in Hanover (Hannover-Messe).
We understand suitable application of our published designs to be state-of-the-art technology which can no longer be classed as inventive under the stipulations of patent law. Our explicit application notes are to be treated only as mere examples of the many possible and extremely advantageous uses our products can be put to.

ORDERING INFORMATION

Type	Package	Order Designation
iC-ML iC-ML evaluation board	TSSOP20	iC-ML TSSOP20 iC-ML EVAL ML1D

For technical support, information about prices and terms of delivery please contact:

iC-Haus GmbH
Am Kuemmerling 18
D-55294 Bodenheim
GERMANY

Tel.: +49 (61 35) 92 92-0
Fax: +49 (61 35) 92 92-192
Web: http://www.ichaus.com
E-Mail: sales@ichaus.com

Appointed local distributors: http://www.ichaus.com/sales_partners