iC-MH
12-BIT ANGULAR HALL ENCODER

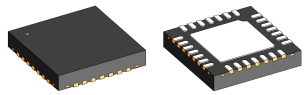
FEATURES

- Real-time system for rotation speed of up to 120,000 rpm
- Integrated Hall sensors with automatic offset compensation
- 4x sensor arrangement for fault-tolerant adjustment
- Amplitude control for optimum operating point
- Interpolator with 4096 angular increments/resolution better than 0.1°
- Programmable resolution, hysteresis, edge spacing, zero position and rotating direction
- Incremental output of sensor position of up to 8 MHz edge rate
- RS422-compatible AB encoder signals with index Z
- UVW commutation signals for EC motor applications
- BiSS interface for data output and configuration
- SSI-compatible output mode
- Integrated ZAP diodes for module setup and OEM data, programmable via BiSS interface
- Signal error (e.g. magnet loss) can be read out via BiSS interface
- Extended temperature range from -40 to +125 °C

APPLICATIONS

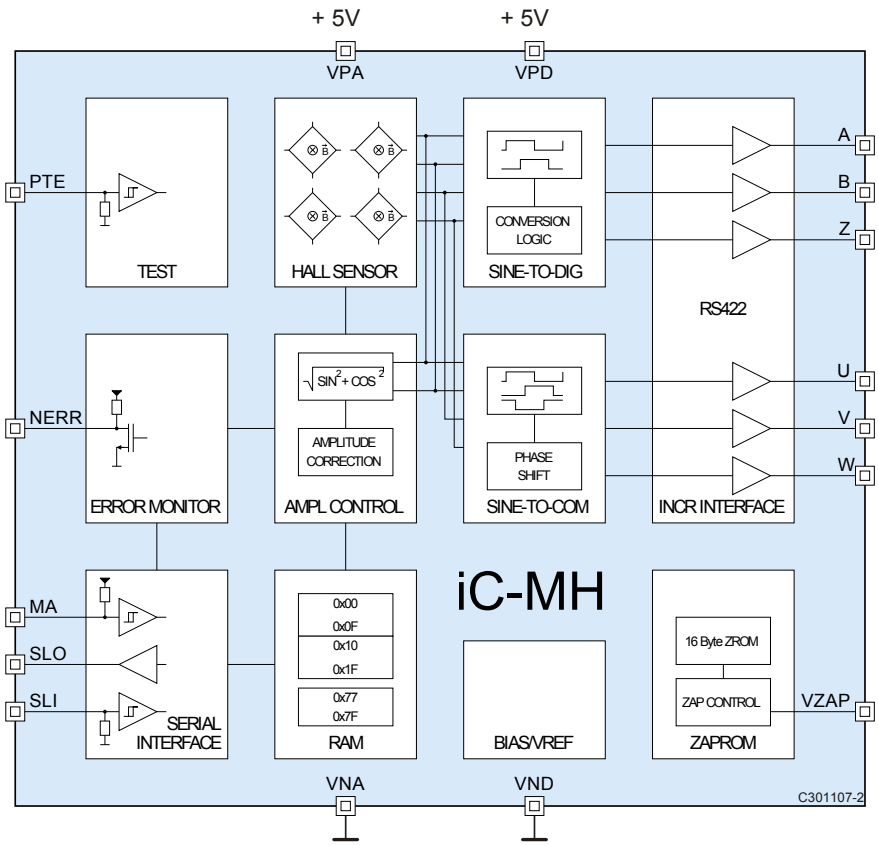
- Digital angular sensor technology, 0–360°
- Incremental angular encoder
- Absolute angular encoder
- Brushless motors
- Motor feedback
- Rotational speed control

PACKAGES



QFN28 5 mm x 5 mm

BLOCK DIAGRAM



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DESCRIPTION

The iC-MH 12-bit angular encoder is a position sensor with integrated Hall sensors for scanning a permanent magnet. The signal conditioning unit generates constant amplitude sine and cosine voltages that can be used for angle calculation. The resolution can be programmed up to a maximum of 4,096 angular increments per rotation.

The integrated BiSS Interface also enables the position data of several networked sensors to be read out. And the integrated memory can be written embedded in the data protocol.

The incremental interface with the pins A, B and Z supplies quadrature signals with an edge rate of up to 8 MHz. Interpolation can be carried out with maximum resolution at a speed of 120,000 rpm. The position of the index pulse Z is adjustable.

The commutation interface with the signals U, V and W provides 120° phase-shifted signals for block commutation. The zero point of the commutation signals is freely definable in increments of 1.875° over 360°. The commutation signals are available for EC motors with 1 and 2 pole pairs.

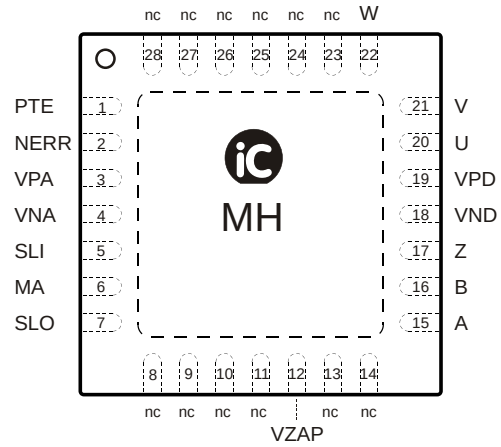
The RS422-compatible outputs of the incremental interface and the commutation interface are programmable in the output current and the slew rate.

In conjunction with a rotating permanent magnet, the iC-MH module forms a one-chip encoder. The entire configuration can be stored in the internal parameter ROM with zapping diodes. The integrated programming algorithm is responsible for the writing of the ROM structure.

The device described here is a multifunctional iC that contains integrated BiSS C interface components. The BiSS C process is protected by patent DE 10310622 B4 owned by iC-Haus GmbH and its application requires the conclusion of a license (free of charge).
Download the license at www.biss-interface.com/bua

PACKAGING INFORMATION QFN28 5 mm x 5 mm to JEDEC MO-220-VHHD-1

PIN CONFIGURATION QFN28 5 mm x 5 mm



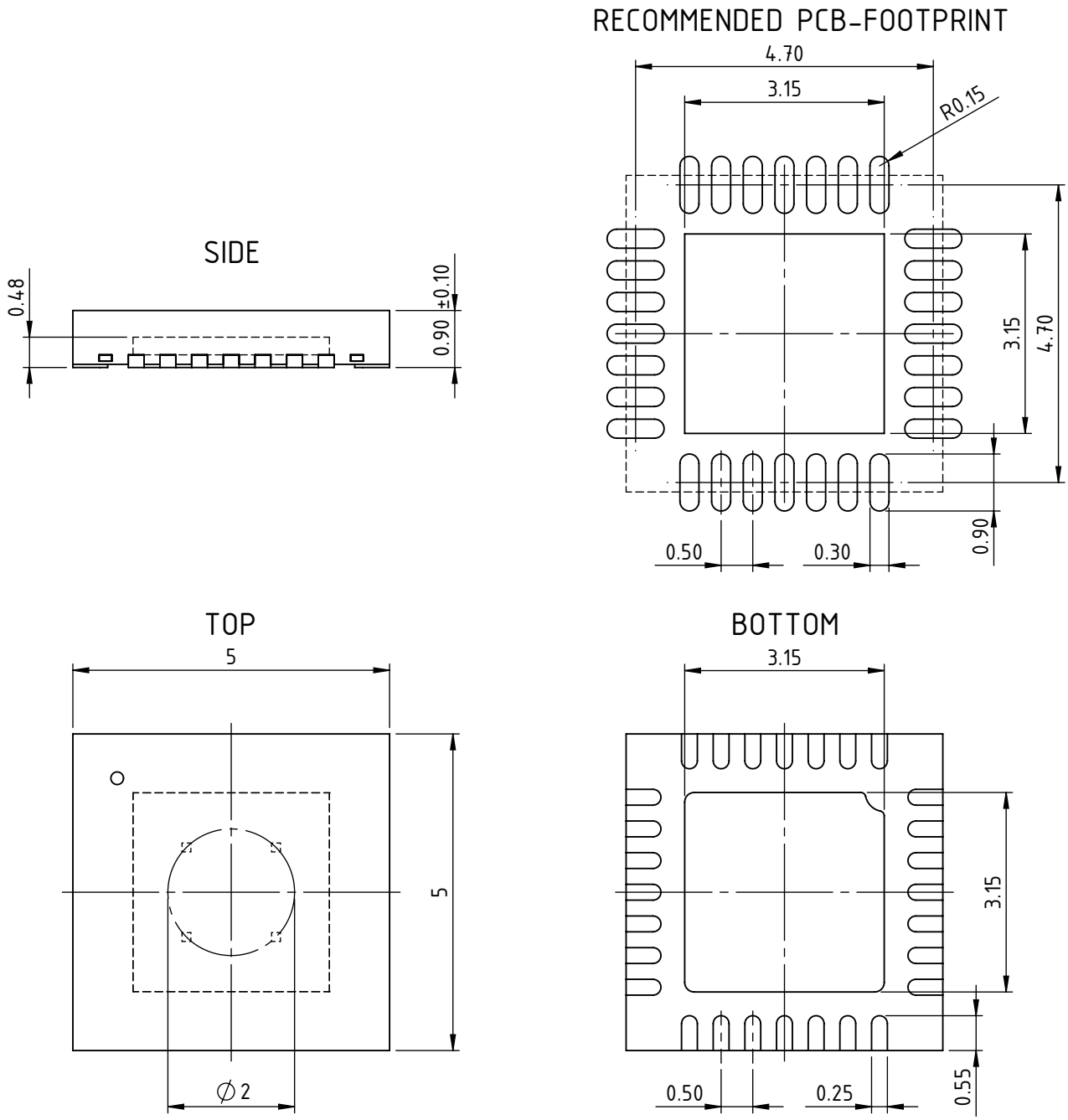
PIN FUNCTIONS

No.	Name	Function
1	PTE	Test Enable Pin (connect to VNA, VND)
2	NERR	Error Output (active low)
3	VPA	+5 V Supply Voltage (analog)
4	VNA	Ground (analog)
5	SLI	BiSS Interface, Data Input
6	MA	BiSS Interface, Clock Input
7	SLO	BiSS Interface, Data Output
8-11	nc	not connected
12	VZAP	Zener Zapping Programming Voltage
13,14	nc	not connected
15	A	Incremental A (+NU)
16	B	Incremental B (+NV)
17	Z	Index Z (+NW)
18	VND	Ground (digital)
19	VPD	+5 V Supply Voltage (digital)
20	U	Commutation U (+NA)
21	V	Commutation V (+NB)
22	W	Commutation W (+NZ)
23-28	nc	not connected
	TP	Thermal Pad

The *Thermal Pad* is to be connected to VNA on the PCB. Orientation of the logo (iC MH CODE ...) is subject to alteration.

PACKAGE DIMENSIONS

All dimensions given in mm.



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.
Tolerance of sensor pattern: ±0.10mm / ±1° (with respect to center of backside pad). dra_qfn28-5x5-2_mh8_pack_1, 10:1

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Supply voltages at VPA, VPD		-0.3	6	V
G002	V(VZAP)	Zapping voltage		-0.3	8	V
G003	V()	Voltages at A, B, Z, U, V, W, MA, SLO, SLI, NERR, PTE		-0.3	6	V
G004	I()	Current in VPA		-10	20	mA
G005	I()	Current in VPD		-20	200	mA
G006	I()	Current in A, B, Z, U, V, W		-100	100	mA
G007	I()	Current in MA, SLO, SLI, NERR, PTE		-10	10	mA
G008	Vd()	ESD voltage, all pins	HBM 100 pF discharged over 1.5 kΩ		2	kV
G009	Ts	Storage temperature		-40	150	°C
G010	Tj	Chip temperature		-40	135	°C

THERMAL DATA

Operating conditions: VPA, VPD = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Ambient temperature		-40		125	°C
T02	Rthja	Thermal resistance chip/ambient	package mounted on PCB, *thermal pad* at approx. 2 cm² cooling area		40		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions:
VPA, VPD = 5 V ±10 %, Tj = - 40 ... 125 °C, IBM adjusted to 200 µA , 4 mm NdFeB magnet, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	V(VPA, VPD)	Supply Voltage Range		4.5		5.5	V
002	I(VPA)	Supply Current in VPA			5	8	mA
003	I(VPD)	Supply Current in VPD	PRM = '0', without load		10	17	mA
004	I(VPD)	Supply Current in VPD	PRM = '1', without load		4	8	mA
005	Vc(hi)	Clamp Voltage hi at MA, SLI, SLO, PTE, NERR	Vc()hi = V() – VPD, I() = 1 mA	0.4		1.5	V
006	Vc(lo)	Clamp Voltage lo	I() = -1 mA	-1.5		-0.3	V
007	Ipd(PTE)						
Hall Sensors and Signal Conditioning							
101	Hext	Operating Magnetic Field Strength	at chip surface	20		100	kA/m
102	fmag	Operating Magnetic Field Frequency Rotating Speed of Magnet				2 120 000	kHz rpm
103	dsens	Diameter of HALL Sensor Array			2		mm
104	xdis	Lateral Displacement of Magnet to Chip				0.2	mm
105	xpac	Displacement Chip to Package	QFN28 package	-0.2		0.2	mm
106	ϕpac	Angular alignment of chip vs. package	QFN28 package	-3		+3	Deg
107	hpac	Distance of chip surface to package surface	QFN28 package		0.4		mm
108	Vos	Trimming range of output offset voltage	VOSS or VOSC = 0x7F			-55	mV
109	Vos	Trimming range of output offset voltage	VOSS or VOSC = 0x3F	55			mV
110	Vopt	Optimal differential output voltage	Vopt = Vpp(PSIN) – Vpp(NSIN), ENAC = '0', see fig. 6		4		Vpp
Amplitude Control							
201	Vampl	Differential Output Amplitude	Vampl = Vpp(PSIN) – Vpp(NSIN), ENAC = '1', see fig. 6	3.2		4.8	Vpp
202	Vratio	Amplitude Ratio	Vratio = Vpp(PSIN) / Vpp(PCOS)	1.09			
203	Vratio	Amplitude Ratio	Vratio = Vpp(PSIN) / Vpp(PCOS)			0.92	
204	tampl	Settling Time of Amplitude Control	±10%			300	µs
205	Vae()lo	Amplitude Error Threshold for active ERRAMIN	Vpp(PSIN) – Vpp(NSIN)	1.0		2.8	Vpp
206	Vae()hi	Amplitude Error Threshold for active ERRAMAX	Vpp(PSIN) – Vpp(NSIN)	4.8		5.8	Vpp
Bandgap Reference							
401	Vbg	Bandgap Reference Voltage		1.18	1.25	1.32	V
402	Vref	Reference Voltage		45	50	55	%VPA
403	Iibm	Bias Current	CIBM = 0x0 CIBM = 0xF Bias Current adjusted	 -370 -220	 -200	-100 -180	µA µA µA
404	VPDon	Turn-on Threshold VPD, System on	V(VPD) – V(VND), increasing voltage	3.65	4,0	4.3	V
405	VPDoff	Turn-off Threshold VPD, System reset	V(VPD) – V(VND), decreasing voltage	3	3.5	3.8	V
406	VPDhys	Hysteresis System on/reset		0.3			V
407	Vosr	Reference voltage offset compensation		475	500	525	mV

ELECTRICAL CHARACTERISTICS

Operating conditions:
VPA, VPD = 5 V ±10 %, Tj = - 40 ... 125 °C, IBM adjusted to 200 µA , 4 mm NdFeB magnet, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Clock Generation							
501	f()sys	System Clock	Bias Current adjusted	0.85	1.0	1.2	MHz
502	f()sdc	Sinus/Digital-Converter Clock	Bias Current adjusted	13.5	16	18	MHz
Sin/Digital Converter							
601	RESsdc	Sinus/Digital-Converter Resolution			12		Bit
602	AAabs	Absolute Angular Accuracy	Vpp() = 4 V, adjusted	-0.35		0.35	Deg
603	AArel	Relative Angular Accuracy	with reference to one output period at A, B, at Resolution 1024, see Fig. 17	-15	± 10	15	%
604	f()ab	Output frequency at A, B	CFGMTB = '0' CFGMTB = '1'		0.5 2.0		MHz MHz
605	REScom	Resolution of Commutation Converter			1.875		Deg
606	AAabs	Absolute Angular Accuracy of Commutation Converter		-0.5		0.5	Deg
BiSS Interface, Digital Outputs MA, SLO, Digital Input SLI							
701	Vs(SLO)hi	Saturation Voltage High	V(SLO) = V(VPD) – V(), I(SLO) = 4 mA			0.4	V
702	Vs(SLO)lo	Saturation Voltage Low	I(SLO) = 4 mA to VND			0.4	V
703	Isc(SLO)hi	Short-Circuit Current High	V(SLO) = V(VND), 25°C	-90	-50		mA
704	Isc(SLO)lo	Short-Circuit Current Low	V(SLO) = V(VPD), 25°C		50	80	mA
705	tr(SLO)	Rise Time SLO	CL = 50 pF			60	ns
706	tf(SLO)	Fall Time SLO	CL = 50 pF			60	ns
707	Vt()hi	Threshold Voltage High: MA, SLI				2	V
708	Vt()lo	Threshold Voltage Low: MA, SLI		0.8			V
709	Vt()hys	Threshold Hysteresis: MA, SLI		140	250		mV
710	Ipd(SLI)	Pull-Up Current: MA, SLI	V() = 0...VPD – 1 V	6	30	65	µA
711	Ipu(MA)	Pull-Up Current 30 µA MA		-60	-30	-6	µA
712	f()MA	Permissible Frequency at MA				10	MHz
Zapping and Test							
801	Vt()hi	Threshold Voltage High VZAP, PTE	with reference to VND			2	V
802	Vt()lo	Threshold Voltage Low VZAP, PTE	with reference to VND	0.8			V
803	Vt()hys	Hysteresis	Vt()hys = Vt()hi – Vt()lo	140	250		mV
804	Vt()nozap	Threshold Voltage Nozap VZAP	V() = V(VZAP) – V(VPD), V(VPD) = 5 V ±5 %, at chip temperature 27 °C	0.7			V
805	Vt()zap	Threshold Voltage Zap VZAP	V() = V(VZAP) – V(VPD), V(VPD) = 5 V ±5 %, at chip temperature 27 °C			1.2	V
806	V()zap	Zapping Voltage	PROG = '1'	6.9	7.0	7.1	V
807	V()zpd	Diode Voltage, zapped				2	V
808	V()uzpd	Diode Voltage, unzapped		3			V
809	Rpd()VZAP	Pull-Down Resistor at VZAP		30		55	kΩ
810	Ipd(PTE)	Pull-Down Current PTE	V() = 0...VPD – 1 V	-60	-30	-6	µA
NERR Output							
901	Vt()hi	Input Threshold Voltage High	with reference to VND			2	V
902	Vs()lo	Saturation Voltage Low	I() = 4 mA , with reference to VND			0.4	V
903	Vt()lo	Input Threshold Voltage Low	with reference to VND	0.8			V
904	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi – Vt()lo	140	250		mV
905	Ipu(NERR)	Pull-up Current	V(NERR) = 0...VPD – 1 V	-800	-300	-80	µA
906	Isc()lo	Short-Circuit Current NERR	V(NERR) = V(VPD), 25°C		50	80	mA
907	tf(NERR)	Decay Time NERR	CL = 50 pF			60	ns

ELECTRICAL CHARACTERISTICS

Operating conditions:
VPA, VPD = 5 V ±10 %, Tj = - 40 ... 125 °C, IBM adjusted to 200 µA , 4 mm NdFeB magnet, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Line Driver Outputs							
P01	Vs()hi	Saturation Voltage hi	Vs() = VPD − V(); CfgDR(1:0) = 00, I() = -4 mA CfgDR(1:0) = 01, I() = -50 mA CfgDR(1:0) = 10, I() = -50 mA CfgDR(1:0) = 11, I() = -20 mA			 200 700 700 400	 mV mV mV mV
P02	Vs()lo	Saturation Voltage lo	CfgDR(1:0) = 00, I() = -4 mA CfgDR(1:0) = 01, I() = -50 mA CfgDR(1:0) = 10, I() = -50 mA CfgDR(1:0) = 11, I() = -20 mA			200 700 700 400	mV mV mV mV
P03	Isc()hi	Short-Circuit Current hi	V() = 0 V; CfgDR(1:0) = 00 CfgDR(1:0) = 01 CfgDR(1:0) = 10 CfgDR(1:0) = 11	 -12 -125 -125 -60		 -4 -50 -50 -20	 mA mA mA mA
P04	Isc()lo	Short-Circuit Current lo	V() = VPD; CfgDR(1:0) = 00 CfgDR(1:0) = 01 CfgDR(1:0) = 10 CfgDR(1:0) = 11	 4 50 50 20		 12 125 125 60	 mA mA mA mA
P05	Ilk()tri	Leakage Current Tristate	TRIHL(1:0) = 11	-100		100	µA
P06	tr()	Rise-Time lo to hi at Q	RL = 100 Ω to VND; CfgDR(1:0) = 00 CfgDR(1:0) = 01 CfgDR(1:0) = 10 CfgDR(1:0) = 11	 5 5 50 5		 20 20 350 40	 ns ns ns ns
P07	tf()	Fall-Time hi to lo at Q	RL = 100 Ω to VND; CfgDR(1:0) = 00 CfgDR(1:0) = 01 CfgDR(1:0) = 10 CfgDR(1:0) = 11	 5 5 50 5		 20 20 350 40	 ns ns ns ns

OPERATING REQUIREMENTS: Serial Interface with SSI Protocol

Operating conditions: VPA, VPD = 5 V ±10 %, Ta = -40...125 °C, IBM calibrated to 200 µA;
Logic levels referenced to VND: lo = 0...0.45 V, hi = 2.4 V...VPD

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SSI Protocol (ENSSI = 1)						
I001	T_{MAS}	Permissible Clock Period	t_{out} determined by CFGTOS	250	2x t_{out}	ns
I002	t_{MASh}	Clock Signal Hi Level Duration		25	t_{out}	ns
I003	t_{MASl}	Clock Signal Lo Level Duration		25	t_{out}	ns

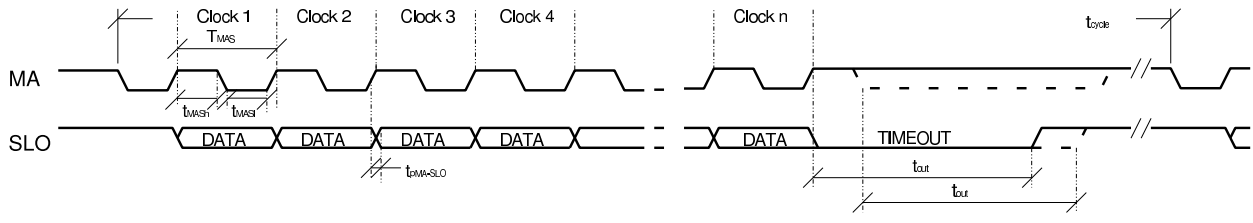


Figure 1: I/O interface timing with SSI protocol

REGISTER MAP

OVERVIEW

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Hall Signal Conditioning								
0x00 *z*	GAING(1:0)		GAINF(5:0)					
0x01 *z*	ENAC	GCC(6:0)						
0x02 *z*	1*	VOSS(6:0)						
0x03 *z*	PRM	VOSC(6:0)						
0x04 *z*	HCLH	DPU	1*	CFGTOB	CIBM(3:0)*			
RS422 Driver								
0x05 *z*	ENSSI	CFGPROT	CFGO(1:0)		TRIHL(1:0)		CFGDR(1:0)	
Sine/Digital Converter								
0x06 *z*	CFGRES(7:0)							
0x07 *z*	CFGZPOS(7:0)							
0x08 *z*	CFGHYS(1:0)		CFGDIR	CFGMTD	CFGSU	CFGPOLE	CFGAB(1:0)	
0x09 *z*	CfgCOM(7:0)							
0x0A *z*	OEMA							CFGMTD2
0x0B *z*	OEMB							
0x0C *z*	OEMC							
0x0D	OEMRAM							
Test Settings								
0x0E *p*	TEST(7:0)							
0x0F	-	res.	res.	res.	-	-	-	PROGZAP
ZAP Diodes (read only)								
0x10 .. 0x1F	ZAP diodes for addresses 0x00..0x0C and 0x7D..0x7F							
not used								
0x20 .. 0x41	'invalid addresses'							
Profile Identification (read only)								
0x42	BiSS Profile Identifier - 0x2C							
0x43	BiSS Profile Identifier - 0x0				Data length DLEN			
not used								
0x44 .. 0x75	'invalid address'							
Status Messages (read only; messages will be set back during reading)								
0x76	GAIN							
0x77	PROGERR	ERRSDATA	ERRAMIN	ERRAMAX	ERREXT	res.	res.	PROGOK

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BiSS Identifier (0x78 to 0x7F, 0x78 to 0x7B read-only)								
0x78	Device ID - 0x4D ('M')							
0x79	Device ID - 0x48 ('H')							
0x7A	Revision - 0x59 ('Y')							
0x7B	Revision - 0x00 (")							
0x7C	-							CFGTOS
0x7D *z*	Manufacturer Revision - 0x00							
0x7E *z*	BiSS Device Manufacturer ID - 0x00							
0x7F *z*	BiSS Device Manufacturer ID - 0x00							

z: Register value programmable by zapping

*: Register value pre-programmed by iC-Haus

p: Register value write protected; can only be changed while V(VZAP)> Vt()hi

Table 5: Register layout

Hall Signal Processing ..... Page 11

GAING: Hall signal amplification range
GAINF: Hall signal amplification (1–20, log. scale)
GCC: Amplification calibration cosine
ENAC: Activation of amplitude control
VOSS: Offset calibration sine
VOSC: Offset calibration cosine
PRM: Energy saving mode
CIBM: Calibration of bias current
DPU Deactivation of NERR pull-up
HCLH Activation of high Hall clock pulse

RS422 Driver ..... Page 19

CFGDR: Driver property
TRIHL: Tristate high-side/low-side driver
CFGO: Configuration of output mode
CFGPROT: Write/read protection memory
ENSSI: Activation of SSI protocol

Sine/Digital Converter ..... Page 17

CFGRES: Resolution of sine digital converter
CFGZPOS: Zero point for position
CFGAB: Configuration of incremental output
CFGPOLE: No. of poles for commutation signals
CFGSU: Behavior during startup
CFGMTD: Frequency at AB
CFGDIR: Rotating direction reversal
CFGHYS: Hysteresis sine/digital converter
CFGCOM: Zero point for commutation

Test

TEST: Test mode
PROGZAP: Activation of programming routine

SENSOR PRINCIPLE

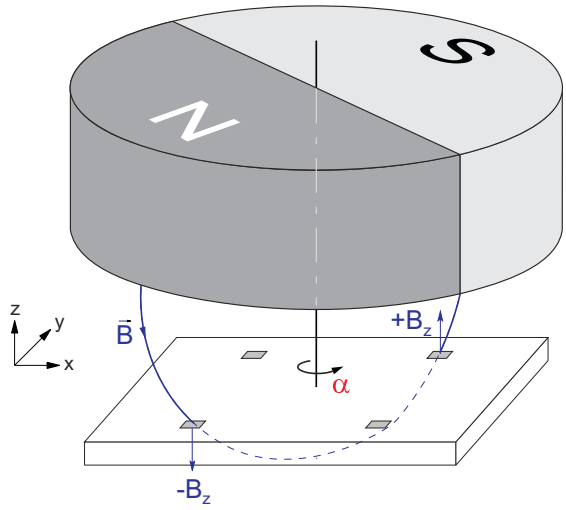


Figure 2: Sensor Principle

In conjunction with a rotating permanent magnet, the iC-MH module can be used to create a complete encoder system. A diametrically magnetized, cylindrical permanent magnet made of neodymium iron boron (NdFeB) or samarium cobalt (SmCo) generates optimum sensor signals. The diameter of the magnet should be within the range of 3 to 6 mm.

The iC-MH has four Hall sensors adapted for angle determination and to convert the magnetic field into a measurable Hall voltage. Only the z component of the magnetic field is evaluated, whereby the field lines pass through two opposing Hall sensors in the opposite direction. Figure 2 shows an example of field vectors. The arrangement of the Hall sensors is selected so that the mounting of the magnets relative to iC-MH is extremely tolerant. Two Hall sensors combined provide a differential Hall signal. When the magnet is rotated around the longitudinal axis, sine and cosine output voltages are produced which can be used to determine angles.

HALL SENSOR SIGNALS

The Hall sensors are placed in the center of the QFN28 package at 90° to one another and arranged in a circle with a diameter of 2 mm as shown in figure 3.

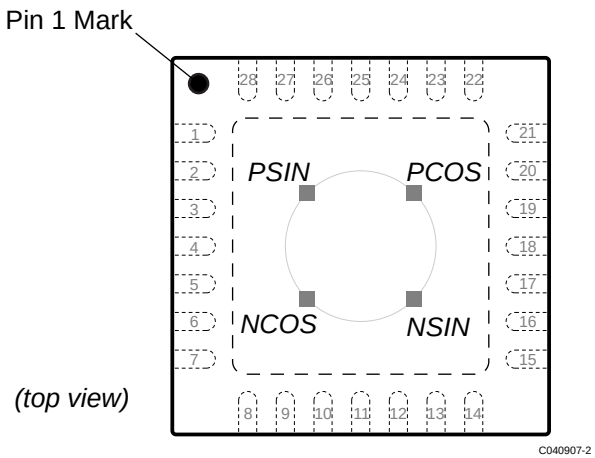


Figure 3: Position of the Hall sensors

When a magnetic south pole comes close to the surface of the package the resulting magnetic field has a positive component in the +z direction (i.e. from the top of the package) and the individual Hall sensors each generate their own positive signal voltage.

In order to calculate the angle position of a diametrically polarized magnet placed above the device a difference in signal is formed between opposite pairs of Hall sensors, resulting in the sine being $V_{SIN} = V_{PSIN} - V_{NSIN}$ and the cosine being $V_{COS} = V_{PCOS} - V_{NCOS}$. The zero angle position of the magnet is marked by the resulting cosine voltage value being at a maximum and the sine voltage value at zero.

This is the case when the south pole of the magnet is exactly above the PCOS sensor and the north pole is above sensor NCOS, as shown in figure 4. Sensors PSIN and NSIN are placed along the pole boundary so that neither generate a Hall signal.

When the magnet is rotated counterclockwise the poles then also cover the PSIN and NSIN sensors, resulting in the sine and cosine signals being produced as shown in figure 5. The signals are internal but can be made externally available for test purposes (see the description of iC-MH's calibration procedure).

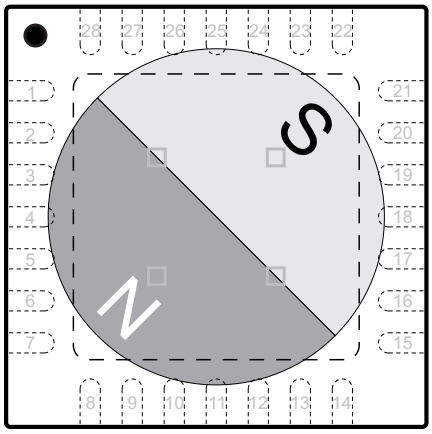


Figure 4: Zero position of the magnet

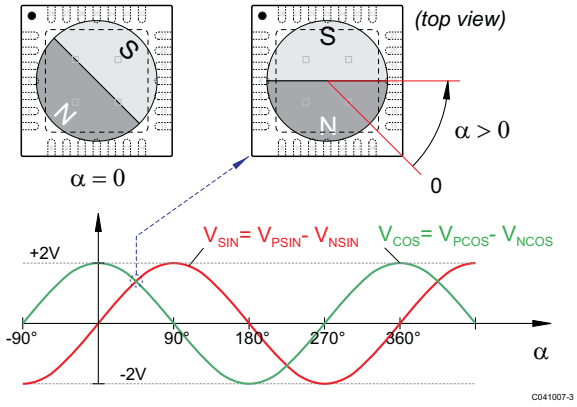


Figure 5: Pattern of the analog sensor signals with the angle of rotation

HALL SIGNAL PROCESSING

The iC-MH module has a signal calibration function that can compensate for the signal and adjustment errors. The Hall signals are amplified in two steps. First, the range of the field strength within which the Hall sensor is operated must be roughly selected. The first amplifier stage can be programmed in the following ranges:

GAING(1:0)	Addr. 0x00; bit 7:6
00	5-fold
01	10-fold
10	15-fold
11	20-fold

Table 6: Range selection for Hall signal amplification

The operating range can be specified in advance in accordance with the temperature coefficient and the magnet distance. The integrated amplitude control can correct the signal amplitude between 1 and 20 via another amplification factor. Should the control reach the range limits, a different signal amplification must be selected via GAING.

GAINF(5:0)	Addr. 0x00; bit 5:0
0x00...0x02	1,098
0x03	1,150
...	$exp(\frac{ln(20)}{64} \cdot GAINF)$
0x3E...0x3F	18,213

Table 7: Hall signal amplification

The second amplifier stage can be varied in an additional range. With the amplitude control (ENAC = '0') deactivated, the amplification in the GAINF register is used. With the amplitude control (ENAC = '1') activated, the GAINF register bits have no effect.

GCC(6:0)	Addr. 0x01; bit 6:0
0x00	1,000
0x01	1,0015
...	$exp(\frac{ln(20)}{2048} \cdot GCC)$
0x3F	1,0965
0x40	0,9106
...	$exp(-\frac{ln(20)}{2048} \cdot (128 - GCC))$
0x7F	0,9985

Table 8: Amplification calibration cosine

The GCC register is used to correct the sensitivity of the sine channel in relation to the cosine channel. The cosine amplitude can be corrected within a range of approximately ±10%.

ENAC	Addr. 0x01; bit 7
0	amplitude control deactivated
1	amplitude control activated

Table 9: Activation of amplitude control

The integrated amplitude control can be activated with the ENAC bit. In this case the differential signal amplitude is adjusted to 4 Vss and the values of GAINF have no effect here.

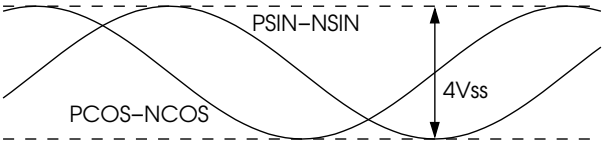


Figure 6: Definition of differential amplitude

After switch-on the amplification is increased until the setpoint amplitude is reached. The amplification is automatically corrected in case of a change in the input amplitude by increasing the distance between the magnet and the sensor, in case of a change in the supply voltage or in temperature. The sine signals are therefore always converted into high-resolution quadrature signals at the optimum amplitude.

VOSS(6:0) **VOSC(6:0)**	Addr. 0x02; bit 6:0 Addr. 0x03; bit 6:0
0x00	0 mV
0x01	1 mV
...	...
0x3F	63 mV
0x40	0 mV
0x41	-1 mV
...	...
0x7F	-63 mV

Table 10: Offset calibration for sine and cosine

Should there be an offset in the sine or cosine signal that, among other things, can also be caused by an inexactly adjusted magnet, then this offset can be corrected by the VOSS and VOSC registers. The output voltage can be shifted by ±63 mV in each case to compensate for the offset.

PRM	Addr. 0x03; bit 7
0	Energy-saving mode deactivated
1	Energy-saving mode activated

Table 11: Energy-saving mode

In the energy-saving mode the current consumption of the Hall sensors can be quartered. This also reduces the maximum rotating frequency by a factor of 4.

CIBM(3:0)	Addr. 0x04; bit 3:0
0x0	-40 %
...	...
0x8	0 %
0x9	+5 %
...	...
0xF	+35 %

Table 12: Calibration of bias current

In the test mode (TEST = 0x43) the internal bias current IBM can be measured on pin B vs pin VNA and changed via register CIBM to achieve a nominal value of 200 µA. CIBM is preprogrammed to the zapping ROM by iC-Haus and needs no further adjustment.

HCLH	Addr. 0x04; bit 7
0	250 kHz
1	500 kHz

Table 13: Activation of high Hall clock pulse

The switching-current Hall sensors can be operated at two frequencies. At 500 kHz the sine has twice the number of support points. This setting is of interest at high speeds above 30,000 rpm.

TEST MODES FOR SIGNAL CALIBRATION

For signal calibration iC-MH has several test settings which make internal reference quantities and the amplified Hall voltages of the individual sensors accessible at external pins A, B, Z and U for measurement purposes. This enables the settings of the offset (VOSS, VOSC), gain (GAING, GAINF) and amplitude ratio of the cosine to the sine signal (GCC) to be directly observed on the oscilloscope.

Test mode can be triggered by connecting pin VZAP to VPD and programming the TEST register (address 0x0E). The individual test modes are listed in the following table:

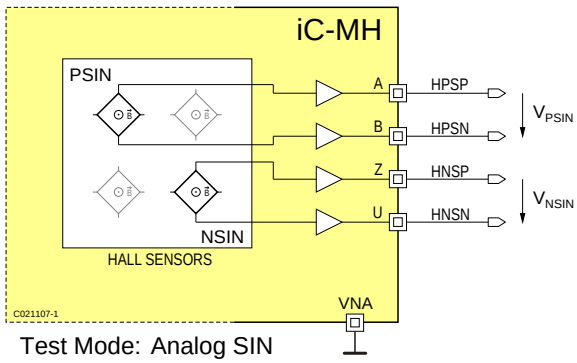
Output signals in test mode					
Mode	TEST	Pin A	Pin B	Pin Z	Pin U
Normal	0x00	A	B	Z	U
Analog SIN	0x20	HPSP	HPSN	HNSP	HNSN
Analog COS	0x21	HPCP	HPCN	HNCP	HNCN
Analog OUT	0x22	PSIN	NSIN	PCOS	NCOS
Analog REF	0x43	VREF	IBM	VBG	VOSR
Digital CLK	0xC0	CLKD			

Table 14: Test modes and available output signals

The output voltages are provided as differential signals with an average voltage of 2.5 V. The gain is determined by register values GAING and GAINF and should be set so that output amplitudes from the sine and cosine signals of about 1 V are visible.

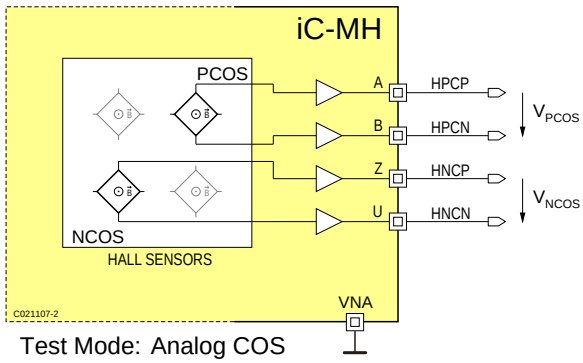
Test Modes Analog SIN and Analog COS
In these test modes it is possible to measure the signals from the individual Hall sensors independent of one another. The name of the signal is derived from the sensor name and position. **HPSP**, for example, is the (amplified) **H**all voltage of sensor **PS**IN at the **p**ositive signal path; similarly, **HNCN** is the **H**all voltage of sensor **NC**OS at the **n**egative signal path. The effective Hall voltage is accrued from the differential voltage between the positive and negative signal paths of the respective sensor.

Test Mode Analog OUT
In this test mode the sensor signals are available at the outputs as they would be when present internally for further processing on the interpolator. The interpolation accuracy which can be obtained is determined by the quality of signals V_{sin} and V_{cos} and can be influenced in this particular test mode by the calibration of the offset, gain and amplitude ratio.



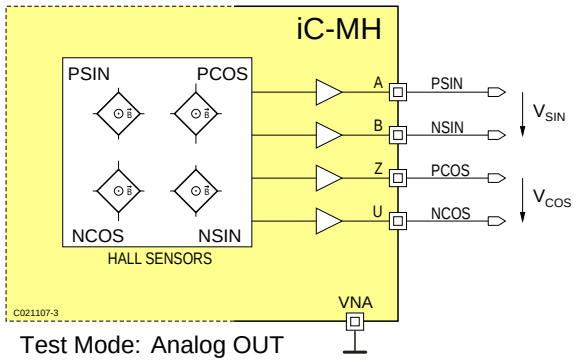
Test Mode: Analog SIN

Figure 7: Output signals of the sine Hall sensors in test mode Analog SIN



Test Mode: Analog COS

Figure 8: Output signals of the cosine Hall sensors in test mode Analog COS



Test Mode: Analog OUT

Figure 9: Differential sine and cosine signals in test mode Analog OUT

Test Mode Analog REF
In this mode various internal reference voltages are provided. VREF is equivalent to half the supply voltage (typically 2.5 V) and is used as a reference voltage for the Hall sensor signals. VBG is the internal bandgap

reference (1.24 V), with VOSR (0.5 V) used to generate the range of the offset settings. Bias current IBM determines the internal current setting of the analog circuitry. In order to compensate for variations in this current and thus discrepancies in the characteristics of the individual iC-MH devices (due to fluctuations in production, for example), this can be set within a range of -40% to +35% using register parameter CIBM. The nominal value of 200 µA is measured as a short-circuit current at pin B to ground. A CIBM preset value is programmed to the zapping ROM during chip test by iC-Haus and therefore no further customer programming is required.

Test Mode Digital CLK
If, due to external circuitry, it is not possible to measure IBM directly, by way of an alternative clock signal CLKD at pin A can be calibrated to a nominal 1 MHz in this test mode via register value CIBM.

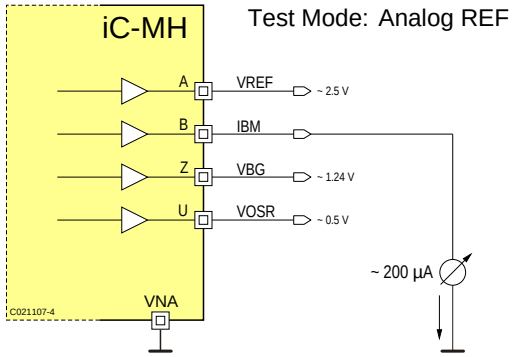


Figure 10: Setting bias current IBM in test mode Analog REF

CALIBRATION PROCEDURE

The calibration procedure described in the following applies to the optional setting of the internal analog sine and cosine signals and the mechanical adjustment of the magnet and iC-MH in relation to one another.

BIAS Setting
The internal bias setting via register CIBM compensates for device process tolerances and an optimum setting value is already pre-programmed into the zapping ROM by iC-HAUS during automatic chip test. Therefore, no further customer adjustments are needed for this setting. However, temporary changing the CIBM RAM content to extreme values can be used to imitate variations in device characteristic or to simulate changes in physical parameter like temperature or supply voltage (see chapter OTP Programming).

Mechanical Adjustment
iC-MH can be adjusted in relation to the magnet in test modes Analog SIN and Analog COS, in which the Hall signals of the individual Hall sensors can be observed while the magnet rotates.

In test mode Analog SIN the output signals of the sine Hall sensors which are diagonally opposite to one another are visible at pins A, B, Z and U. iC-MH and the magnet are then adjusted in such a way that differential signals V_{PSIN} and V_{NSIN} have the same amplitude and a phase shift of 180°. The same applies to test mode Analog COS, where differential signals V_{PCOS} and V_{NCOS} are calibrated in the same manner.

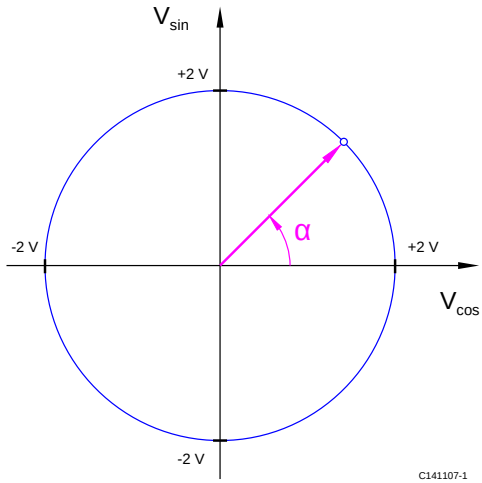


Figure 11: Ideal Lissajous curve

Calibration Using Analog Signals
In test mode Analog OUT as shown in Figure 5 the internal signals which are transmitted to the sine/digital converter can be tapped with high impedance. With a rotating magnet it is then possible to portray the differential signals V_{SIN} and V_{COS} as an x-y graph (Lissajous curve) with the help of an oscilloscope. In an ideal setup the sine and cosine analog values describe a perfect circle as a Lissajous curve, as illustrated in figure 11.

At room temperature and with the amplitude control switched off (ENAC = 0) a rough GAINING setting is selected so that at an average fine gain of GAINF = 0x20 (a gain factor of ca. 4.5) the Hall signal amplitudes are as close to 1 V as possible. The amplitude can then be

set more accurately by varying GAINF. Variations in the gain factor, as shown in figure 12, have no effect on the Lissajous curve, while enabling the angle information for the interpolator to be maintained.

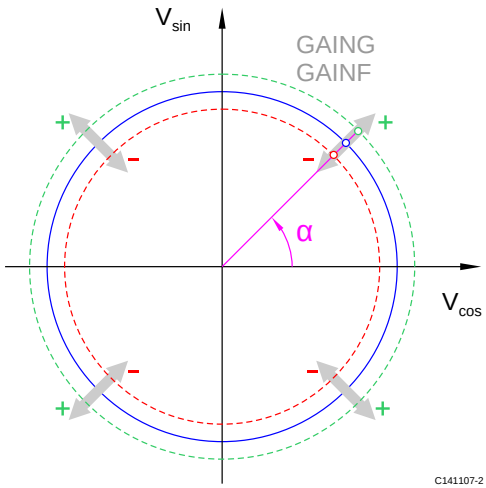


Figure 12: Effect of gain settings GAING and GAINF

Deviations of the observed Lissajous curve from the ideal circle can be corrected by varying the amplitude offset (register VOSS, VOSC) and amplitude ratio (register GCC). Changes in these parameters are described in the following figures 13 to 15. Each of these settings has a different effect on the interpolated angle value. A change in the sine offset thus has a maximum effect on the angle value at 0° and 180°, with no alterations whatsoever taking place at angles of 90° and 270°. When varying the cosine offset exactly the opposite can be achieved as these angle pairs can be set independent of one another. Setting the cosine/sine amplitude ratio does not change these angles (0°, 90°, 180° and 270°); however, inbetween values of 45°, 135°, 225° and 315° can still be influenced by this parameter.

Once calibration has been carried out a signal such as the one illustrated in figure 11 should be available.

In the final stage of the process the amplitude control can be switched back on (ENAC =1) to enable deviations in the signal amplitude caused by variations in the magnetic field due to changes in distance and temperature to be automatically controlled.

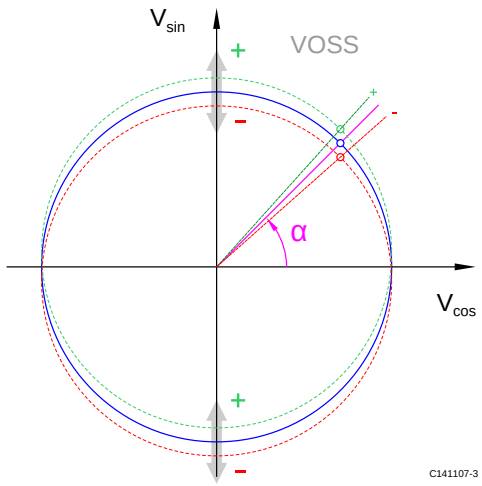


Figure 13: Effect of the sine offset setting

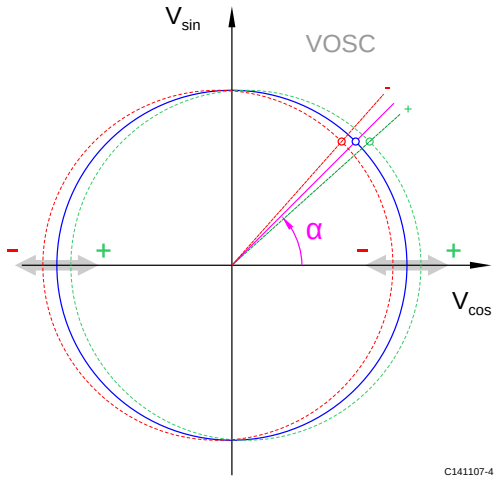


Figure 14: Effect of the cosine offset setting

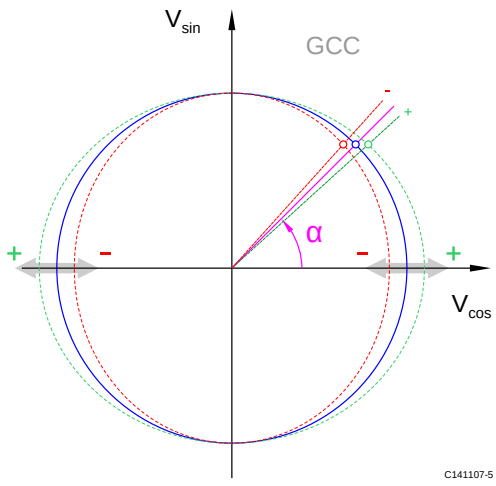


Figure 15: Effect of the amplitude ratio

Calibration Using Incremental Signals

If test mode cannot be used, signals can also be calibrated using the incremental signals or the values read out serially. In order to achieve a clear relationship between the calibration parameters which have an effect on the analog sensor signals and the digital sensor values derived from these, the position of the zero pulse should be set to ZPOS = 0 so that the digital signal starting point matches that of the analog signals.

At an incremental resolution of 8 edges per revolution (CFGRES = 0x1) those angle values can be displayed at which calibration parameters VOSS, VOSC and GCC demonstrate their greatest effect. When rotating the magnet at a constant angular speed the incremental signals shown in figure 16 are achieved, with which the individual edges ideally succeed one another at a temporal distance of an eighth of a cycle (a 45° angle distance). Alternatively, the angle position of the magnet can also be determined using a reference encoder, rendering an even rotational action unnecessary and allowing calibration to be performed using the available set angle values.

The various possible effects of parameters VOSS, VOSC and GCC on the flank position of incremental signals A and B are shown in figure 16. Ideally, the distance of the rising edge (equivalent to angle positions of 0° and 180°) at signal A should be exactly half a period (PER). Should the edges deviate from this in distance, the offset of the sine channel can be adjusted using VOSS. The same applies to the falling edges of the A signal which should also have a distance of half a period; deviations can be calibrated using the offset of cosine parameter VOSC. With parameter GCC the distance between the neighboring flanks of signals A and B can then be adjusted to the exact value of an eighth of a cycle (a 45° angle distance).

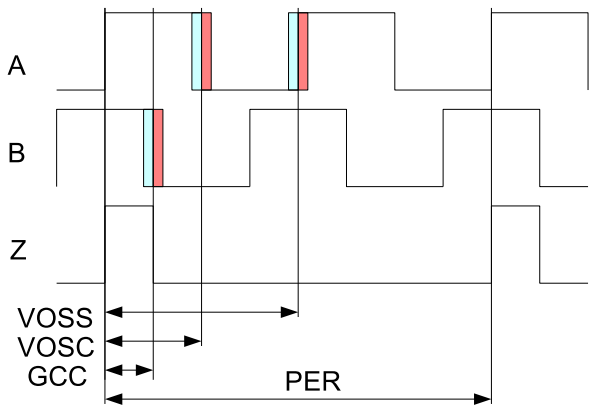


Figure 16: Calibration using incremental signals

SINE/DIGITAL CONVERTER

The iC-MH module integrates two separate sine/digital converters. A high-resolution 12-bit converter for the ABZ incremental signals can be programmed in broad ranges of the resolution and generate quadrature signals even at the highest speed and resolution. The converter operates for the commutation signals independently of this and can be set in the zero point separately from the quadrature converter. This enables the commutation at other angles based on the index track Z.

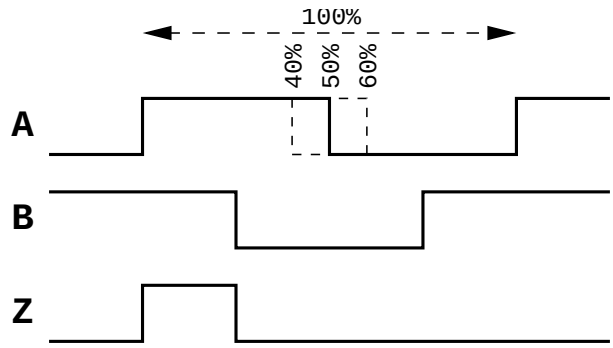


Figure 17: ABZ signals and relative accuracy

CFGRES(7:0)	Addr. 0x06; bit 7:0
0x0	1
0x1	2
...	...
0x7e	127
0x7f	128
0x80	256
0x81	512
0x82	1024

Table 15: Programming interpolation factor

The resolution of the 12-bit converter can virtually be set as desired. Any resolution can be set up to an interpolation factor of 128, i.e. 512 edges per rotation. At higher resolutions, only the binary resolutions can be set, i.e. 256, 512 and 1024. In the highest resolution with an interpolation factor of 1024, 4096 edges per rotation are generated and 4096 angular steps can be differentiated. Even in the highest resolution, the absolute position can be calculated in real time at the maximum speed. After the resolution is changed, a module reset is triggered internally and the absolute position is recalculated.

CFGAB(1:0)	Addr. 0x08; bit 1:0
0x0	A and B not inverted
0x1	B inverted, A normal
0x2	A inverted, B normal
0x3	A and B inverted

Table 16: Inversion of AB signals

The incremental signals can be inverted again independently of the output drivers. As a result, other phase angles of A and B relative to the index pulse Z can be generated. The standard is A and B *high* level for the zero point, i.e. Z is equal to *high*.

Figure 17 shows the position of the incremental signals around the zero point. The relative accuracy of the edges to each other at a resolution setting of 10 bit is better than 10%. This means that, based on a period at A or B, the edge occurs in a window between 40% and 60%.

CFGHYS(1:0)	Addr. 0x08; bit 7:6
0x0	0,17°
0x1	0,35°
0x2	0,7°
0x3	1,4°

Table 17: Programming angular hysteresis

With rotating direction reversal, an angular hysteresis prevents multiple switching of the incremental signals at the reversing point. The angular hysteresis corresponds to a slip which exists between the two rotating directions. However, if a switching point is approached from the same direction, then the edge is always generated at the same position on the output. The following figure shows the generated quadrature signals for a resolution of 360 edges per rotation (interpolation factor 90) and a set angular hysteresis of 1.4°.

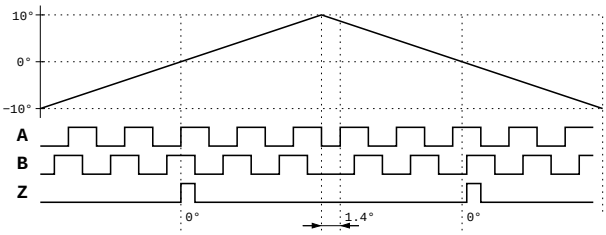


Figure 18: Quadrature signals for rotating direction reversal (hysteresis 1.4°)

At the reversal point at +10°, first the corresponding edge is generated at A. As soon as an angle of 1.4° has been exceeded in the other direction in accordance with the hysteresis, the return edge is again generated at A first. This means that all edges are shifted by the same value in the rotating direction.

CFGZPOS(7:0)	Addr. 0x07; bit 7:0
0x0	0°
0x1	1,4°
0x2	2,8°
...	$\frac{360}{256}$·CFGZPOS
0xff	358,6°

Table 18: Programming AB zero position

The position of the index pulse Z can be set in 1.4° steps. An 8-bit register is provided for this purpose, which can shift the Z pulse once over 360°.

CFGMTD2	**CFGMTD**	**Minimum edge spacing**	
0	0	500 ns	max. 500 kHz at A
0	1	125 ns	max. 2 MHz at A
1	0	8 µs	max. 31.25 kHz at A
1	1	2 µs	max. 125 kHz at A

Table 19: Minimum edge spacing

The CFGMTB register defines the time in which two consecutive position events can be output. The default is a maximum output frequency of 500 kHz on A. This means that at the highest resolution, speeds of 30,000 rpms can still be correctly shown. In the setting with an edge spacing of 125 ns, the edges can be generated even at the highest revolution and the maximum speed. However, the counter connected to the module must be able to correctly process all edges in this case. The settings with 2 µs and 8 µs can be used for slower counters. It should be noted then, however, that at higher resolutions the maximum rotation speed is reduced.

CFGDIR	Addr. 0x08; bit 5
0	Rotating direction CCW
1	Rotating direction CW

Table 20: Rotating direction reversal

The rotating direction can easily be changed with the bit CFGDIR. When the setting is CCW (counter-clockwise, CFGDIR = ’0’) the resulting angular position values will increase when rotation of the magnet is performed as shown in figure 5. To obtain increasing angular position values in the CW (clockwise) direction, CFGDIR then has to be set to ’1’.

The internal analog sine and cosine signals which are available in test mode are not affected by the setting of CFGDIR. They will always appear as shown in figure 5.

CFGSU	Addr. 0x08; bit 3
0	ABZ output "111" during startup
1	AB instantly counting to actual position

Table 21: Configuration of output startup

Depending on the application, a counter cannot bear generated pulses while the module is being switched on. When the supply voltage is being connected, the current position is determined first. During this phase the quadrature outputs are constantly set to "111" in the setting CFGSU = ’0’. In the setting CFGSU = ’1’, edges are generated at the output until the absolute position is reached. This enables a detection of the absolute position with the incremental interface.

The converter for the generation of the commutation signals can be configured for two and four-pole motors. Three rectangular signals each with a phase shift of 120° are generated. With two-pole commutation, the sequence repeats once per rotation. With a four-pole setting, the commutation sequence is generated twice per rotation.

CFGPOLE	Addr. 0x8; bit 1
0	2-pole commutation
1	4-pole commutation

Table 22: Commutation

The zero position of the commutation, i.e. the rising edge of the track U, can be set as desired over a rotation. Here 192 possible positions are available. Values above 0xC0 are the mirrored positions from 0x70.

CFGCOM(7:0)	Addr. 0x09; bit 7:0
0x00	0°
0x01	1,875°
...	$\frac{360°}{192}$· CFGCOM
0xBF	358,125°

Table 23: Commutation

OUTPUT DRIVERS

Six RS422-compatible output drivers are available, which can be configured for the incremental signals and commutation signals. The following table on the CFGO register bits provides an overview of the possible settings.

CFGO(1:0)	Addr. 0x05; bit 5:4
00	Incremental Diff ABZ (U=NA, V=NB, W=NZ)
01	Incr. ABZ + Comm UVW
10	Commutation Diff UVW (A=NU, B=NV, Z=NW)
11	Incr. ABZ + AB4 (U=A4, V=B4, W=0)

Table 24: Configuration of output drivers

In the differential incremental mode (CFGO = '00', figure 19), quadrature signals are available on pins A, B and Z. The respective inverted quadrature signals are available on the pins U, V and W. As a result, lines can be connected directly to the module. Another configuration of the incremental signals is specified in the section "Sine/Digital Converter".

With CFGO = '01' (figure 20) the ABZ incremental signals and the UVW commutation signals are available on the six pins. As long as the current angular position is not yet available during the startup phase, all commutation signals are at the low level.

With CFGO = '10', the third mode (figure 21) is available for transferring the commutation signals via a differential line. The non-inverted signals are on the pins U, V and W, the inverted signals on A, B and Z.

The ABZ quadrature signals with an adjustable higher resolution and quadrature signals with one period per rotation are available in the fourth mode (figure 22). Four segments can be differentiated with the pins U and V. This information can be used for an external period counter which counts the number of scanned complete rotations.

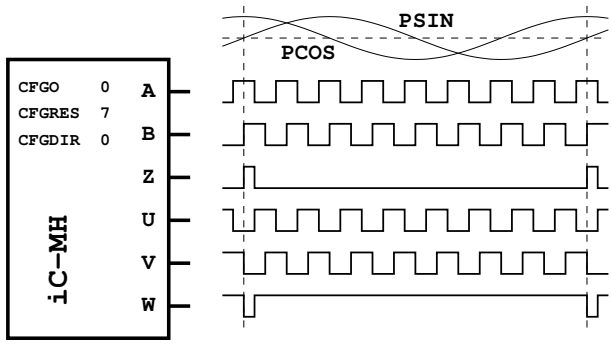


Figure 19: ABZ differential incremental signals

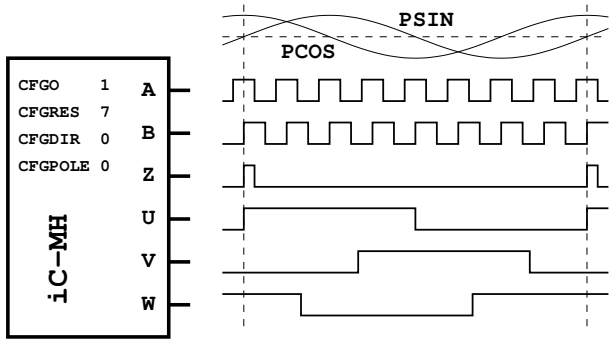


Figure 20: ABZ incremental/UVW commutation signals

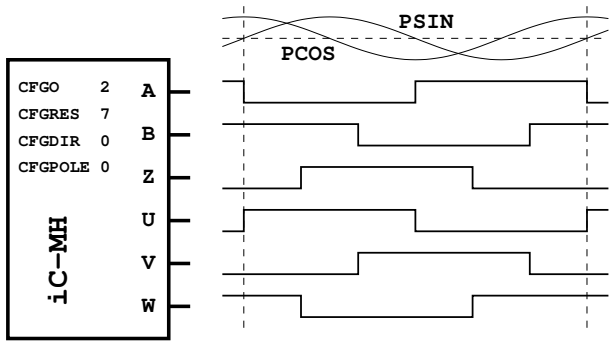


Figure 21: UVW differential commutation signals

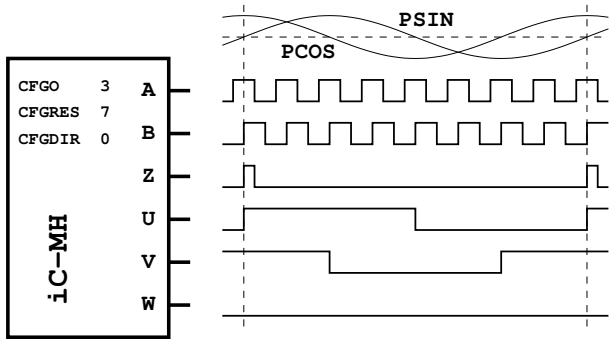


Figure 22: ABZ incremental signals/period counter

The property of the RS422 driver of the connected line can be adjusted in the CFGDR register.

CfgDR(1:0)	Addr. 0x07; bit 1:0
00	10 MHz 4 mA (default)
01	10 MHz 60 mA
10	300 kHz 60 mA
11	3 MHz 20 mA

Table 25: Driver property

Signals with the highest frequency can be transmitted in the setting CFGDR = ’00’. The driver capability is at least 4 mA, however it is not designed for a 100 Ω line. This mode is ideal for connection to a digital input on the same assembly. With the setting CFGDR = ’01’ the same transmission speed is available and the driver power is sufficient for the connection of a line over a short distance. Steep edges on the output enable a high transmission rate. A lower slew rate is offered by the setting CFGDR = ’10’, which is excellent for longer lines in an electromagnetically sensitive environment. Use of the setting CFGDR = ’11’ is advisable at medium transmission rates with a limited driver capability.

TRIHL	Addr. 0x07; bit 3:2
00	Push-Pull Output Stage
01	Lowside Driver
10	Highside Driver
11	Tristate

Table 26: Tristate Register

The drivers consist of a push-pull stage in each case with low-side and high-side drivers which can each be activated individually. As a result, open-drain outputs with an external pull-up resistor can also be realized.

BISS INTERFACE

The BiSS interface with BiSS C protocol is a serial bidirectional interface used to read out the absolute position and flags and to parameterize the module. All BiSS communications are CRC secured. For a detailed description, see separate BiSS C protocol specification *www.biss-interface.com*.

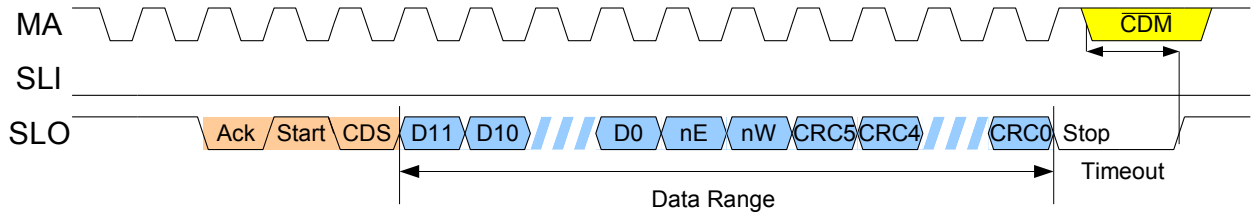


Figure 23: BiSS Interface Protocol Frame (Single Cycle Data SCD)

The sensor sends a fixed cycle start sequence containing the acknowledge, start and control bit followed by the binary 12 bit sensor data. At lower resolution settings the data word contains leading zeros. The low-active error bit nE at ’0’ indicates an error which can be further identified by reading the status register 0x77. The following bit nW is always at ’1’ state. Following the 6 CRC bits the data of the next sensors, if available, are presented. Otherwise the BiSS master stops generating clock pulse on the MA line an the sensor runs into a timeout, indicating the end of communication.

Serial Protocol Content	BiSS C
Cycle Start Sequence	Ack/Start/CDS
Length of Sensor Data	12 bit + nERR + nWARN
CRC Polynomial	0x43 = 0b1000011
CRC Transmission	inverted transmission
Max. Data Rate	10 MHz

Table 27: BiSS C Protocol

ENSSI	Addr. 0x05; bit 7
0	BiSS C protocol
1	SSI protocol

Table 28: Activation of SSI protocol

In the SSI mode the absolute position is output with 13 bits according to the SSI standard. However, in the SSI

mode it is not possible to vary the parameter set. The data is transmitted as reduced Gray code, e.g. after converting into binary code, the data range is symmetrical to the center of the number string. For example, with a set resolution of 360 data values between 76 and 435 are transmitted.

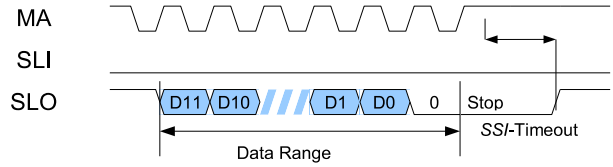


Figure 24: SSI protocol, data GRAY-coded

The register range 0x00 to 0x0F is equivalent to the settings with which the IC can be parameterized. The settings directly affect the corresponding switching parts. It is important to note that test register 0x0E can only be written to when pin VZAP is connected to VPD. When VPD > 6 V, write access to the test register is ignored. Register 0x0F can be configured at potentials V(VZAP) > Vt(VZAP)hi.

The register range 0x10 to 0x1F is read-only and reflects the contents of the integrated zapping diodes. Following programming the data can be verified via these addresses. After the supply voltage is connected, the contents of the zapping diodes are copied to the RAM area 0x00 to 0x0F. Then the settings can be overwritten via the BiSS interface. Overwriting is not possible if the CFGPROT bit is set.

Errors in the module are signaled via the error message output NERR. This open-drain output signals an error if the output is pulled against VND. If the error condition no longer exists, then the pin is released again after a waiting time of approximately 1 ms. If the integrated pull-up resistor is deactivated with DPU = '1', then an external resistor must be provided. With DPU = '0' it brings the pin up to the high level again.

DPU	Addr. 0x04; bit 6
0	Pull-up activated
1	Pull-up deactivated

Table 29: Activation of NERR pull-up

With the BiSS profile ID, the data format of the sensor can be requested. Reading the BiSS profile ID results 0x2C in address 0x43, which identifies BiSS Profile BP1 and two most significant bits of the multiturn resolution, what is here always '00'. Reading the register 0x43 contains the three least significant bits of the multiturn resolution, what is here always '000' and five bits of the singleturn resolution as is the data length DLEN of the transmitted sensor data in accordance with the set resolution. The sensor data is transmitted right-justified and filled with preceding zeros on smaller resolutions than 12 bit. The following table shows the data length according to the resolution.

DLEN	Addr. 0x43; bit 3:0
2	CFGRES = '00000000', 4
3	CFGRES = '00000001', 8
4	CFGRES = '0000001x', 12 to 16
5	CFGRES = '000001xx', 20 to 32
6	CFGRES = '00001xxx', 36 to 64
7	CFGRES = '0001xxxx', 68 to 128
8	CFGRES = '001xxxxx', 132 to 256
9	CFGRES = '01xxxxxx', 260 to 512
10	CFGRES = '10000000', 1024
11	CFGRES = '10000001', 2048
12	CFGRES = '10000010', 4096

Table 30: Data length

N.B. With CFGRES = '10000010', 4096 and using BiSS protocol the device provides a BiSS Profile ID 0x2C 0x0C (0x2C in address 0x42 and 0x0C in address 0x43) that is "BiSS Profile BP1 Standard Rotary Encoder" conform.

The status register provides information on the status of the module. There are 5 different errors that can be signaled. Following unsuccessful programming of the zapping diodes, the bit PROGERR is set. If an attempt is made to read the current position via the BiSS Interface during the startup phase, an error is signaled with ERRSDATA, as the actual position is not yet available. The ERRAMAX bit is output to signal that the amplitude is too high, while the ERRAMIN bit signals an amplitude which is too low, caused, for example, by too great a distance to the magnet. If the NERR pin is pulled against VND outside the module, this error is also signaled via the BiSS Interface on the low active status flag nERR in the SCD. The ERREXT bit is then equal to '1'. The error bits are reset again after the status register is read out at the address 0x77. The error bit in the data word is then also read in the next cycle as '0'.

CFGTOS	CFGTOB	Timeout
0	0	16 µs
1	0	2 µs
x	1	2 µs

Table 31: BiSS timeout for sensor data (SCD)

The BiSS timeout can be programmed to a shorter value with the CFGTOS bit. However, this setting is reset to the default value 16 µs again following a reset.

The BiSS timeout can be permanently programmed for faster data transmission with the CFGTOB register via a zapping diode. Resetting to slower data transmission is then not possible.

The registers 0x78 to 0x7F are reserved for the BiSS Identifier. The BiSS Identifier identifies the device manufacturer and the type of BiSS module. The registers 0x7D to 0x7F are alterable and programmable to provide a manufacturer individual BiSS Device Manufacturer ID and revision.

OTP PROGRAMMING

Once the RAM parameters have been configured these settings can be written to the underlying zapping ROM.

As a requirement for programming, a zapping voltage (nominal 7 V, see item 806 in the electrical characteristics for tolerances) has to be provided via pin VZAP and VNA. Also, the device is not in the test mode, e.g. the test register has to be set to TEST = 0x00. Temporary, CIBM has to be set to 0x0.

Then the internal programming algorithm for the ZAP diodes is started by setting the bit PROGZAP. When programming routine terminates, the PROGZAP bit resets automatically. Successful programming is then indicated by the status register (address 0x77) when bit PROGOK is set and PROGERR is unset - otherwise, an error situation has occurred (like missing zapping voltage).

PROGOK	PROGERR	Corrective actions
0	0	Set VZAP to 7 V
0	1	Set VZAP to 7 V and TEST = 0x00
1	0	Zapping was successful
1	1	Undefined state

Table 32: Zapping results

The following sequence has to be performed according to Fig. 25 to verify zapping ROM content:

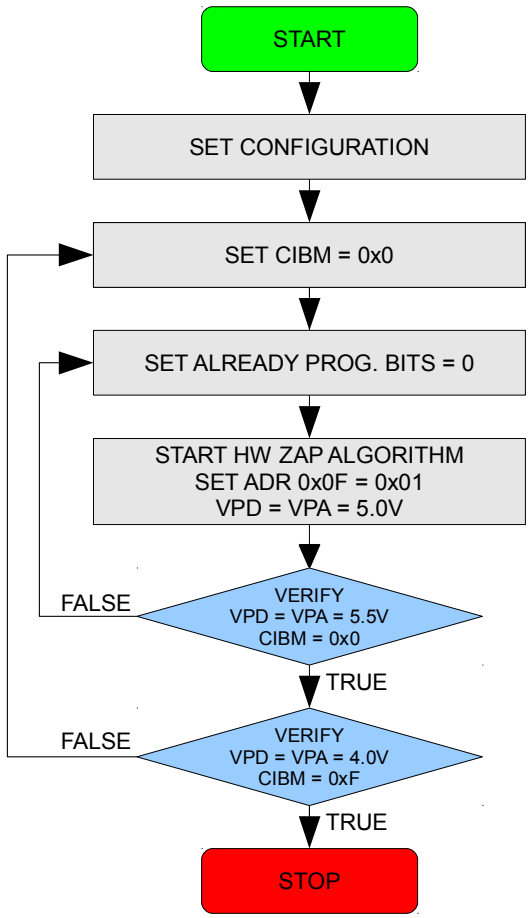


Figure 25: Programming algorithm

CIBM is first set to 0x0 at address 0x04 and the hardware programming algorithm started by bit PROGZAP. After programming, as a first verification step, set CIBM back to 0x0 and change VPD, VPA to a high supply voltage of 5.5 V. Then read-out the ROM value which should not differ from the intended programmed configuration. (In case of differences, a new programming run is needed.) The second verification step requires setting CIBM to its maximum value of 0xF and changing VPD, VPA to a low supply voltage of 4.0 V, again followed by a read out of the ROM. If both kind of readouts at these extreme settings are showing no deviations from the expected values, the the verification process has completed.

For reliable ROM writing, a low impedance connection path as shown in figure 26 must be established for the VZAP blocking capacitor (about 100 nF) between pin VZAP and pin VNA to ensure stable VZAP voltage during programming. A further capacitor of 10 µF which may be located externally (e.g. on the programming board) is recommended for additional blocking purpose.

When a register bit has to be programmed once again after verifying failed, already programmed register bits need not be programmed and the corresponding RAM register bits have to be set to 0.

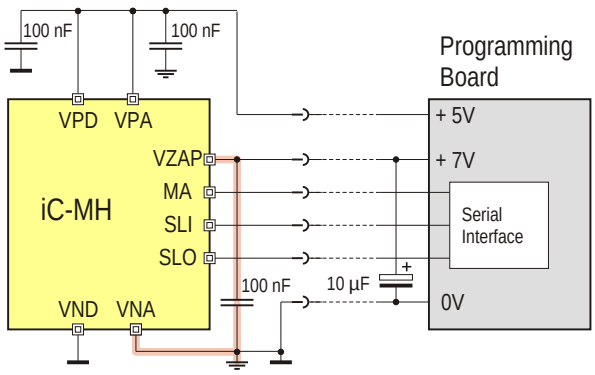


Figure 26: Recommended setup for external programming. A short low impedance path (shown in light red) must be provided directly from pin VZAP to pin VNA

A typical PCB layout may look like the one shown in figure 27.

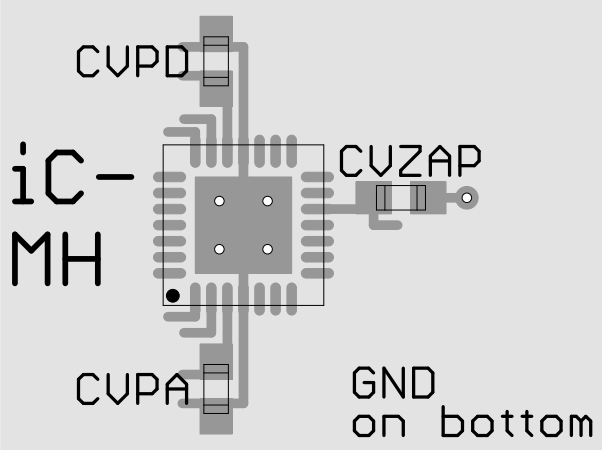


Figure 27: Example PCB layout showing low impedance connection of capacitors to supply voltages (VPA, VPD, VZAP) and common ground

The ROM content may be protected against further changes by register CFGPROT.

CFGPROT	Addr. 0x05; bit 6
0	no protection
1	write/read protection

Table 33: Write/read protection of configuration

With CFGPROT = '0', the registers at the addresses 0x00 to 0x0F and 0x78 to 0x7F are readable and writeable. The addresses 0x10 to 0x1F and 0x77 are read-only. With CFGPROT = '1', all registers except the addresses 0x7B and 0x7C are write-protected; the addresses 0x77 to 0x7F are readable, while all others are read-protected.

DESIGN REVIEW: Notes on Chip Functions

iC-MH Y		
No.	Function, Parameter/Code	Description and Application Hints
		No further notes at time of printing.

Table 34: Notes on chip functions regarding iC-MH chip release Y.

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
C1	2014-12-10	ELECTRICAL CHARACTERISTICS	Item 003 max. value changed to 17 mA	5
		ELECTRICAL CHARACTERISTICS	Item 603 typical value 10% introduced, min./max. values changed to 15%	6
		ELECTRICAL CHARACTERISTICS	Item 710 max. values changed to 65 µA	6

Rel.	Rel. Date*	Chapter	Modification	Page
C2	2016-12-09	ELECTRICAL CHARACTERISTICS	Item 203 max value changed from 0.91 to 0.92 Item 205 min value changed from 1.1 to 1.0 Item 206 min value changed from 4.9 to 4.8 Item 404 min value changed from 3.7 to 3.65 Item 407 min value changed from 480 to 475 Item 502 min value changed from 14 to 13.5 Item 709 min value changed from 150 to 140 Item 803 min value changed from 150 to 140 Item 804 min value changed from 0.8 to 0.7 Item 904 min value changed from 150 to 140 Item 905 min value changed from -750 to -800	5,6
		BiSS Interface	BiSS Profile BP1 conformity with DLEN = 12 and BiSS. BiSS Identifier updated.	21
			Serial Interface updated to BiSS Interface and BiSS C protocol.	all
		BISS INTERFACE	Headline changed from "Serial Interface" to "BISS INTERFACE"	20
		DESCRIPTION	BiSS User Agreement ”BUA” added	2
		BLOCK DIAGRAM	block diagram with new fill colour	1
		PACKAGES	package view with new style	1
		PACKAGING INFORMATION	Package drawing and suggested footprint added	3
		ELECTRICAL CHARACTERISTICS	Item 205, 206 old parameter names MINERR, MAXERR renamed to ERRAMIN, ERRAMAX	5
		REGISTER MAP	Footnote (*) added indicating register values pre-programmed by iC-Haus (affecting addresses 0x02, 0x04)	9
		SENSOR PRINCIPLE	Figure 2 with new style	10
		HALL SENSOR SIGNALS	Headline changed from "POSITION OF THE HALL SENSORS and THE ANALOG SENSOR SIGNAL" to "HALL SENSOR SIGNALS"	10
		HALL SENSOR SIGNALS	Figure 4 and 5 with new style	11
		HALL SIGNAL PROCESSING	Note on default factory setting of bias register CIBM parameter	12
		CALIBRATION PROCEDURE	Note on default factory setting of bias register CIBM parameter	14
		OUTPUT DRIVERS	Figures 19 to 22 revised - settings of parameters CFGO, CFGRES, CFGDIR and CFGPOLE added	19
		OTP PROGRAMMING	Chapter revised, Figures 25 and 26 modified, Fig. 27 new introduced	23,24
		DESIGN REVIEW: Notes on Chip Functions	Design Review introduced	24

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* Release Date format: *YYYY-MM-DD*

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Type	Package	Options	Order Designation
iC-MH	QFN28		iC-MH QFN28

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