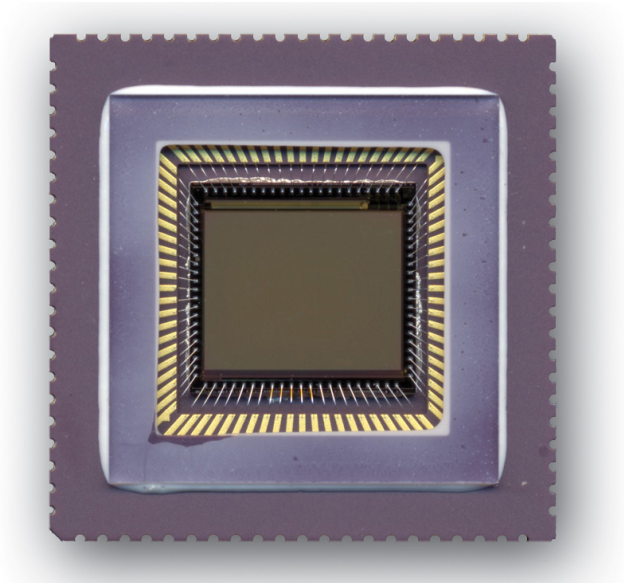
IBIS4-1300

1.3 MPxl Rolling Shutter CMOS Image Sensor



Overview

The IBIS4-1300 is a digital CMOS active pixel image sensor with SXGA format.

Due to a patented pixel configuration a 60% fill factor and 50% quantum efficiency are obtained. This is combined with an on-chip double sampling technique to cancel fixed pattern noise.

Features

- SXGA resolution: 1280 x 1024 pixels
- High sensitivity 20 $\mu V/e^-$
- High fill factor 60%
- Quantum efficiency > 50% between 500 and 700 nm.
- 20 noise electrons = 50 noise photons
- Dynamic range: 69 dB (2750:1) in single slope operation
- Extended dynamic range mode (80…100 dB) in double slope integration
- On-chip 10 bit, 10 mega Samples/s ADC
- Programmable gain & offset output amplifier
- 4:1 sub sampling viewfinder mode (320x256 pixels)
- Electronic shutter
- 7 x 7 μm^2 pixels
- Low fixed pattern noise (1% Vsat p/p)
- Low dark current: 344 pA/cm^2
- (1055 electrons/s, 1 minute auto saturation)
- RGB or monochrome
- Digital (ADC) gamma correction

Part Number

Part Number	Package	Glass lid	RGB/B&W
CYII4SC1300AA-QSC	LCC	S8612	RGB Bayer pattern
CYII4SM1300AA-QDC	LCC	D263	B&W

TABLE OF CONTENTS

Overview 1
Features 1
Part Number 1
Architecture of the image sensor 4
Image sensor core - focal plane array 5
Output amplifier 11
Analog to digital converter 17
ADC timing 18
Operation of the image sensor 20
Set configuration & pulse timing 20
Illumination control 26
"Double slope" or "High-dynamic range" mode 27
Electrical parameters 28
Pin configuration 29
Pin list 29
Bonding pad geometry for the IBIS4-1300 31
Package 33
Cover glass 33
Ordering Information 35
FAQ 35
Temperature dependence of dark signal 35
Useful range of "double slope" 35
Skipping rows or columns 36
Disclaimer 36
Document History Page 37

LIST OF FIGURES

Block diagram 4
Architecture of the image sensor core 4
Pixel selection - principle 5
Spectral response * fill factor of the IBIS4-1300 pixels 7
Near infrared spectral response 8
IBIS4-1300 response curve - two pixels - lowest gain setting (0000) 9
Output amplifier architecture 12
Offset adjustment: fast offset adjustment mode 13
Slow offset adjustment mode 13
Output amplifier DC gain 15
Output amplifier bandwidth for different gain settings 16
Typical transfer characteristic of the output amplifier (no clipping, Voffset = 2 V, input signal during offset adjustment is 1.2 V) 16
Suggested circuit for high and low references of DAC 17

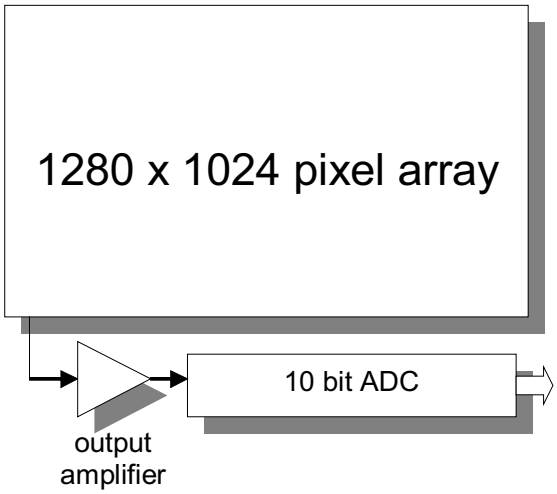
ADC timing 18
Linear and non-linear ADC conversion characteristic 19
Typical operation mode (readout of a frame) 20
Timing of Y shift registers (for row selection) 22
End-of-scan pulse 22
Timing constraints for row readout initialization (blanking time) 23
Pulse on 'CALIB_F'& 'UNITYGAIN' to be given once per frame, or on CALIB_S once per line 24
Timing of X shift register and pixels read-out 25
Pixel timing 25
Pulse sequence used in IBIS4 breadboard v. jan 2000 26
Schematic representation of the curtain type electronic shutter 26
response curve of the pixels in dual slope integration 27
Linear long exposure time 27
Linear short exposure time 28
Double slope integration 28
Pin layout and package, top view 33
Transmission characteristics of the BG39 glass used as NIR cut-off filter for the FUGA1000 color image sensors 34
Transmission characteristics of the D263 glass used as protective cover for the IBIS4-1300 monochrome image sensors 34

LIST OF TABLES

Optical & electrical characteristics 5
Calculation of sensitivity in [V/lx.s] 8
Pins of the image sensor core 10
Summary of output amplifier specifications 11
Pins involved in output amplifier circuitry 14
DC gain of output amplifier for different gain settings 15
ADC specifications 17
Pins of the ADC 18
Co-ordinate of the row or column selected by the Y/X shift registers after a # clock periods in viewfinder mode and full image mode 21
Timing constraints on row initialization pulses sequence 23
FillFactory and Cypress part numbers 35

Architecture of the image sensor

Block diagram



The IBIS4-1300 is an SXGA CMOS image sensor. The chip is composed of 3 modules: an image sensor core, a programmable gain output amplifier, and an on-chip 10 bit ADC.

Figure 1. Architecture of the image sensor core

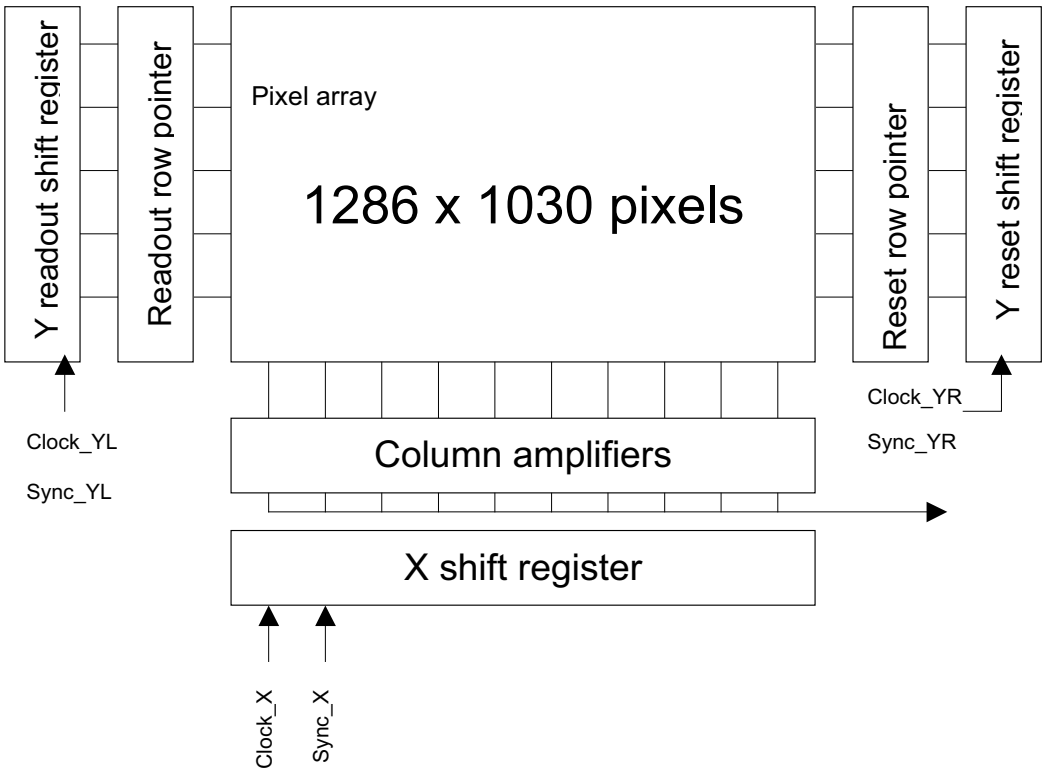


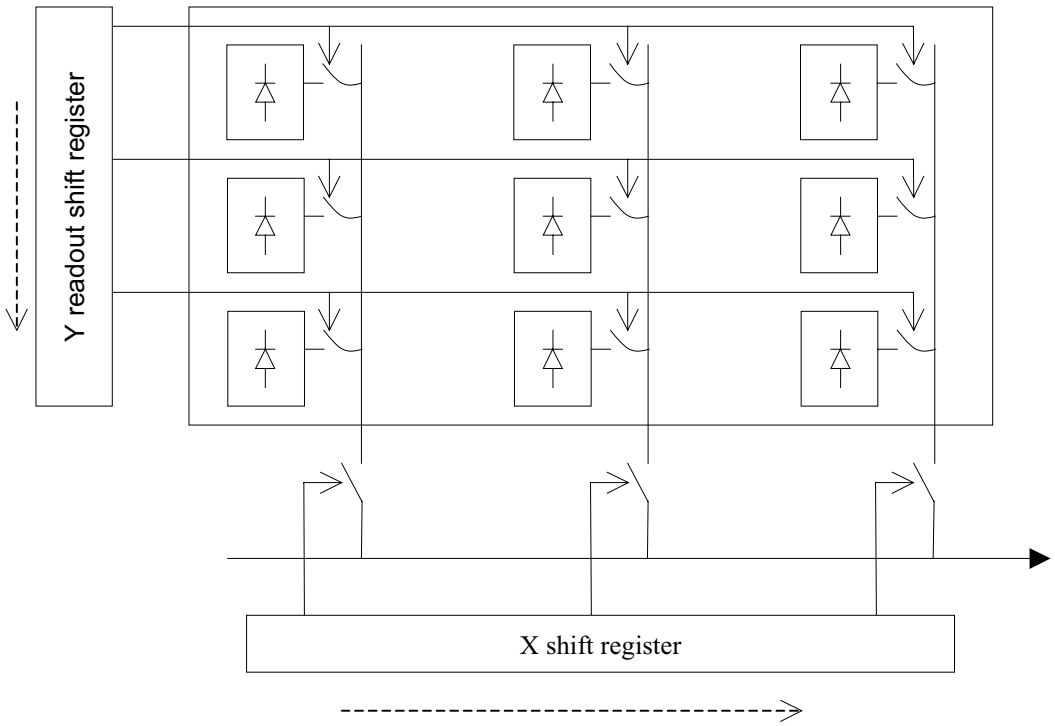
Image sensor core - focal plane array

Figure 1. shows the architecture of the image sensor core.

The core of the sensor is the pixel array with 1280 x 1024 (SXGA) active pixels.

The name 'active pixels' refers to the amplifying element in each pixel. This type of pixels offer a high light sensitivity combined with low temporal noise. The actual array size is 1286 x 1030 including the 6 dummy pixels in X and Y. Although the dummy pixels fall outside the SXGA format, their information can be used e.g. for color filter array interpolation.

Figure 2. Pixel selection - principle



Next to the pixel array there are two Y shift registers, and one X shift register with the column amplifiers. The shift registers act as pointers to a certain row or column. The Y readout shift register accesses the row (line) of pixels that is currently readout. The X shift register selects a particular pixel of this row. The second Y shift register is used to point at the row of pixels that is reset. The delay between both Y row pointers determines the integration time -thus realizing the electronic shutter.

A clock and a synchronization pulse control the shift registers. On every clock pulse, the pointer shifts one row/column further. A sync pulse is used to reset and initialize the shift registers to their first position.

The smart column amplifiers compensate the offset variations between individual pixels. To do so, they need a specific pulse pattern on specific control signals before the start of the row readout.

Table 1. summarizes the optical and electrical characteristics of the image sensor. Some specifications are influenced by the output amplifier gain setting (e.g. temporal noise, conversion factor,...). Therefore, all specifications are referred to an output amplifier gain equal to 1.

Table 1. optical & electrical characteristics

Pixel characteristics	
Pixel structure	3-transistor active pixel
Photodiode	High fill factor photodiode
Pixel size	7 x 7 μm^2
Resolution	1286 x 1030 pixels SXGA plus 6 dummy rows & columns
Pixel rate with on-chip ADC	Nominal 10 MHz (note 1) (note 2)
Frame rate with on-chip ADC	About 7 full frames/s at nominal speed

Table 1. optical & electrical characteristics

Pixel characteristics	
Frame rate with analog output	Up to 23 full frames per second (see table1.1)

Table 1.1: In this table you find achievable values using the analog output

X pixels	Y pixels	X Freq	X Clock	X Blanking	line time	frame time	frame rate	pixel rate	pixel rate freq
#	#	Hz	sec	sec	sec	sec	per sec	sec	Hz
1286	1030	1,00E+07	1,00E-07	6,25E-06	0,000134850	0,138895500	7,20	1,049E-07	9536522
1286	1030	2,00E+07	5,00E-08	6,25E-06	0,000070550	0,072666500	13,76	5,486E-08	18228207
1286	1030	3,00E+07	3,33E-08	6,25E-06	0,000049117	0,050590167	19,77	3,819E-08	26182559
1286	1030	3,75E+07	2,67E-08	6,25E-06	0,000040543	0,041759633	23,95	3,153E-08	31719148
1286	512	3,75E+07	2,67E-08	6,25E-06	0,000040543	0,020758187	48,17	3,153E-08	31719148

Note 1. The pixel rate can be boosted to 37.5 MHz. This requires a few measures.

- increase the analog bandwidth by halving the resistor on pin Nbias_oamp
- increase the ADC speed by the resistors related to the ADC speed (nbiasana1, nbiasana2, pbiasencload)
- experimentally fine tune the relative occurrence of the ADC clock relative to the X-pixel clock.

Note 2. The pure digital scan speed in X and Y direction is roughly 50 MHz. This is the maximum speed for skipping rows and columns.

Light sensitivity & detection	
Spectral sensitivity range	400 - 1000 nm
Spectral response * fill factor	0.165 A/W @ 700 nm
Quantum efficiency * fill factor	> 30% between 500 & 700 nm
Fill factor	60%
Charge-to-voltage conversion gain	20 μV/e^-
Output signal amplitude	1.2 V
Full well charge [electrons]	IBIS4-1300: about 90000 saturation, 50000 linear range
Noise equivalent flux at focal plane (700 nm)	1.1e-4 lx*s (at focal plane) 6.3 e-7 s.W/m2
Sensitivity	7 V/lx.s 1260 V.m2/W.s
MTF @ Nyquist frequency	0.4-0.5 @ 450 nm 0.25-0.35 @ 650 nm
Optical cross talk	10% to 1st neighbor 2% to 2nd neighbor
Image quality	
Temporal noise (dark, short integration time)	20 noise electrons = 50 peak noise photons (*) 400 μV RMS
Dynamic range (analog output, before ADC conversion)	2750:1 69 dB
Dark current	344 pA/cm^2 @ 21°C 19 mV/s 1055 electrons/s
Dark current non-uniformity	Typically 15% RMS of dark current level.
Fixed pattern noise (dark, short integration time)	9.6 mV peak-to-peak 1-2 mV RMS
Photo-response non-uniformity (PRNU)	10% peak-to-peak @ ½ of saturation signal

Table 1. optical & electrical characteristics

Pixel characteristics	
Yield criteria	No missing columns nor rows Less than 100 missing pixels, clusters=<4 pixels
Anti-blooming	Overexposure suppression > 105
Smear	Absent
(*) peak noise photons are defined as (noise electrons) / (FF*peak QE)	
Features & general specifications	
Electronic shutter	Rolling curtain type Increment = line time = 135 us
Viewfinder mode	4 x sub-sampling (320 x 256 pixels)
Digital output	10 bit
Color filter array	Primary colors (Red, Green, Blue) RGB diagonal stripe pattern or Bayer pattern
Die size	10.30 x 9.30 mm^2
Package	84 pins LCC chip carrier 0.460 inch cavity
Supply voltage	5 V stabilized (e.g. from a 7805 regulator)
Power supply feed trough (dVout/dVdd)	< 0.3 for low-frequencies (< 1 MHz) < 0.05 for high frequencies (> 1 MHz)
Power dissipation (continuous operation, 10 MHz, ADC outputs loaded)	Min. 50 mA, Typ. 70 mA, Max. 90 mA

Light sensitivity

Figure 3. Spectral response * fill factor of the IBIS4-1300 pixels

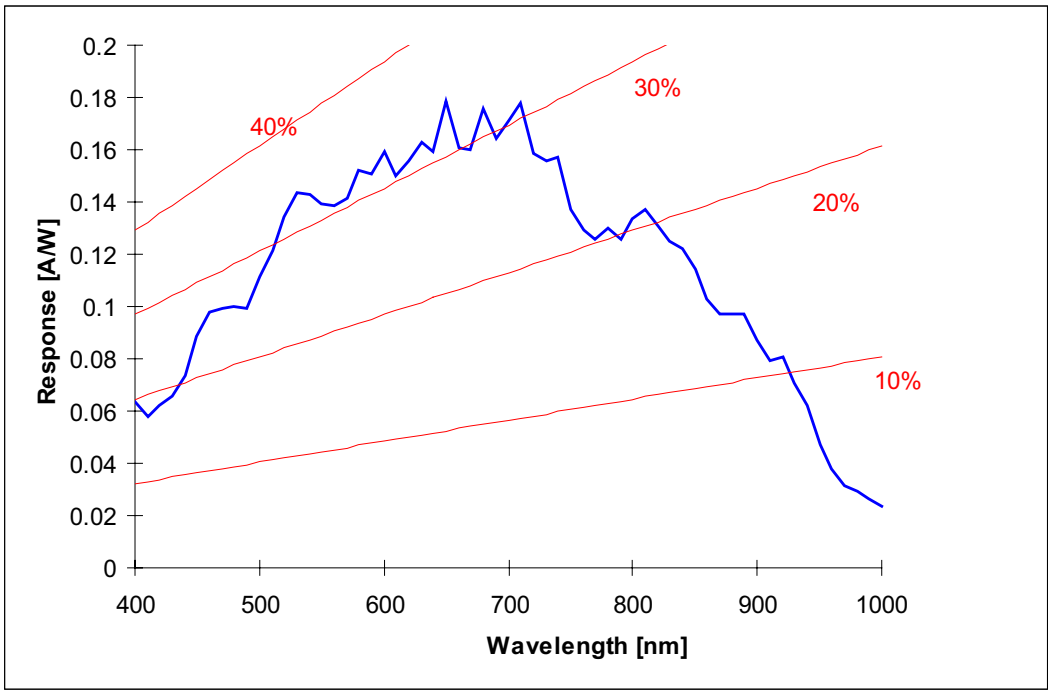
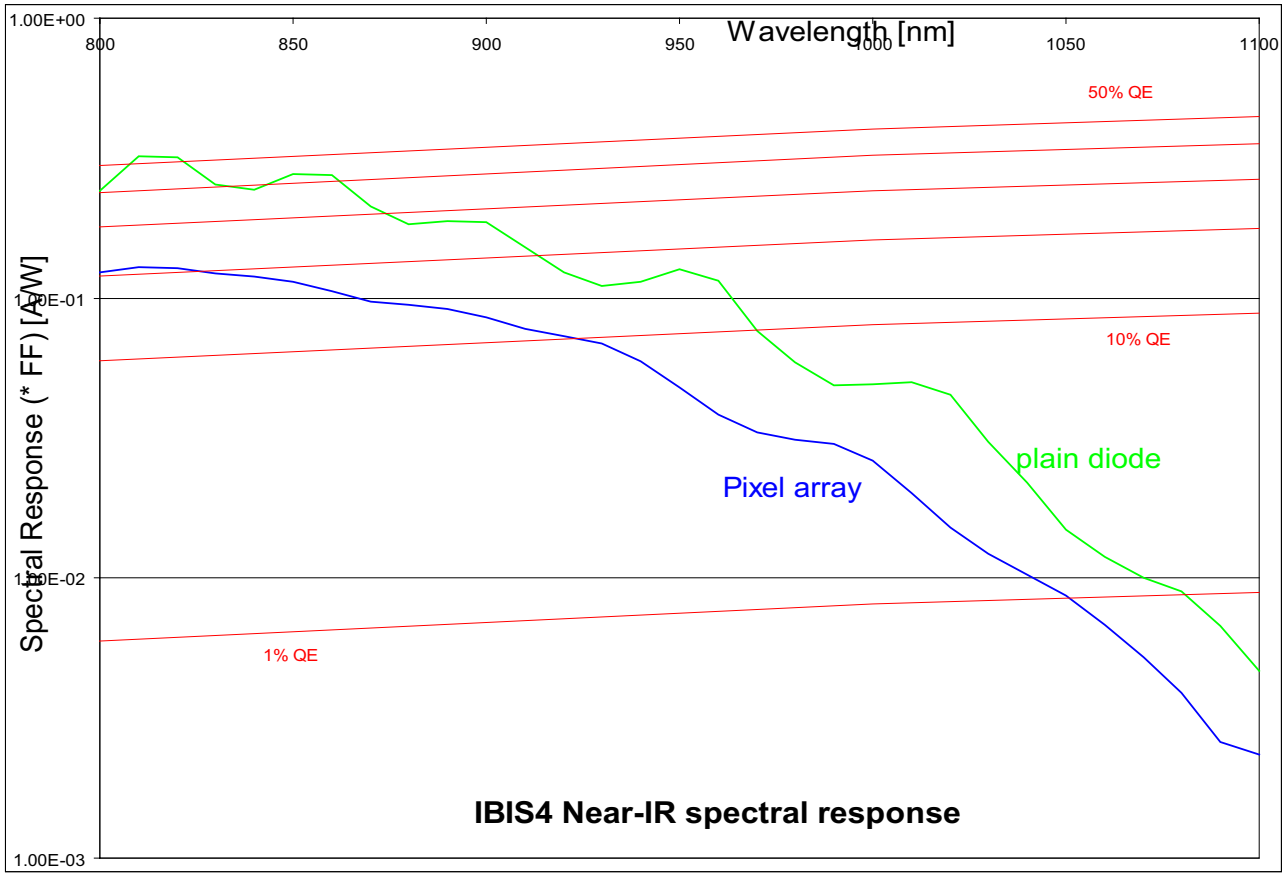


Figure 3. shows the spectral response characteristic. The curve is measured directly on the pixels. It includes effects of non-sensitive areas in the pixel, e.g. interconnection lines. The sensor is light sensitive between 400 and 1000 nm. The peak QE * FF is more than 30% between 500 and 700 nm. In view of a fill factor of 60%, the QE is thus larger than 50% between 500 and 700 nm.

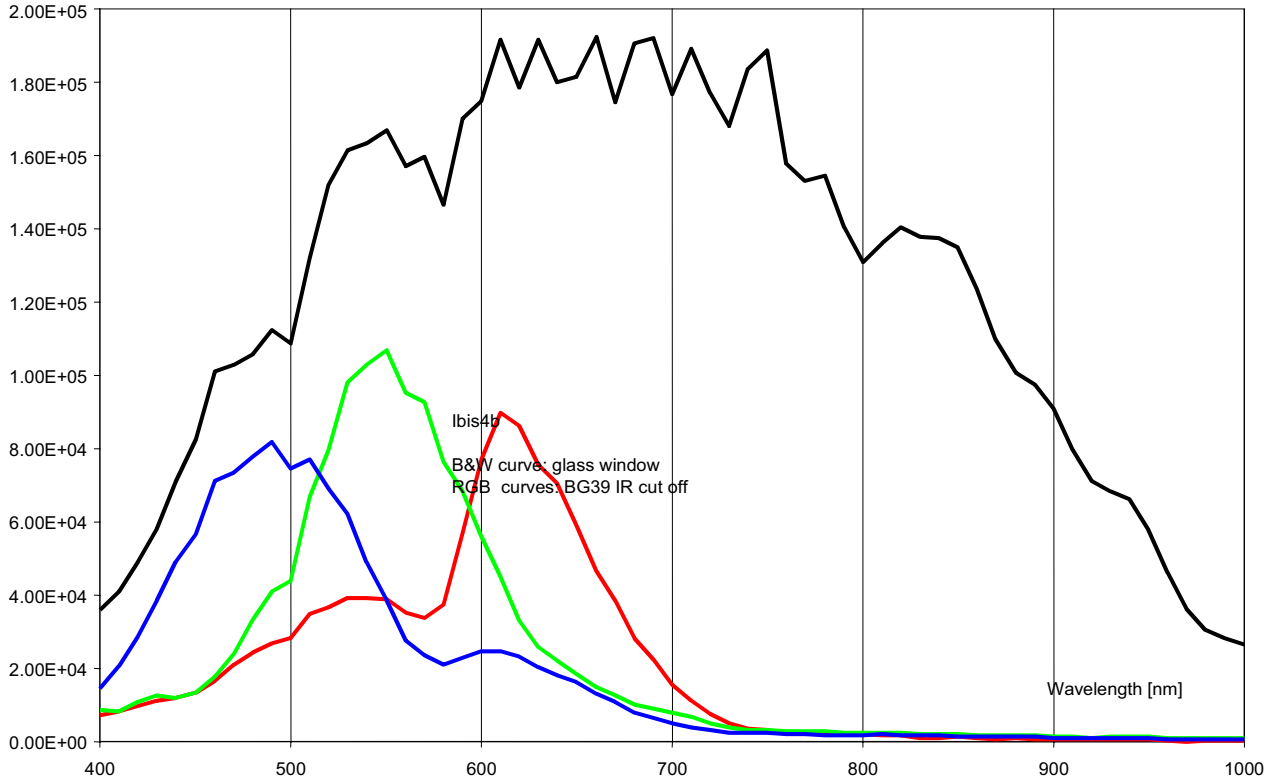
Figure 4. Near infrared spectral response



calculation of sensitivity in [V/lx.s]

Pixel area A	49 E-12 m2
Fill factor FF	60%
Spectral response SR	0.22 A/W (average)
FF*SR	0.13 A/W (average over wavelength)
Pixel capacitance Ceff	5E-15 F
Sensitivity = FF*SR*Ceff/A	1.27E+3 [V.W/s.m2]
Conversion to lux: 1W/m2 =	About 180 lux, visible light only About 70 lux, including Near Infrared
Sensitivity in lux units:	7.08 [V/lx.s] visible light only 18 [V/lx.s] if near IR included.

Color sensitivity



Charge conversion - Conversion of electrons in an output signal

Figure 5. IBIS4-1300 response curve - two pixels - lowest gain setting (0000)

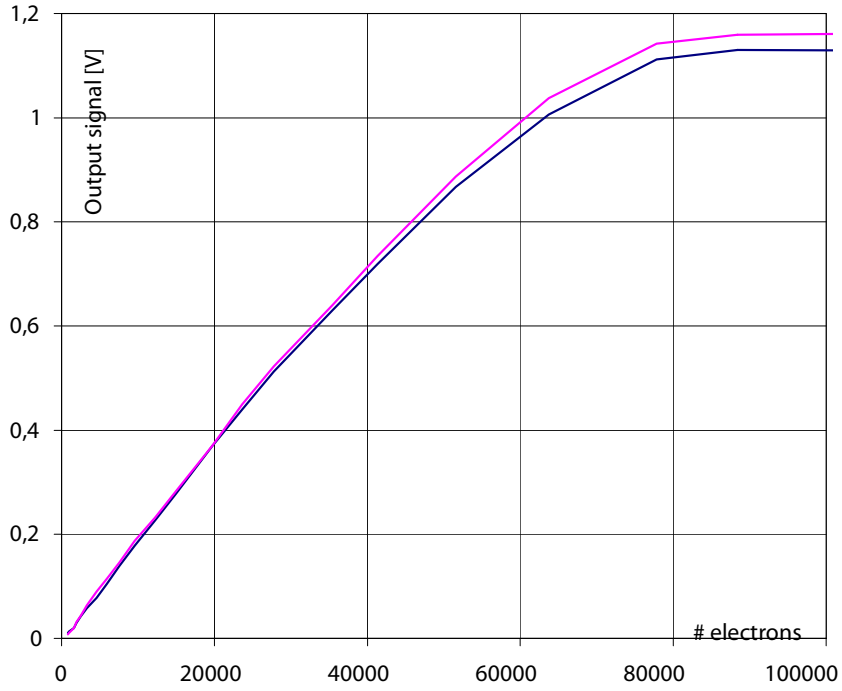


Figure 5. shows the pixel response curve in linear response mode. This curve is the relation between the electrons detected in the pixel and the output signal. This curve was measured with light of 600 nm, with an integration time of 138.75 ms (10 MHz pixel rate), at minimal gain setting 0000. The resulting voltage/electron curve is independent of these parameters. The conversion gain is 18 uV/electron for this gain setting.

Note that the upper part of the curve (near saturation) is actually a logarithmic response, similar to the FUGA1000 sensor. The level of saturation can be adjusted by the voltage on GND-AB. However note also that this logarithmic part of the response is not FPN corrected by the on-chip offset correction circuitry.

The signal swing (and thus the dynamic range) is extended by increasing the VDD_RESET (pins 59/79) to 5.5 V. This is mode of operation is not further documented.

Table 2. shows the pins of the IC that are related to the image sensor core, describing their functionality.

Table 2. Pins of the image sensor core

Digital controls		
SYNC_YR\	5	Reset right Y shift register (low active, 0 = sync)
CLK_YR	6	Clock right Y shift register (shifts on falling edge)
EOS_YR\	7	(output) low 1st CLK_YR pulse after last row (low active)
SYNC_X\	28	Reset X shift register (low active, 0 = sync)
CLK_X	29	Clock X shift register (shifts on falling edge)
EOS_X\	8	(output) Low 1st CLK_X pulse after last active column (low active)
SYNC_YL\	36	Reset left Y shift register (low active, 0 = sync)
CLK_YL	37	Clock left Y shift register (shifts on falling edge)
EOS_YL\	38	Low 1st CLK_YL pulse after last row
SHY	30	Parallel Y track & hold (1 = hold, 0 = track) apply pulse pattern - see sensor timing diagram
SIN	35	Column amplifier calibration pulse 1 = calibrate - see sensor timing diagram
SELECT	40	Selects row indicated by left/right shift register high active (1= select row) Apply 5 V DC for normal operation
RESET	41	Resets row indicated by left/right shift register high active (1 = reset) Apply pulse pattern - see timing diagram
L/R\	80	Use left or right register for SELECT and RESET 1 = left / 0 = right - see sensor timing
SUBSMPL	84	Activate viewfinder mode (1:4 sub sampling = 320 x 256 pixels) high active, 1 = sub sampling
Reference voltages		
DCCON	31	Control voltage for the DCREF voltage generation Connect to ground by default
DCREF	32	Reference voltage (output), to be decoupled to GND Should be about 1.2V, can be adjusted by DCCON
NBIASARRAY	1	1 MegaOhm to VDD and decouple to ground by 100 nF capacitor
PBIAS2	2	1 MegaOhm to ground and decouple to VDD by 100 nF capacitor
PBIAS	3	1 MegaOhm to ground and decouple to VDD by 100 nF capacitor
XMUX_NBIAS	4	100K to VDD and decouple to ground by 100 nF capacitor

Table 2. Pins of the image sensor core

Digital controls		
GND_AB	54	Anti-blooming drain control voltage • Default: connect to ground. The anti blooming is operational but not maximal. • Apply about 1 V DC for improved anti-blooming
Power & ground		
VDD_RESETL	59	Power supply for left reset line drivers apply 5 V DC (default) or about 4…4.5 V for dual slope mode
VDD_RESETR	79	Power supply for right (default) reset line drivers 5 V DC
VDD_ARRAY	55	Power supply for the pixel array 5 V DC
VDD	11 34 53 77	Power supply of image sensor core & output amplifier 5 V DC
GND	10 33 52 78	Ground of image sensor core & output amplifier

Output amplifier

The output amplifier stage is user-programmable for gain and offset level. Gain and offset are controlled by 4-bit wide words. Gain settings are on an exponential scale. Offset is controlled by a 4-bit wide DAC, which selects the offset voltage between 2 reference voltages (Vhigh_dac & Vlow_dac) on a linear scale.

The offset setting is independent of the gain setting.

The gain setting is independent of amplifier bandwidth.

The amplifier is designed to match the specifications like the output of the imager array. This signal has a data rate of 10 MHz and is located between 1.2 and 2.4 V. Table 3. summarizes the specifications of the amplifier.

Table 3. Summary of output amplifier specifications

	Min.	Typ	Max
Gain	1.2 (gain setting 0)	2.7 (setting 4)	16 (setting 15)
Output signal range	1 V		4.5 V
Bandwidth (40 pF load)	12 MHz (gain setting 15)	22 MHz (gain setting 0...8)	33 MHz (gain setting 0)
Output slew rate (40 pF load)	40 V/ μs	50 V/μs	80 V/μs

The range of the output stage input is between 1 and 4 V. A lowest gain the sensor outputs a signal in between 1.2 and 2.2 V, which fits into the input range of the amplifier. The range of the output signal is between 1 and 4.5 V, dependent on the gain and offset settings of the amplifier. This range should fit to the input range of the ADC, external or internal. The on-chip ADC range is between 2 and 4 V. A minimal gain setting of "3" seems necessary for the internal ADC, and the offset voltage should be set to the low-reference voltage of the ADC.

Figure 6. output amplifier architecture

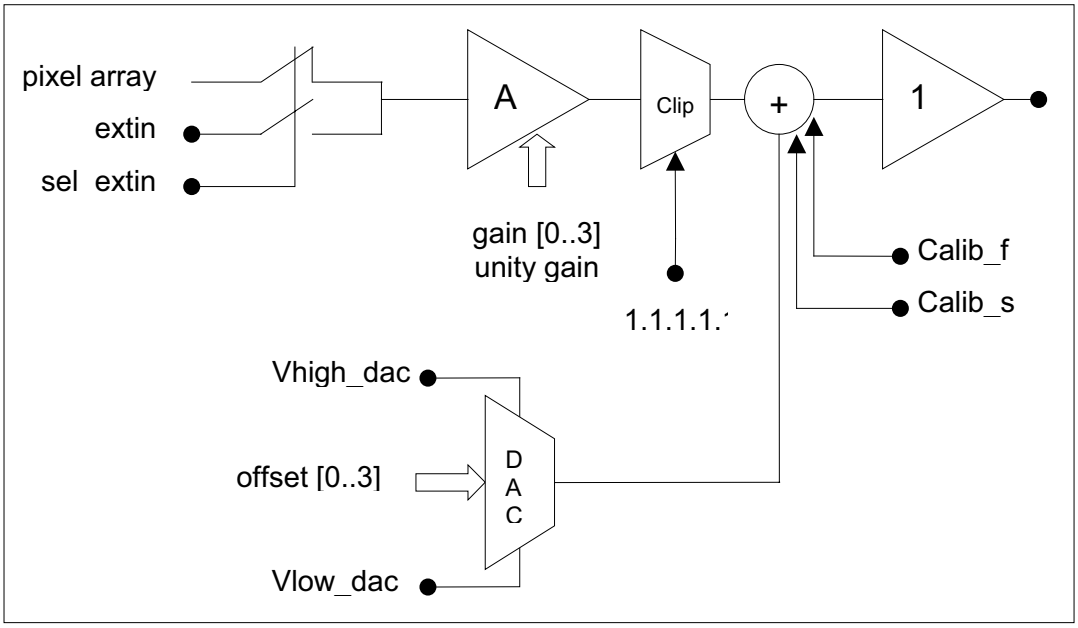


Figure 6. shows the architecture of the output amplifier. First of all, there is a multiplexer which selects either the imager core signal or an external pin EXTIN as the input of the amplifier. EXTIN can be used for evaluation, or to feed alternative data to the output.

SEL_EXTIN controls this switch.

Then, the signal is fed to the first amplifier stage. This stage has an adjustable gain, controlled by a 4-bit word ('gc_bit0...3').

Then, the upper level of the signal must be clipped in some situations (clipping sometimes is necessary when the imager signal is highly saturated, which affects the calibration level. This is visible as black banding at the right side of bright objects in the scene). In order to do this, a voltage should be applied to the 'Clip' pin. The signal is clipped if it is higher than Vclip - Vth,pmos, where Vth,pmos is the PMOS threshold voltage and is typically -1 V. If clipping is not necessary, 5 V should be applied to 'Clip'.

After this, the offset level is added. This offset level is set by a DAC, controlled by a 4-bit word (DAC_bit0...3). The offset level can be calibrated in two modes: fast offset adjustment or slow offset adjustment. This is controlled by 'calib_s' and 'calib_f'. The slow adjustment yields a somewhat cleaner image.

After this, the signal is buffered by a unity feedback amplifier and it leaves the chip. This 2nd amplifier stage determines the maximal readout speed, i.e. the bandwidth and the slew rate of the output signal. The whole amplifier chain is designed for a data rate of 10 Mpix/s (@ 40 pF). (It is up to the experimenter to increase this speed by reducing the various setting resistors)

Table 4. shows the IBIS4-1300 pins used by the output amplifier with a short functional description. Power and ground lines are shared between the output amplifier and the image sensor.

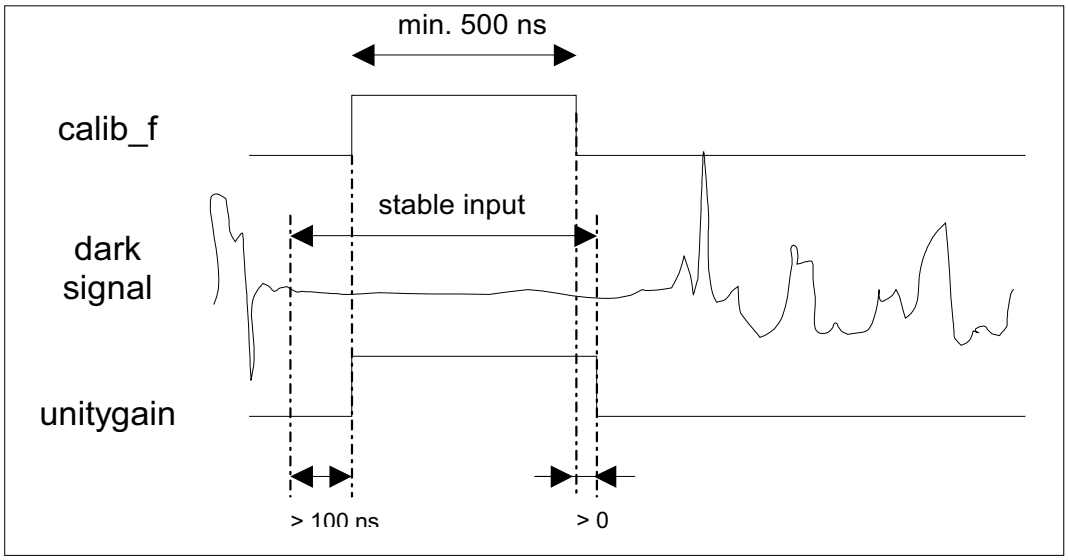
Output amplifier offset level adjustment

The purpose of this adjustment is to bring the pixel voltage range as good as possible within the ADC range. The offset level of the output signal is controlled by a 4-bit resistive DAC. This DAC selects the offset level on a linear scale between 2 reference voltages. These reference voltages are applied to Vlow_dac and Vhigh_dac.

This offset level is adjusted during the calibration phase. During this phase, the amplifier input should be constant and refers to the 'zero' signal situation. The IBIS4-1300 outputs a dark reference signal after a row has been read out completely. This signal can be used as the 'zero signal' reference. Alternatively one can apply an external reference on pin EXTIN, which is applied to the output amplifier when SEL_EXTIN is 1.

Offset adjustment can be done during row or frame blanking time.

Figure 7. offset adjustment: fast offset adjustment mode



There are 2 modes of offset calibration for the output amplifier: slow and fast adjustment. Figure 7. shows the timing and signal waveforms for fast offset adjustment mode. Closing both 'calib_f' and 'unitygain' operates it. After 'calib_f' is opened again, the offset level is adjusted to the desired value in a single cycle. The signal applied to the output amplifier should be stable just before and during the adjustment phase. The same is true for the DAC output.

The signal applied to the output amplifier can be either:

- The signal generated by the electrical dark reference in the imager core itself, i.e. the pixels named "dark" inFigure 20.
- Apply the reference from outside on the pin EXTIN, controlled by SEL_EXTIN.

If this fast offset adjustment is used, it should be done once each frame, before the readout of the frame starts, e.g. during the blanking time of the first line.

Figure 8. slow offset adjustment mode

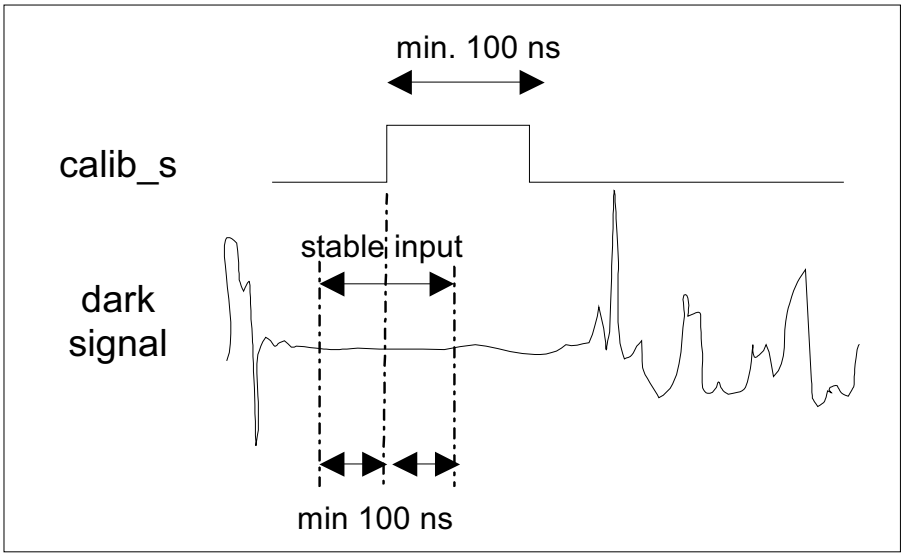


Figure 8. shows the timing and signal waveforms for slow offset adjustment mode. It is operated by pulsing 'calib_s'. The amplifier input signal must be stable and refer to 'dark' signal at the moment when calib_s goes low. The offset is slowly adjusted with a time constant of about 100 of these pulses. One pulse is then generated during each row blanking time.

The baseline is to use the fast calibration once per image. The slow calibration is intended as alternative if, for very slow readout, the offset drifts during the image.

Table 4. Pins involved in output amplifier circuitry

Name	No.	Function
Analog signals		
Extin	12	External input of the output amplifier Active if Sel_extin = 1
Output	13	Analog output signal To be connected to the input of the ADC (in_adc, pin 73)
Digital Controls		
Sel_extin	9	1 = external input pin (extin) is applied at the input of the amplifier 0 = output amplifier is connected to the image sensor array
gc_bit0	17	LSB Control bits for output amplifier gain setting Gain adjustment between 1.2 (0000) & 16X (1111) MSB
gc_bit1	18	
gc_bit2	19	
gc_bit3	20	
unitygain	21	1 = output amplifier in unity feedback mode 0 = output amplifier gain controlled by gc_bit0...3
calib_s	16	Slow (or incremental) output offset level adjustment (calibration of output amplifier). Offset adjustment converges after about 100 pulses on calib_s Amplifier input should refer to a 'zero signal' at the moment of the 1->0 transition on calib_s 0 = connect to capacitor (of stage 2) and in- (of stage 1) 1 = connect to DAC output (of stage 2) and out (of stage1)
calib_f	22	Fast (=in 1 cycle) output offset level adjustment (calibration of output amplifier) Offset level is adjusted when both calib_f and unitygain are high Amplifier input should refer to 'zero signal' when calib_f is high 1 = connect DAC output to offset of capacitor 0 = DAC output disconnected
dac_b0	26	LSB Control bits for output offset level adjustment Between Vlow_dac (0000) & Vhigh_dac (1111) MSB
dac_b1	25	
dac_b2	24	
dac_b3	23	
Reference voltages		
Vlow_dac	14	Low and high references for offset control DAC of the analog output. The range of this resistive division DAC should be about 1V to 2.5V. If the range is not OK, one will notice that it is not possible to adjust the output voltage to the appropriate level of the ADC. As the internal division resistor is about 1.3 Kohm, we suggest to tie Vlow_dac with 1K to GND and Vhigh_dac with 2K7 to VDD.
Vhigh_dac	15	
Nbias_oamp	27	Output amplifier speed/power. Connect with 100 K to VDD and decouple with 100 nF to GND. This setting yields 10 MHz nominal pixel rate. Lowering the resistance does increasing this rate.
Clip	83	Voltage that can be used to clip the output signal Clips output if output signal > 'Vclip - Vth, PMOS' with Vth,PMOS=-1V Default: 5 V (no clipping)

Output amplifier gain control

Figure 9. output amplifier DC gain

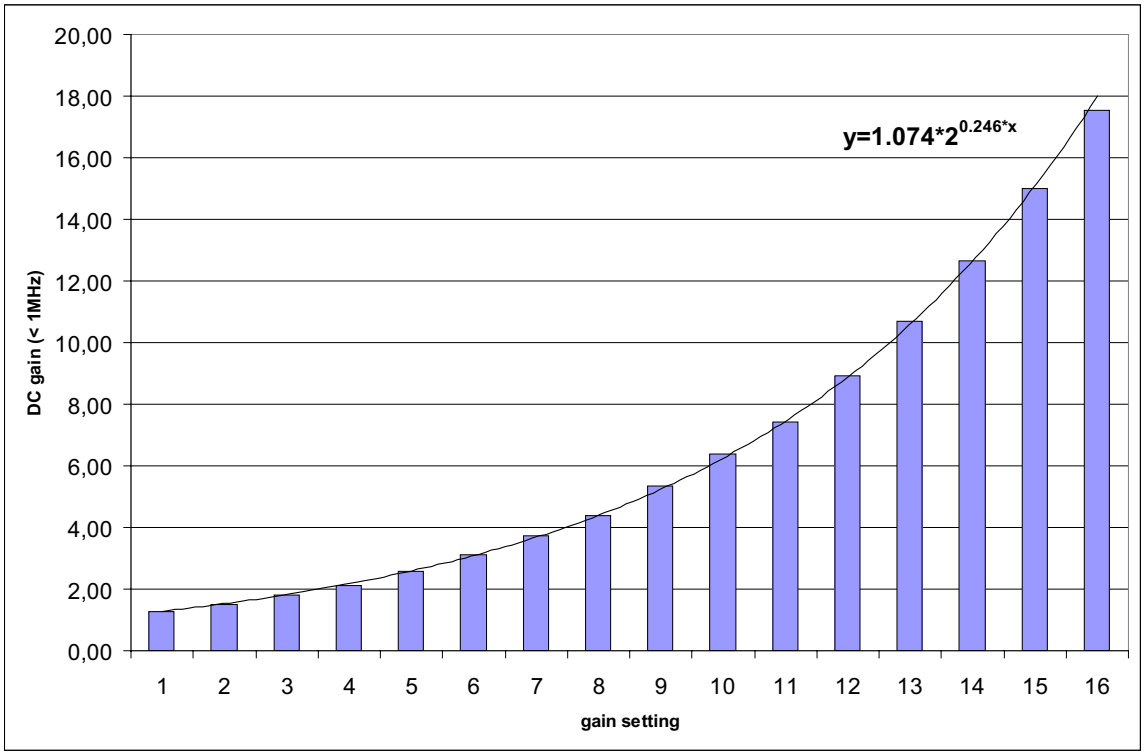


Table 5. DC gain of output amplifier for different gain settings

gain setting	DC gain (<1MHz)	gain setting	DC gain (<1MHz)
0000	1.28	1000	5.33
0001	1.51	1001	6.37
0010	1.82	1010	7.41
0011	2.13	1011	8.91
0100	2.60	1100	10.70
0101	3.11	1101	12.65
0110	3.71	1110	15.01
0111	4.40	1111	17.53

The output amplifier gain is controlled by a 4-bit word. In principle, the output amplifier can be configured in unity feedback mode by a permanent high signal on UNITYGAIN, but the purpose of this mode is purely diagnostic. The "normal" gain settings vary on an exponential scale. Figure 9. and Table 5. report all gain settings.

In first approximation, the gain setting is independent of bandwidth, as the amplifier is a 2-stage design. The first stage sets the gain, and the second stage is a unity gain buffer, that determines bandwidth and slew rate. There is however some influence of gain setting on bandwidth. Figure 10. shows the output amplifier bandwidth for all gain settings.

Figure 10. output amplifier bandwidth for different gain settings

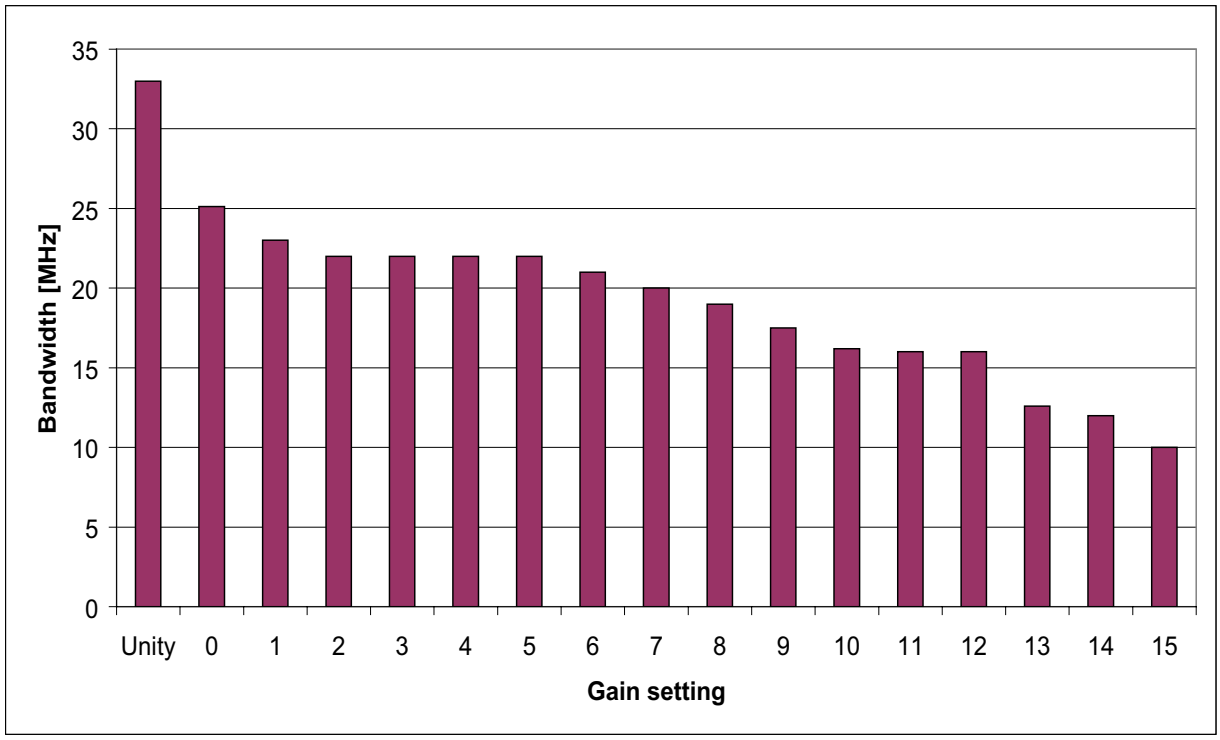


Figure 11. typical transfer characteristic of the output amplifier (no clipping, Voffset = 2 V, input signal during offset adjustment is 1.2 V)

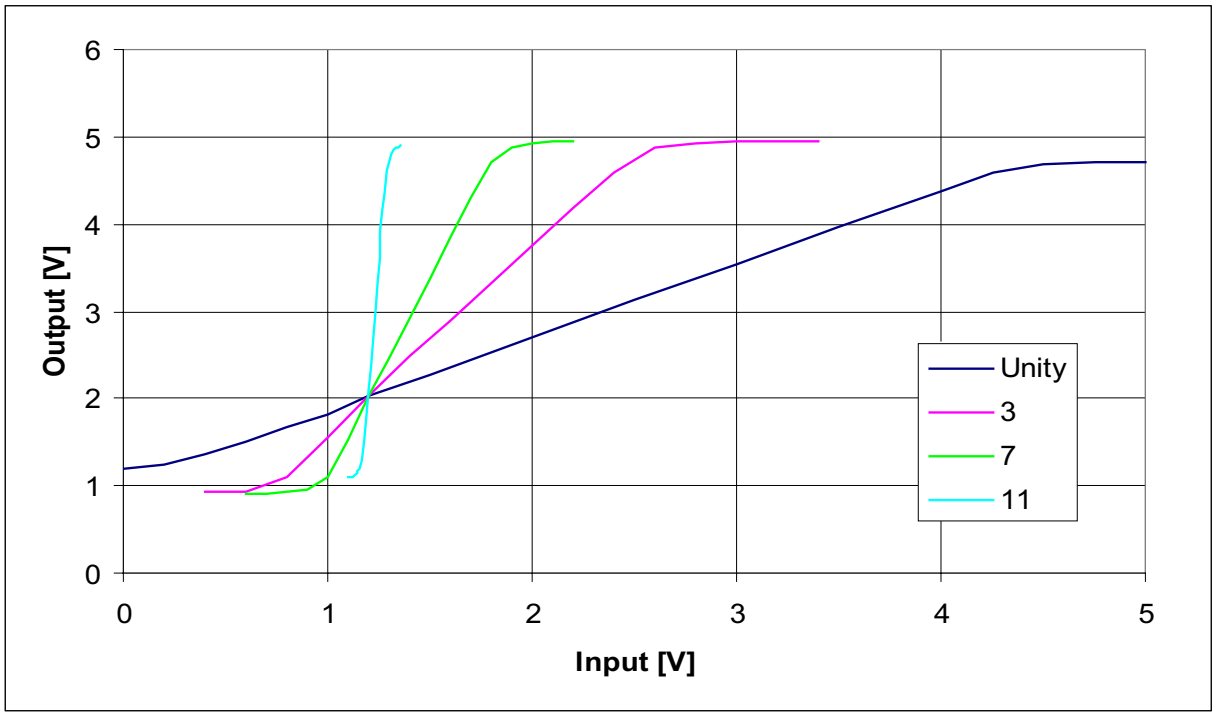
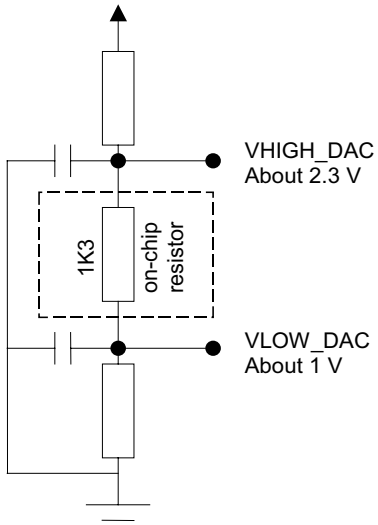


Figure 11. shows the output characteristic curve in a typical case for the imager. The offset voltage is adjusted to 2 V, which corresponds to the low-level voltage of the ADC. Clipping is off, and the input signal is changed between 0 and 5 V. During offset adjustment (when calib_s is switched from 1 -> 0 or when calib_f is on), the input signal is at 1.2 V. This level corresponds to the imager dark reference output. The input signal is transferred to the output by adding a 2V offset and multiplication with the appropriate gain. The input signal of dark pixels (at 1.2 V) corresponds with 2 V at the output. Higher input signals are amplified. The curves for 3 typical gain settings are shown (unity gain, setting 3, 7 & 11).

Again, as can be seen on the above figure, the applied input signal during the output amplifier calibration (by 'CALIB_S' or 'CALIB_F') is the reference level to which the signal is amplified. During this calibration, a stable input is required.

Setting of the VLOW_DAC & VHIGH_DAC reference voltages

Figure 12. suggested circuit for high and low references of DAC



VLOW_DAC & VHIGH_DAC are the reference voltages for the DAC. They represent the 0000 resp. 1111 code. The internal series resistance is about 1.3 kOhms. They can be connected as in Figure 12., and decoupled to ground.

Analog to digital converter

The IBIS4-1300 has a 10 bit flash analog digital converter running nominally at 10 Msamples/s. The ADC is electrically separated from the image sensor. The input of the ADC ("IN_ADC") should be tied externally to the OUTPUT of the output amplifier.

Table 6. ADC specifications

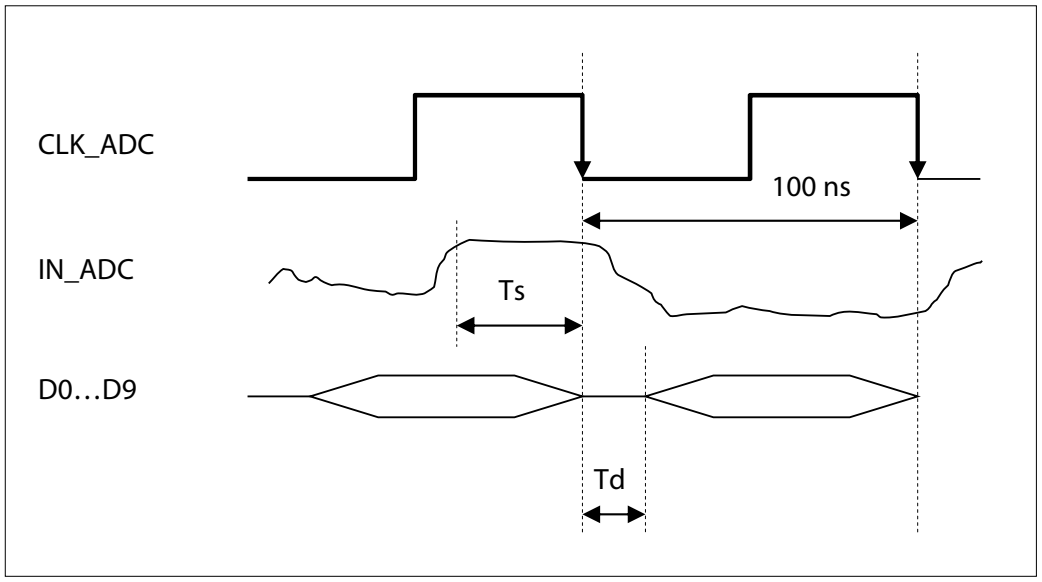
Input range	2 - 4 V
Quantization	10 Bits
Nominal data rate	10 Msamples/s (*)
DNL (linear conversion mode)	
INL (linear conversion mode)	
Input capacitance	< 20 pF
Power dissipation @ 10 MHz	107 mA 535 mW
Delay of digital circuitry (Td, 40 pF load)	< 50 ns after falling edge of clock
Input setup time (Ts) for a stable LSB	< 100 ns before falling edge of clock
Conversion law	Linear / Gamma-corrected

(*) Project partners have demonstrated 20 MHz data rate by careful timing and by decreasing some or all of the resistors on NBIAS* and PBIAS*.

ADC timing

The ADC converts on the falling edge of the CLK_ADC clock. The input signal should be stable during a time Ts before the falling clock edge. The digital output is available Td after the falling clock edge (Figure 13., Ts = 100 ns, Td = 50 ns). These values are the delays to obtain a stable LSB after a half-scale swing of the input signal. For the MSB to become stable, Ts=20 ns is sufficient. For a full scale input swing (which normally doesn't appear with image sensors), Ts is 140 ns for the LSB and 20 ns for the MSB.

Figure 13. ADC timing



TRI_ADC can be used to put the output bits in a tristate mode (e.g. for bi-directional busses). If this is used, the output signal becomes valid 50 ns after the falling edge on TRI_ADC.

BITINVERT can be used to invert the output word, if necessary (one's complement).

When NONLINEAR is high, the ADC conversion is non-linear. The contrast will be higher in dark image regions, and lower in bright areas, similar to gamma correction.

Table 7. pins of the ADC

Name	No.	Description
Analog signals		
IN_ADC	73	Input, connect to sensor's output (pin 13) Input range is between 2 & 4 V (VLOW_ADC & VHIGH_ADC)
Digital Controls		
CLK_ADC	62	ADC Clock ADC converts on falling edge
TRI_ADC	63	Tristate control of ADC digital outputs 1 = tristate; 0 = output
NONLINEAR	67	1 = non-linear analog-digital conversion 0 = linear analog-digital conversion
BITINVERT	39	1 = invert output bits 0 = no inversion of output bits
Digital output		
DO… D9	51…42	Output bits D0 = LSB, D9 = MSB
Reference voltages		

Table 7. pins of the ADC

Name	No.	Description
VLOW_ADC	71	Low reference and high reference voltages of ADC should be 2V to 4V. The resistance between VLOW_ADC and VHIGH_ADC is about 1.5 K, thus this range can be approximated by tying LOW with 2K to GND And HIGH with 1K to VDD.
VHIGH_ADC	61	
PBIASDIG1	64	Connect with 100K to GND and decouple to VDD
PBIASENCLOAD	65	Connect with 100K to GND and decouple to VDD
PBIASDIG2	66	Connect with 100K to GND and decouple to VDD
NBIASANA2	69	Connect with 100K to VDD and decouple to GND
NBIASANA	70	Connect with 100K to VDD and decouple to GND
		These resistors determine the analog resp. digital speed /power of the ADC. Both can be increased/decreased by lowering or increasing the resistance values.
Power & Ground		
VDD_DIG	56, 76	Power supply of digital circuits of ADC, + 5 V
VDD_AN	58, 74	Power supply of analog circuits of ADC, + 5 V
GND_DIG	57, 75	Ground of digital ADC circuits
GND_AN	60, 72	Ground of analog ADC circuits

Control of the VLOW_ADC & VHIGH_ADC reference voltages

VLOW_ADC & VHIGH_ADC are the reference voltages for a 0 and 1023 code. A 2K-resistor ladder internally connects them. The appropriate 2 V and 4 V DC voltages can be obtained as in Table 7. : pins of the ADC, and decoupled to ground.

Non-linear and linear conversion mode - "gamma" correction

Figure 14. linear and non-linear ADC conversion characteristic

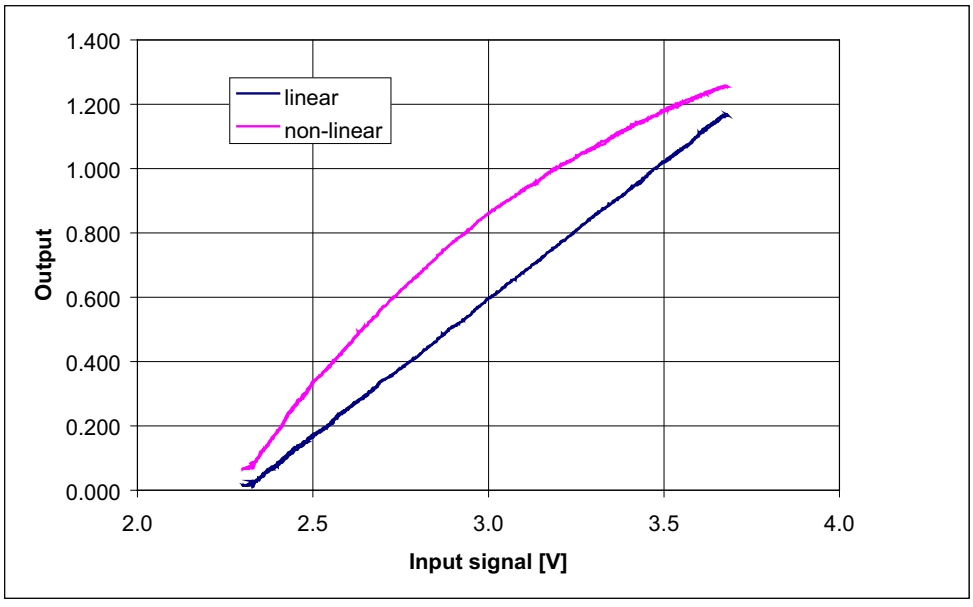


Figure 14. shows the ADC transfer characteristic. For this measurement, the ADC input was connected to a 16-bit DAC. The input voltage was a 100 KHz triangle waveform.

The non-linear ADC conversion is intended for gamma-correction of the images. It increases contrast in dark areas and reduces contrast in bright areas. The non-linear

curve is tolerant for external pixel offset error correction. This means that pixel offset variations can be corrected by changing the offset after the non-linear AD conversion. This is so because the non-linear transfer function is

$$H(s) = 1-\exp(-a*s)$$

by design, and neglecting the offset, the relation between the non-linear output (y) and the linear output (x) is exactly:

$$Y = 1024 * (1 - \exp(-x/713)) / (1 - \exp(-1024/713))$$

This law yields an increased accuracy of about a factor 2 near the zero end of the scale. It is thus possible to obtain an effective 11 bit accuracy on a linear scale after post processing by applying the reverse law to the non-linear output:

$$Z = -2 * 713 * \ln(1 - y/(1024/(1-\exp(-1024/713)))) = -1426 * \ln(1-y/1343.5)$$

Then Z is an 11-bit linear output in the range 0...2047.

Operation of the image sensor

Set configuration & pulse timing

Figure 15. typical operation mode (readout of a frame)

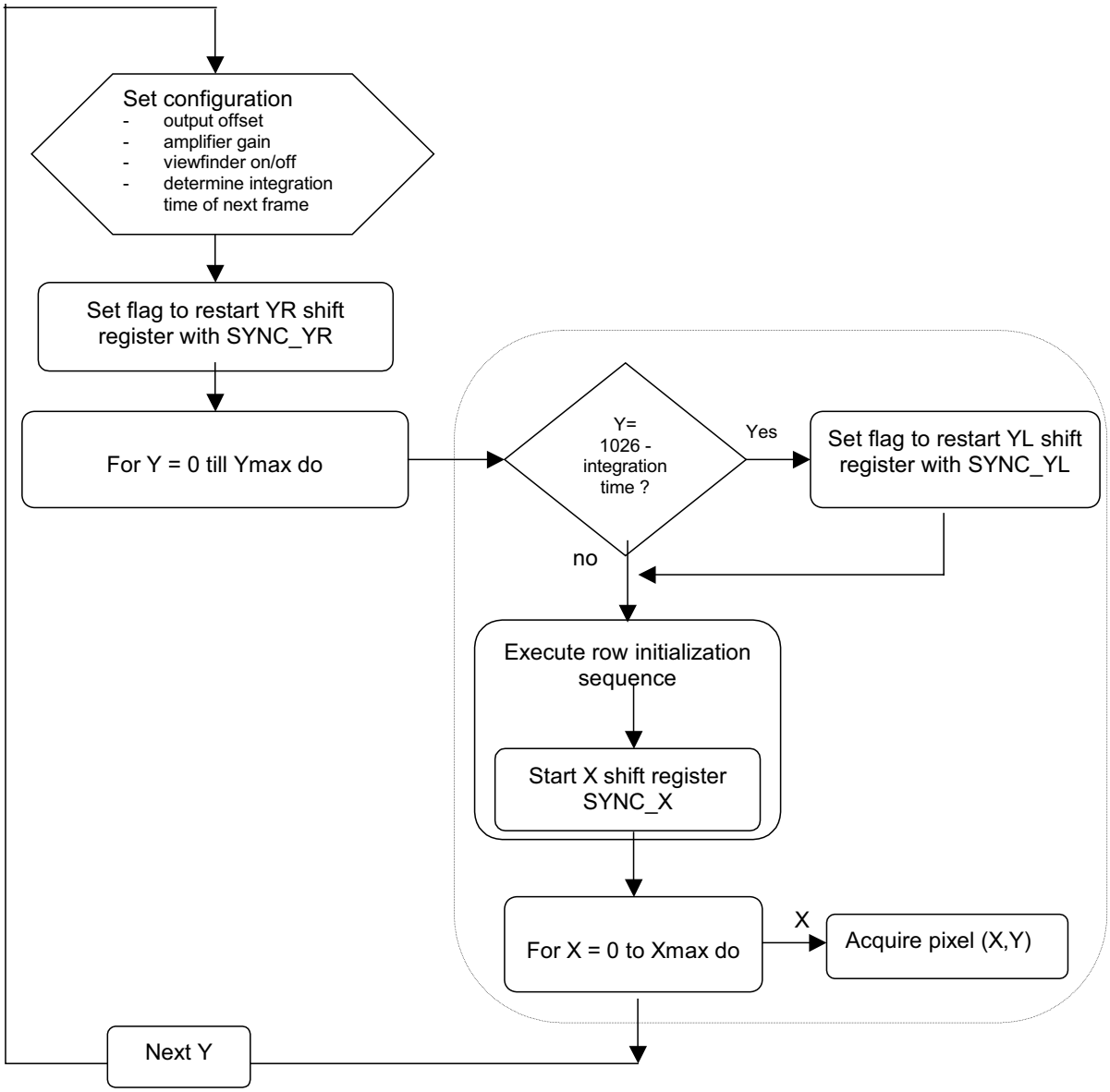


Figure 15. shows a typical operation mode of the image sensor.

At the start of a new frame, the device may be (re-)configured. If necessary, the output amplifier gain and offset are adjusted or the device is put in viewfinder mode.

Then, the frame readout shift register is initiated by pulsing "SYNC_YR". This pulse occurs once per frame, normally as a part of the first row blanking sequence.

The readout of a row (line) starts with row blanking initialization sequence. Here several pulses are applied for Y-direction shift, the column amplifier S&H and nulling, and the start (SYNC_X) of the X-direction shift register.

The frame reset shift register is started also once per frame by "SYNC_YL", this pulse occurs once per frame, normally as a part of the row blanking sequence of one particular row. The time delay from the SYNC_YL to SYNC_YR is the integration time. The integration is thus a multiple of the row readout time. The reset shift register always leads the readout shift register.

Viewfinder mode vs. normal readout

Therefore, the integration time should be determined before the start of the frame readout. The value that is fixed at that moment will be the integration time of the NEXT frame. If the value set for the integration time changes during frame readout, the start pulse might be lost and the next frame might be invalid. We will now discuss all steps in more detail.

Set configuration

Configuration of the image sensor implies control & adjustment of the following points:

- output amplifier offset level, set by 'dac_bit[0...3]'
- output amplifier gain setting, set by 'gc_bit[0...3]'
- choose the integration time of the next frame
- set/clear viewfinder mode (pin 'subsampl')
- in case when the fast adjustment of the offset level is used, plus 'calib_f' and 'unitygain' as described before in figures Figure 7. and Figure 8.

Table 8. co-ordinate of the row or column selected by the Y/X shift registers after a # clock periods in viewfinder mode and full image mode

Clock	Sync	1	2	3	4	5	6	
Viewfinder mode	None	None	Row 1	Row 5	Row 9	Row 13	Row 17	Y reg.
			Dark	Col. 1	Col. 5	Col. 9	Col. 13	X reg.
Full image mode	None	None	Row 1	Row 2	Row 3	Row 4	Row 5	Y reg.
			Dark	Col. 1	Col. 2	Col. 3	Col. 4	X reg.

Clock	258	259	260
Viewfinder mode	Row 1025	Row 1029	EOS

322	323	324
Col. 1281	Col. 1285	EOS Dark

Clock	1030	1031	1032
Full image mode	Row 1029	Row 1030	EOS
	Y shift register		

1287	1288	1289
Col. 1285	Col. 1286	EOS Dark
X shift register		

In full image readout mode (pin 84, subsmpl = 0), the imager is a 1280 x 1024 SXGA image sensor. There are 3 dummy pixels read at all 4 borders of the image.

In viewfinder mode (subsmpl = 1), the imager acts as a 320 x 256 QVGA image sensor with one dummy pixel at the start of a row/column.

Table 8. shows which column or row is selected after a number of clock pulses.

Start of the Y shift registers for row readout & row reset

The shift registers are put in their initial state by a synchronization- or start pulse. (sync_x, sync_yr, sync_yl). The synchronization signal is low-active and should only be generated when the clock of the shift register is high. After the synchronization pulse, two falling clock edges are needed to skip dummy pixels/lines. On every falling clock edge, the shift register selects a new row for readout or reset. Figure 16. shows this timing.

Figure 16. Timing of Y shift registers (for row selection)

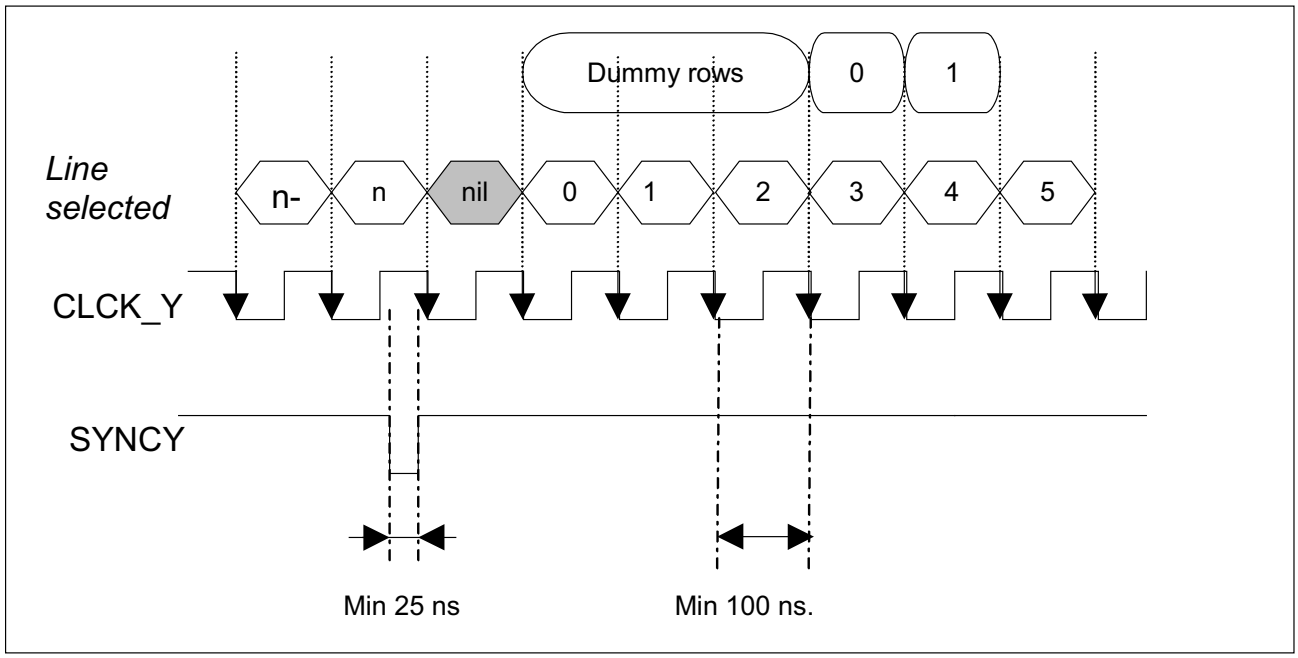
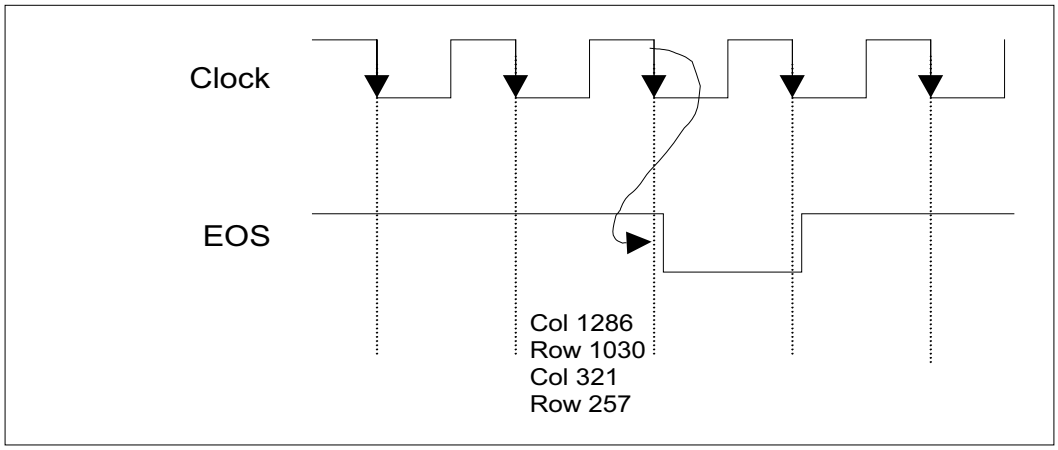


Figure 17. End-of-scan pulse



End-of-scan: EOS_YL, EOS_YR, EOS_X

All 3 shift registers are equipped with 'end-of-scan' pulses. These pulses are low during the clock period after the last pixel or row has been read out, also in viewfinder mode.

At the EOS_X pulse, the electrical dark reference level is put on the readout bus. This voltage remains on the bus until the SIN pulse goes high. During the row blanking time, this voltage can be used for the offset adjustment of the output amplifier. The SIN high forces the DCREF voltage on the output bus.

We advise not to use the EOS pulses as an input for the row blanking time sequence generation, but to use simple counters instead. If by some reasons the EOS signal is absent or subject to glitches, the system would hang. EOS is intended as diagnostic means.

Row initialization

During the row blanking time (which occurs at the beginning of every row read), several tasks are executed: selection of a new row, readout of this row by double sampling, reset of a new row, and possibly (slow) offset adjustment of the output amplifier. Therefore, a pulse patterns must be applied to several signals during this time. There is some freedom to make this pattern. The constraints are listed below:

Figure 18. Timing constraints for row readout initialization (blanking time)

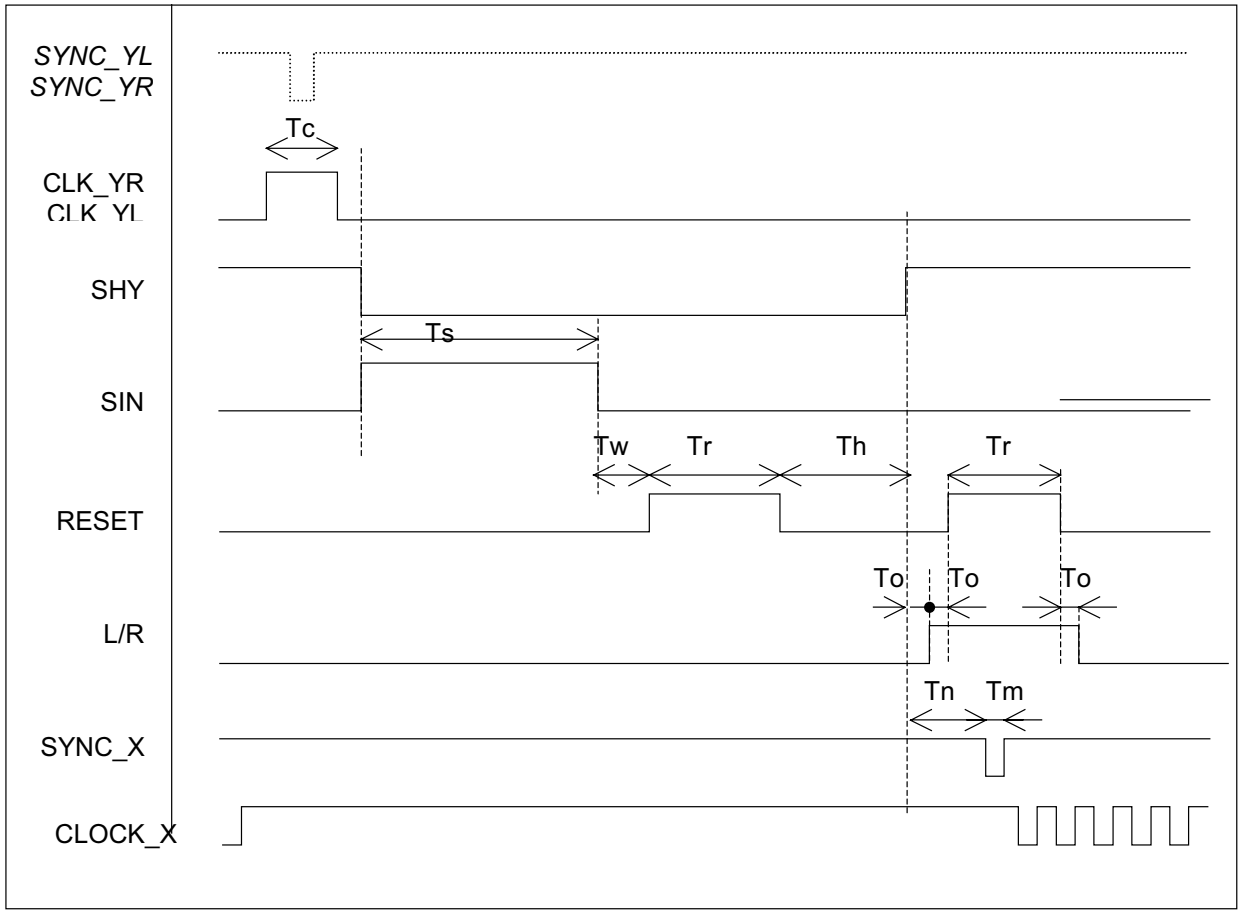


Table 9. Timing constraints on row initialization pulses sequence

Ta	Min 0	Delay between falling edge of CLK_Y* and SHY or SIN
Tc	Min 25 ns	CLK_YR & CLK_YL high time
Ts	Typ. 3 us	On-time of SIN (offset calibration pulse) Delay between selection of new row and end of column amplifier calibration
Tw	Typ. 200 ns	Delay between end SIN and pixel reset
Tr	Typ. 1 us	On-time of reset pulse
Th	Typ 1 us	Th + Tr = Delay between pixel reset and column sample & hold
To	Typ 100 ns	Delay between SHY and L/R\ Overlap of L/R\ over 2nd reset pulse
Tm	Min 25 ns	On-time of one of the SYNC pulses. SYNC==low may only occur when the associated CLOCK is high.
Tn	Min. 200 ns	Delay between SHY and start row readout

Figure 18. and Table 9. illustrate the timing constraints of the row initialization/ blanking sequence.

- The EOS_X pulse flags the end of the scanning of previous line, and should be considered as a diagnostic means only. The blanking sequence could start earlier or later.

- The next row (=line) is selected after the falling edge of CLK_YR and CLK_YL,
- The column amplifiers receive the signals on the pixels array columns buses when SHY is low (transparent).
- The SIN pulse (high) forces the column amplifiers in an “offset nulling" state.
- After 3 us, the column amplifiers have reached offset-free equilibrium, and the SIN pulse is brought low again. The pixel's signal level is thus stored in the column amplifier.
- After that the pixels in the selected row (line) are be reset (first pulse on RESET).
- Consequently the reset level is frozen in the column amplifiers when SHY goes high. Both signal level and reset level have now been applied to the column amplifiers. The sample hold (SHY) guarantees that this information will not change anymore during readout of the line.
- Now, the row is ready for readout. A pulse on SYNC_X must be given to start the row readout. SYNC_X initiates the X-direction scanning register. The scanning itself is controlled by CLOCK_X.
- During the beginning of the row readout, or possibly before, the RESET pulse for the electronic shutter (ES) must be given, if the ES is used. This is a pulse on RESET together with a high level on L/R. If the ES is not used, L/R remains low and the second RESET pulse is not generated.

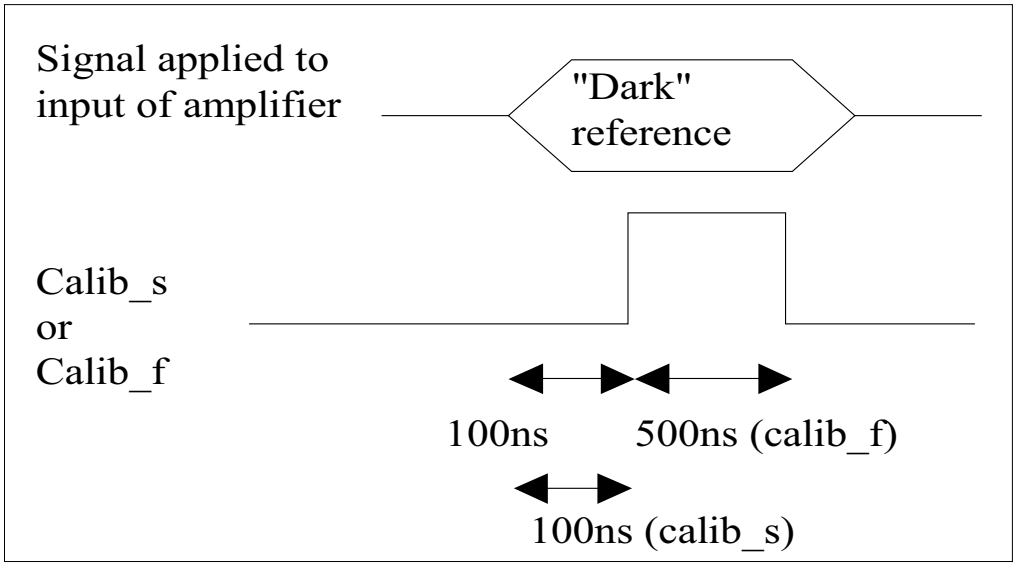
During some or the entire row blanking times, the output amplifier can be calibrated.

If the slow calibration method is used, pulse the 'CALIB_S' pin once per line. The calibration happens on the rising edge of the pulse.

If the fast calibration is used, the 'CALIB_F' should be pulsed during the row blanking time of the first row only. This calibration happens during the time that the pulse is high.

During this calibration, the input applied to the amplifier must be the dark reference, which can either be the built-in electrical dark reference, or an external dark reference on the pin EXTIN.

Figure 19. Pulse on 'CALIB_F'& 'UNITYGAIN' to be given once per frame, or on CALIB_S once per line



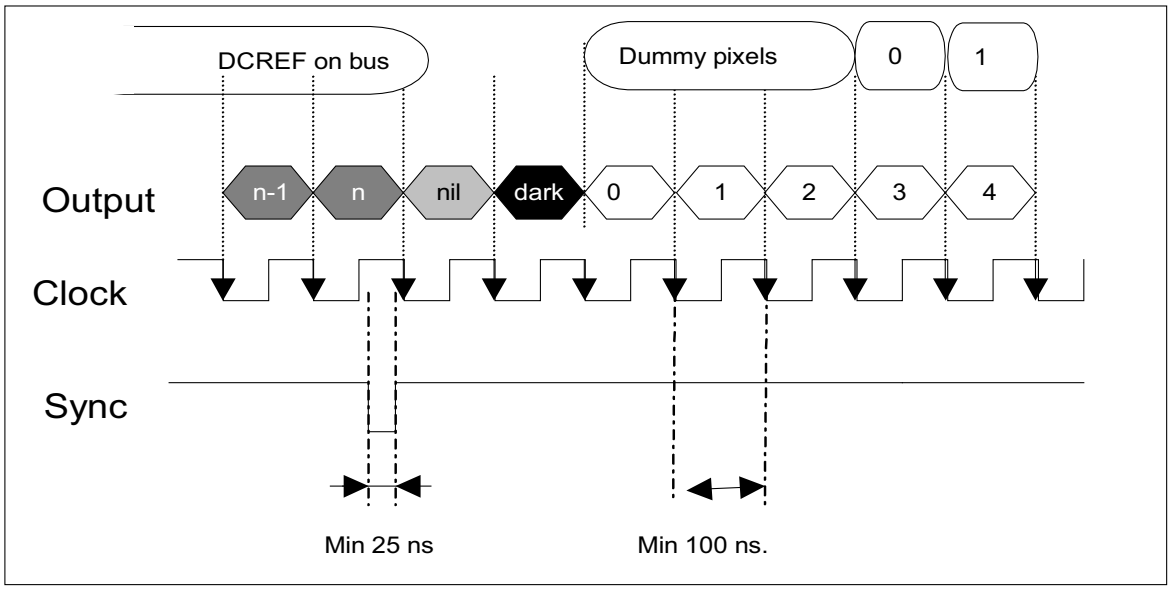
The X-direction shift register

The X shift register behaves like the Y shift registers.

The sequence if initiated by SYNC_X, which should occur when CLOCK_X is high. As CLOCK_X is halted during the blanking time, the SYNC_X pulse could occur anywhere, and be taken equal to some other pulse (e.g. CLOCK_Y).

The first real (dummy) pixel is read out after the 3rd falling edge on the clock. Dummy pixels are perfectly operational pixels, but are added to shield the "real" pixels from the cross talk of the periphery.

Figure 20. Timing of X shift register and pixels read-out



On-chip generated electrical dark references.

The sensor outputs a electrical dark reference level after the 2nd falling edge on the clock (after sync).

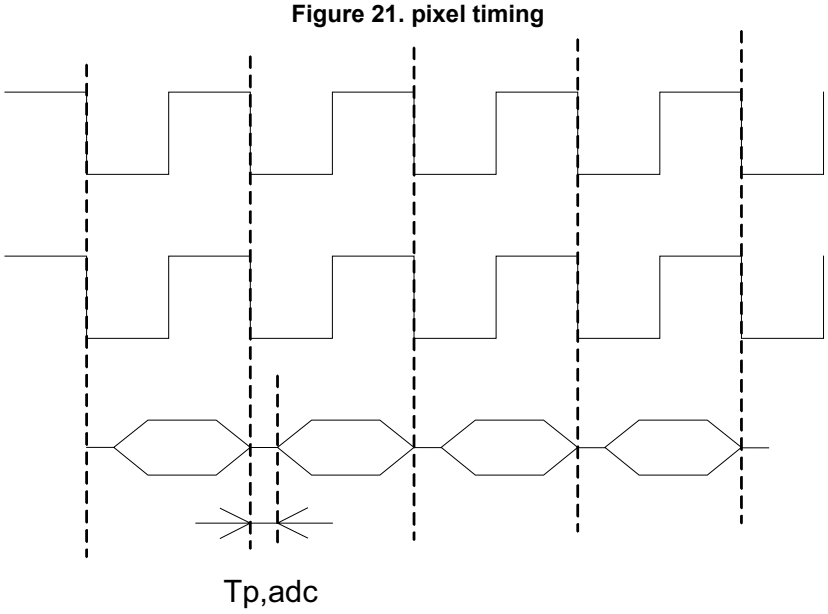
At the end of the row readout, after EOS_X becomes low, the sensor outputs the electrical dark reference voltage also, and it remains present on the on the readout bus until the SIN goes high.

Note that if the X-register is reset before the EOS is reached, the dark reference is not put on the bus. Use the dark reference of the beginning of the line instead.

Pixel readout

The same continuous 10 MHz clock drives CLK_ADC and CLK_X. On the falling edge of CLK_X, a new pixel is selected and propagates to the output amplifier. At the same time, the ADC input is frozen by the falling edge on CLK_ADC. The digital output has a delay of one pixel compared to the analog signal. The digital output becomes valid between 25 to 50 ns after the falling edge on CLK_ADC.

Figure 21. pixel timing

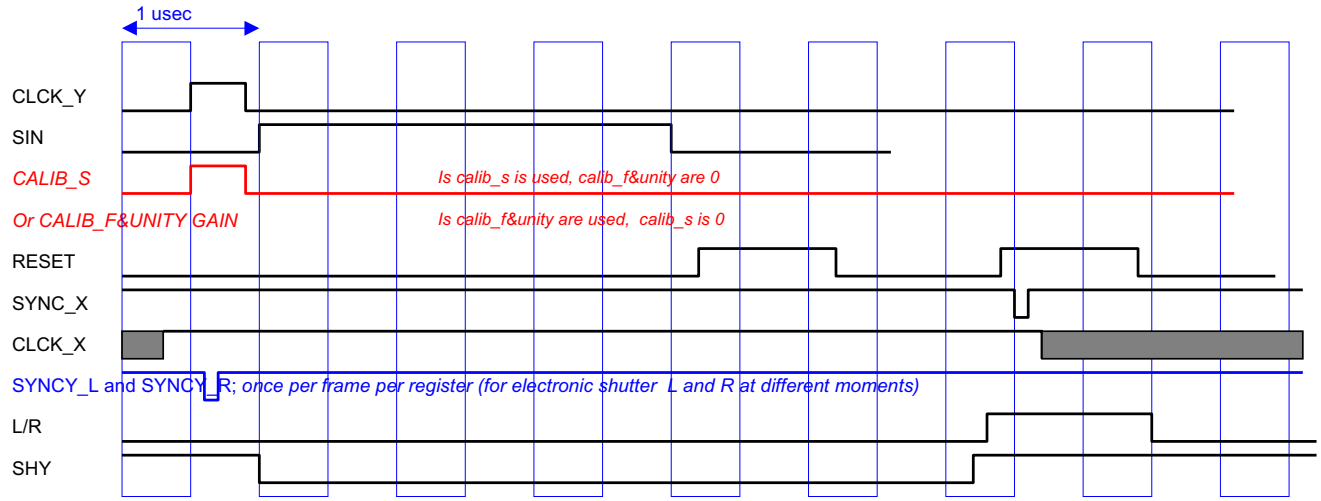


If the end of a row is reached, the sensor outputs an end-of-scan (EOS) pulse during one pulse period. And the electrical black reference level appears at the output for all successive pulses. So, the same 10 MHz clock can drive CLK_X and CLK_ADC.

Example: timing used on the IBIS4 breadboard

The next figure is the timing as used in the IBIS4 breadboard version 12 jan 2000. In this baseline only CALIB_F is used (pulsing once per frame). CALIB_S (pulse every line) is shown as reference, but is actually not used in the baseline. The UNITY_GAIN pulse is identical to CALIB_F.

Figure 22. pulse sequence used in IBIS4 breadboard v. jan 2000



Illumination control

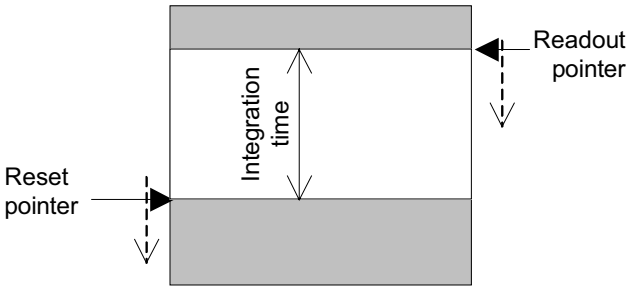
There are two means of controlling the illumination level electrically. For high light levels, there is an electronic shutter. For low light levels, the output signal can be amplified by controlling the output amplifier gain. The offset level of the signal can also be controlled digitally.

"Rolling curtain" electronic shutter

The electronic shutter can reduce the integration time (= exposure time). This is achieved by an additional reset pulse every frame. In this way, the integration time is reduced to a fraction of the frame readout time.

There are two Y shift registers. One of them points at the row that is currently being read out. The other shift register points at the row that is currently being reset. Both pointers are shifted by the same Y-clock and move over the focal plane. The integration time is set by the delay between both pointers.

Figure 23. Schematic representation of the curtain type electronic shutter



This is a so-called 'rolling curtain'-type shutter. It 'rolls' over the focal plane.

The left and right shift registers can be used both for pointing to the row that is readout or the row that is reset. The shift register that is active for readout or reset is selected by the signal on L/R. In the above timing diagrams, we use the R shift register for readout, and the L shift register for electronic shutter reset. We call them the readout shift register and reset shift register.

The integration time is controlled by the delay between the SYNCY_L and SYNCY_R pulse. The shorter this delay, the shorter the integration time and the smaller the output signal will be.

If the electronic shutter is not used, the L/R signal is not pulsed. The integration time is then equal to the frame readout time.

For proper operation of the ES, the CLOCK_Y must come as an uninterrupted pulse train. Also during the dead time between frames the CLOCK_Y must be clocked. The reason is that each line should see the same elapsed time between the "ES-reset" and the reset of the line being read-out. If the CLOCK_Y is halted, the lines between the two pointers will have a longer effective integration time, and appear brighter.

Gain control

For low illumination levels, the electronic shutter is not used - or set to its maximal value. Longer integration times can only be obtained by decreasing the frame rate. As an alternative or in complement, one can increase the output amplifier gain.

The gain is controlled by a 4-bit word. Gain values vary between 1.2 and 16, and on an exponential scale, as the F-stops of a lens.

Of course, increasing the signal amplitude by increasing the gain, will also increase the noise level. The apparent increase of sensitivity is at the cost of a lower dynamic range.

Offset level adjustment

The offset level of the output signal is set by a 4-bit digital word. The offset level voltage is selected between VLOW_DAC and VHIGH_DAC on 16 taps.

"Double slope" or "High-dynamic range" mode

IBIS4-1300 has a feature to increase the dynamic range. The pixel response can be extended over a larger range of light intensities by using a "dual slope integration" (patents pending). This is obtained by the addition of charge packets from a long and a short integration time in the pixel during the same frame time.

Figure 24. response curve of the pixels in dual slope integration

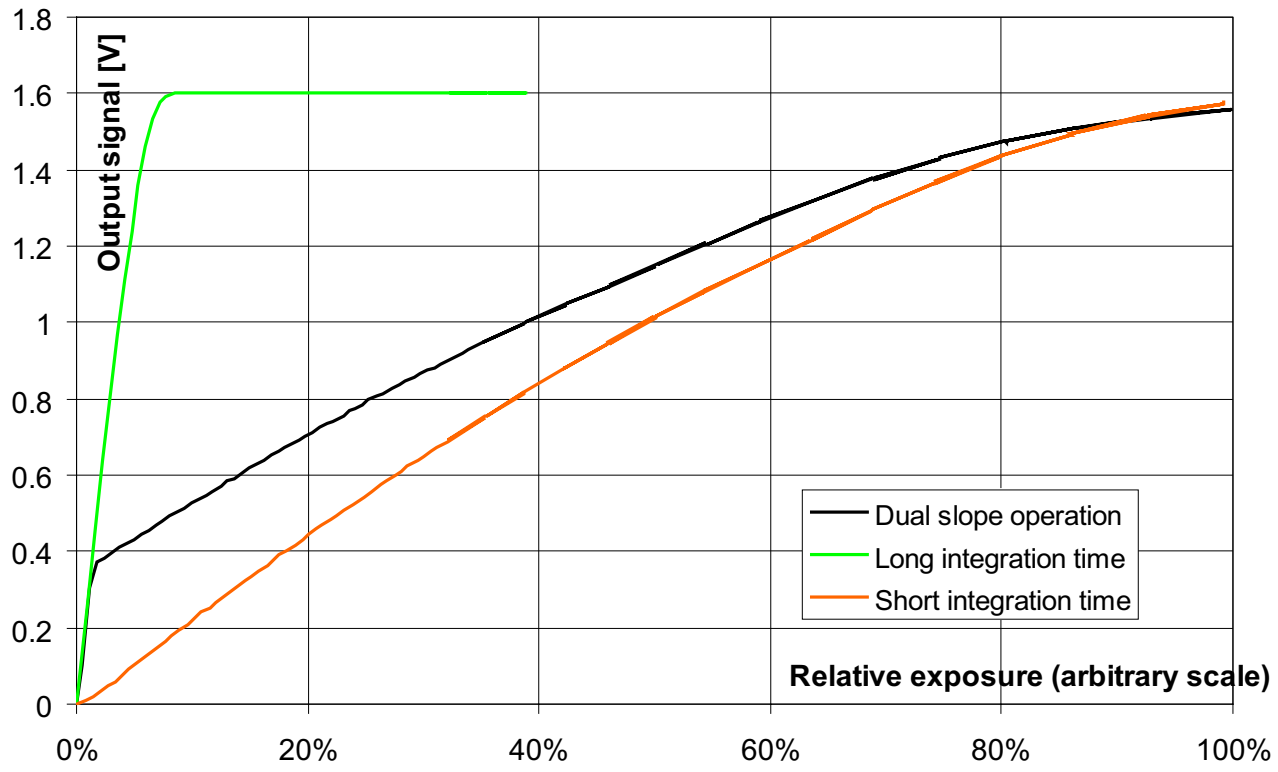


Fig.24 shows the response curve of a pixel in dual slope integration mode. The curve also shows the response of the same pixel in linear integration mode, with a long and short integration time, at the same light levels.

Dual slope integration is obtained by

- Feeding a lower supply voltage to VDD_RESETL. E.g. apply 4 to 4.5 Volts. The difference between this voltage and VDD determines the range of the high sensitivity, thus the output signal level at which the transition between high and low sensitivity occurs.
- Put the amplifier gain to the lowest value where the analog output swing covers the ADC's digital input swing. Increasing the amplification too much will likely boost the high sensitivity part over the whole ADC range.
- The electronic shutter determines the ratio of integration times of the two slopes. The high sensitivity ramp corresponds to "no electronic shutter", thus maximal integration time. The low sensitivity ramp corresponds to the electronics shutter value that would have been obtained in normal operation.

These example images are found at http://www.fillfactory.com/htm/technology/htm/dual-slope.htm

Figure 25. Linear long exposure time



Figure 26. Linear short exposure time



Figure 27. Double slope integration



Electrical parameters

DC voltages

VDD and GND:

Nominal VDD-GND is 5V DC.

Overall current consumption for the different parts

- imager core + output amplifier analog
- imager core digital
- ADC analog
- ADC digital

Are quoted in the datasheets

The sensor works properly when using a 7805 type of regulator.

Decoupling VDD to GND must happen close to the IC.

Other applied DC voltages

Should be clean as the VDD. Can be derived by resistive division of VDD-GND, and decoupled to VDD or GND (as indicated)

External Resistors

Are used as current mirror settings. Should be decoupled to the opposite rail voltage as the connection of the resistor (thus: if the resistor is tied to VDD, the capacitor is tied to GND). In practice the decoupling can be omitted for almost all signals - to be experimented.

Input / output

Digital inputs:

Clean rail to rail CMOS levels. 10%-90% rise and fall times between 10 ns and 40 ns

Digital outputs:

Deliver CMOS level, able to drive 40 pF capacitive loads

Analog output of imager core

Designed to drive a 40 pF capacitive load

Analog input of ADC

Is equivalent to a capacitive load of typ. 15 pF.

Pin configuration

Pin list

Signal type symbols	
A	Analog
D	Digital
W	Word bit

I/O Symbols	
I	Input
O	Output
P	Power supply
G	Ground

No.	Name	Type	I/O	Description	Signal
1	Nbiasarray	A	I	1MEG to VDD and decouple to GND	Pixel source follower bias current
2	pbias2	A	I	1MEG to GND and decouple to VDD	Column amp 1st source follower (after SHY) bias current
3	Pbias	A	I	1MEG to GND and decouple to VDD	Column amp current source bias current
4	xmux_nbias	A	I	100K to VDD and decouple to GND	X-multiplexing bias current (/6)
5	Sync_yr\	D	I	low active (0=sync)	0 = reset right shift register
6	clk_yr	D	I	Shifts on falling edge	clock right shift register
7	Eos_yr\	D	O	Active low	low 1st clk_yr pulse after last row
8	Eos_x\	D	O	Active low	low 1st clk_x pulse after last active column
9	Selextin	D	I	input selector for output amplifier	1 = external input; [0] = imager core
10	Gnd	A	G	Analog GND	
11	Vdd	A	P	Analog VDD	+ 5 V DC
12	Extin	A	I	external input to output amplifier	
13	Output	A	O	analog output of imager core	Connect to in_adc (p73)
14	Vlow_dac	A	I	low reference voltage offset DAC	+/- 1 V
15	Vhigh_dac	A	I	high reference voltage offset DAC	+/- 2.5 V
16	Calib_s	D	I	Slow dark offset level adjustment	0: connect to cap (st2) and in- (st1) 1: connect to rdac (st2) and output (st1)
17	gc_bit0	W	I	Lsb	gain control output amplifier
18	gc_bit1	W	I		
19	gc_bit2	W	I		
20	gc_bit3	W	I	Msb	
21	Unitygain	D	I	sets output amplifier in unity gain	High active
22	Calib_f	D	I	fast dark offset level calibration	High active
23	Dac_b3	W	I	Msb	dac control for black offset level
24	Dac_b2	W	I		dac control for black offset level
25	Dac_b1	W	I		dac control for black offset level
26	Dac_b0	W	I	Lsb	dac control for black offset level
27	Nbias_oamp	A	I	100K to VDD and decouple to GND	output amplifier bias current
28	Sync_x\	D	I	low active (0=sync)	0 = reset X shift register

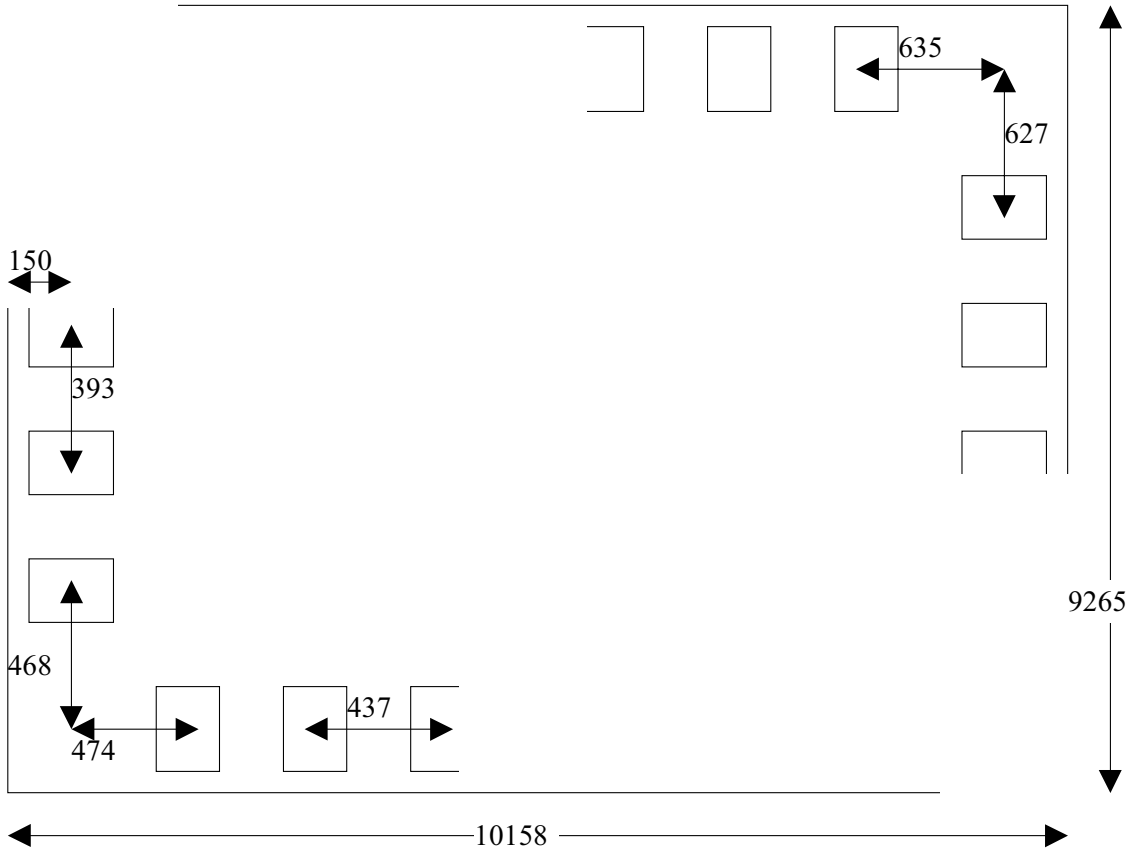
No.	Name	Type	I/O	Description	Signal
29	clk_x	D	I	Shifts on falling edge	clock X shift register
30	shy	D	I	Column parallel track and hold	1 = hold; 0 = track
31	dccon	A	I	control voltage for DC reference generation	Connect to GND (default)
32	dcref	A	O	reference voltage	Should be +/- 1.2 V, depends on dccon
33	gnd	A	G		
34	vdd	A	P		
35	sin	D	I	Column amplifier calibration signal	1 = calibrate, see timing diagram
36	sync_y\l	D	I	0 = start left shift register	low active (0=sync)
37	clk_yl	D	I	clock left shift register	Shifts on falling edge
38	eos_yl\	D	O	low 1st clk_yl pulse after last row	Active low
39	bitinvert	D	I	High active, 1 = invert bits	inverts ADC output bits
40	select	D	I	High active	selects row indicated by left/right shift register
41	reset	D	I	High active	resets row indicated by left/right shift register
42	d9	W	O	MSB	ADC output
43	d8	W	O		
44	d7	W	O		
45	d6	W	O		
46	d5	W	O		
47	d4	W	O		
48	d3	W	O		
49	d2	W	O		
50	d1	W	O		
51	d0	W	O	LSB	
52	gnd	A	G		
53	vdd	A	P	+ 5 V DC	
54	gnd_ab	A	G	Anti-blooming drain voltage	GND or +1V for improved anti-blooming
55	vdd_array	A	P	+ 5 V DC	Pixel power supply
56	vdd_dig	D	P	+ 5 V DC	ADC digital power supply
57	gnd_dig	D	G		ADC ground of digital circuits
58	vdd_an	A	P	+ 5 V DC	ADC analog power supply
59	vdd_resetl	A	P	5 V DC default (5.5 V for large output swing) 4…4.5 V for double slope mode	VDD for reset by left shift register
60	gnd_an	A	G		ADC ground of analog circuits
61	vhigh_adc	A	I	+ 4 V DC	High ADC reference voltage

No.	Name	Type	I/O	Description	Signal
62	clk_adc	D	I	ADC Clock	Converts on falling edge
63	tri_adc	D	I	ADC output tristate control	1=tristate; 0=output
64	pbiasdig1	A	I	100K to GND and decouple to VDD	current bias for comparator after encoder
65	pbiasencload	A	I	100K to GND and decouple to VDD	current bias for encoder
66	pbiasdig2	A	I	100K to GND and decouple to VDD	current bias for digital logic in columns
67	nonlinear	D	I	high active (1 = non-linear conversion)	control for non-linear behavior of sensor
68	n.c.			not connected	
69	nbiasana2	A	I	100K to VDD and decouple to GND	bias current 2nd comparator stage
70	nbiasana	A	I	100K to VDD and decouple to GND	bias current 1st comparator stage
71	vlow_adc	A	I	+ 2 V DC, +-2 K between P71 and P61	Low ADC reference voltage
72	gnd_an	A	G		ADC ground of analog circuits
73	in_adc	A	I	Converts between vlow and vhigh (2-4V)	ADC input
74	vdd_an	A	P	+ 5 V DC	ADC analog power supply
75	gnd_dig	D	G		ADC ground of digital circuits
76	vdd_dig	D	P	+ 5 V DC	ADC digital power supply
77	vdd	A	P	+ 5 V DC	
78	gnd	A	G		
79	vdd_resetr	A	P	5 V DC default (5.5 for large signal swing)	Power supply for reset by right (readout) shift register
80	L/R\	D	I	1=left; 0=right	Selects left or right shift register for 'select' and 'reset'
81	Pixel diode	A	O	groups current of 24 x 18 pixels	Test structure for spectral response measurement of pixels
82	Photodiode	A	O	168x126 um2 (eq. 24 x 18 pixels)	Test structure for spectral response measurement of photodiode
83	clip	A	I	Clips if output > 'clip' - Vth (PMOS)	Clipping voltage for output amplifier
84	subsmpl	D	I	high active, 1 = subsampling	Selects viewfinder mode (1:4 = 320 x 256)

Bonding pad geometry for the IBIS4-1300

- The 84 pins are distributed evenly around the perimeter of the Chip. At each edge there are 21 pins. Pin 1 is (in this drawing) in the middle of the left edge.
- The opening in the bonding pads (the useful area for bonding) is 200 x 150 um.
- The centers of the bonding pads are at all four edges at 150 um distance from the nominal chip border.
- The scribe line (=the spacing between the nominal borders of neighboring chips) is 250 um.
- The bonding pad pitch is 437 um in X-direction
- The bonding pad pitch in Y-direction is 393 um

- Relative position of pads in corners: see next figure (measures in um).



Color filter geometry

Sensors with diagonal pattern have

- -pixel (1,1) is RED
- -first line sequence is BGRBGR
- -second line sequence is RBGRBG

B

sensors with Bayer pattern have

- -pixel (1,1) is GREEN
- -first line sequence is .GRGRG
- -second line sequence is .BGBGB

Package

84 pins ceramic LCC package (JLCC also available)

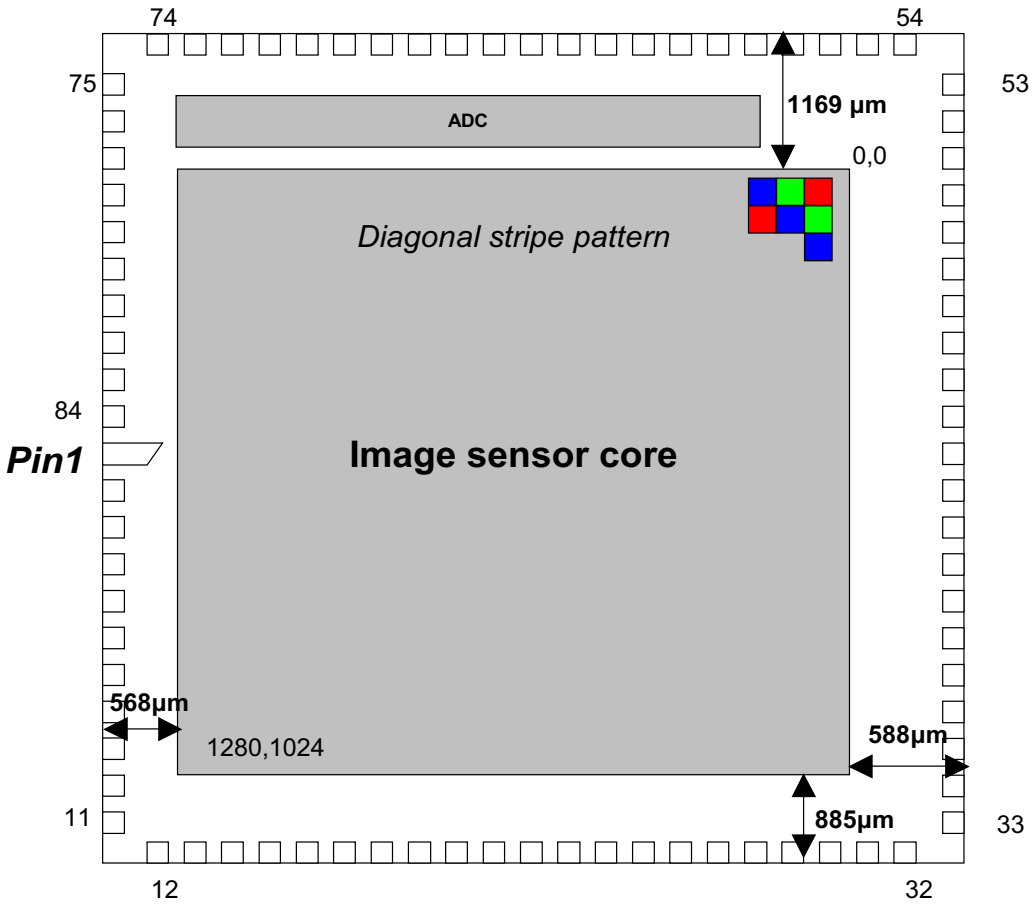
Standard 0.04 inch pitch outline

0.46" square cavity

Die thickness nominally 711 um +- 50um

Clearance from top of die to bottom of glass lid: 400um nominally

Figure 28. Pin layout and package, top view



Cover glass

Size 18x18 mm for JLCC& LCC

Color sensor

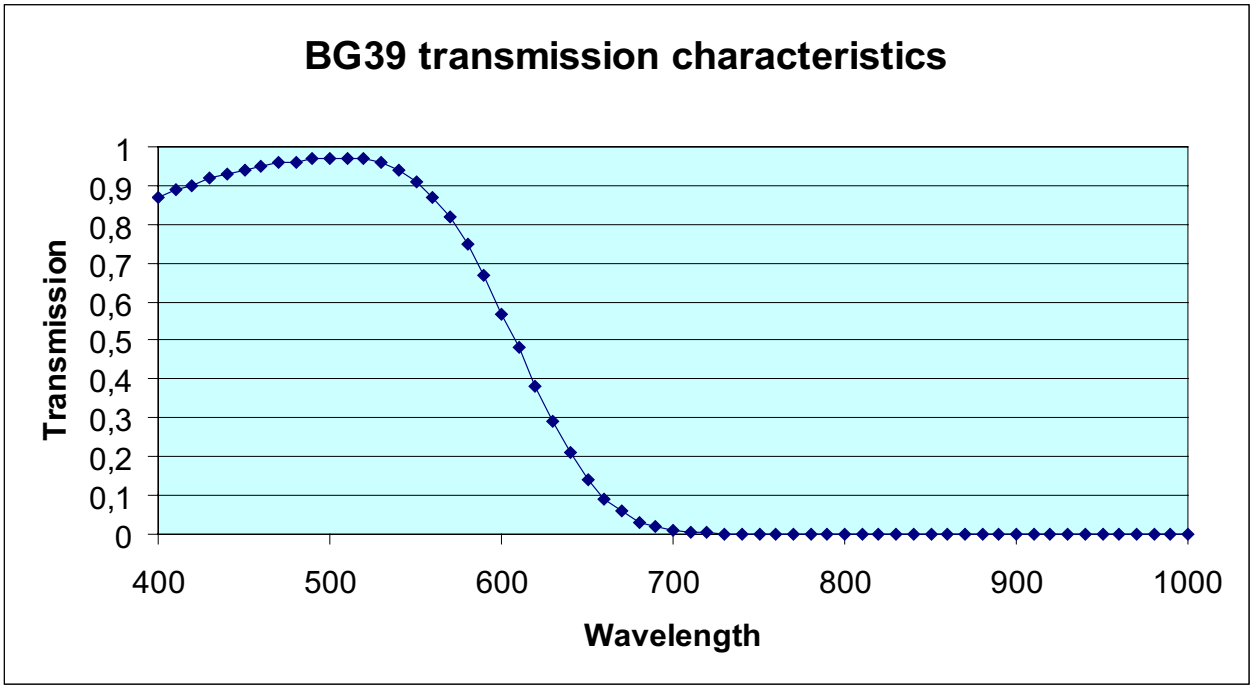
Refractive index: 1,55

Thickness: 0,75+-0.05 mm

Material: BG39

This material acts a NIR cut-off filter. The transmission characteristics are given in the figure below. The data used to create the transmission curve of the BG39 material can be obtained as an excel file upon simple request to info@fillfactory.com.

Figure 29. Transmission characteristics of the BG39 glass used as NIR cut-off filter for the IBIS4-1300 color image sensors



Monochrome sensor

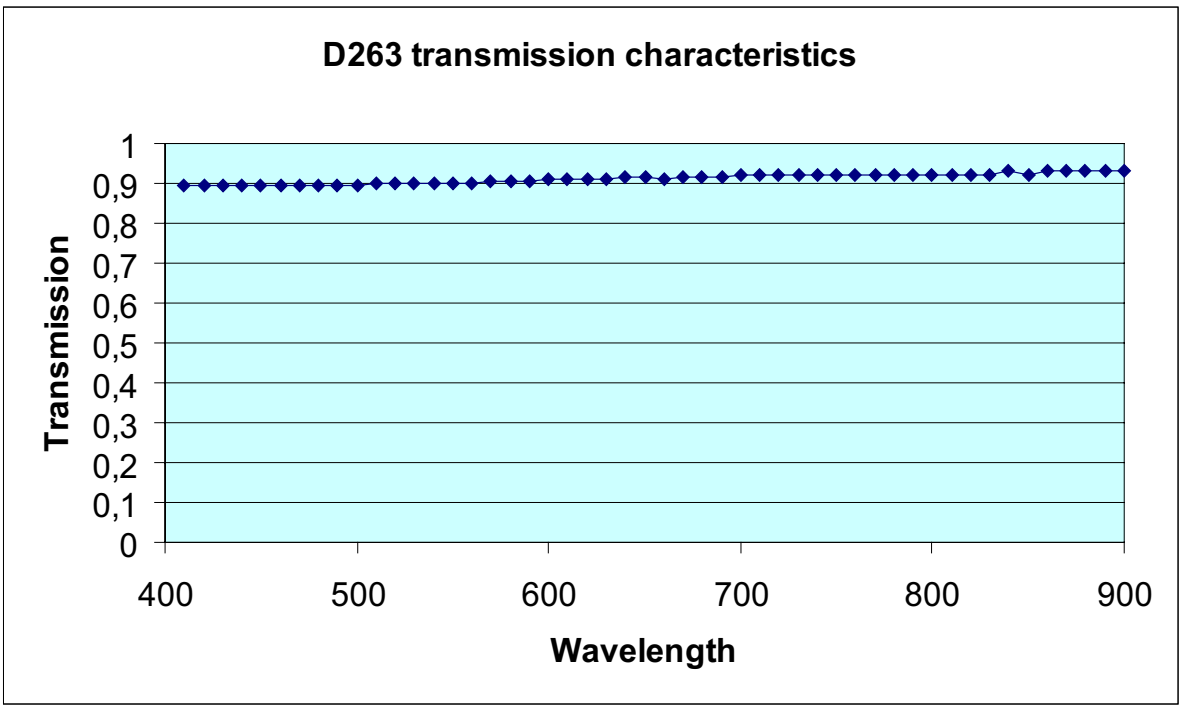
Refractive index: 1,52

Thickness: 0,55+-0.05 mm

Material: D263

The transmission characteristics are given in the figure below.

Figure 30. Transmission characteristics of the D263 glass used as protective cover for the IBIS4-1300 monochrome image sensors



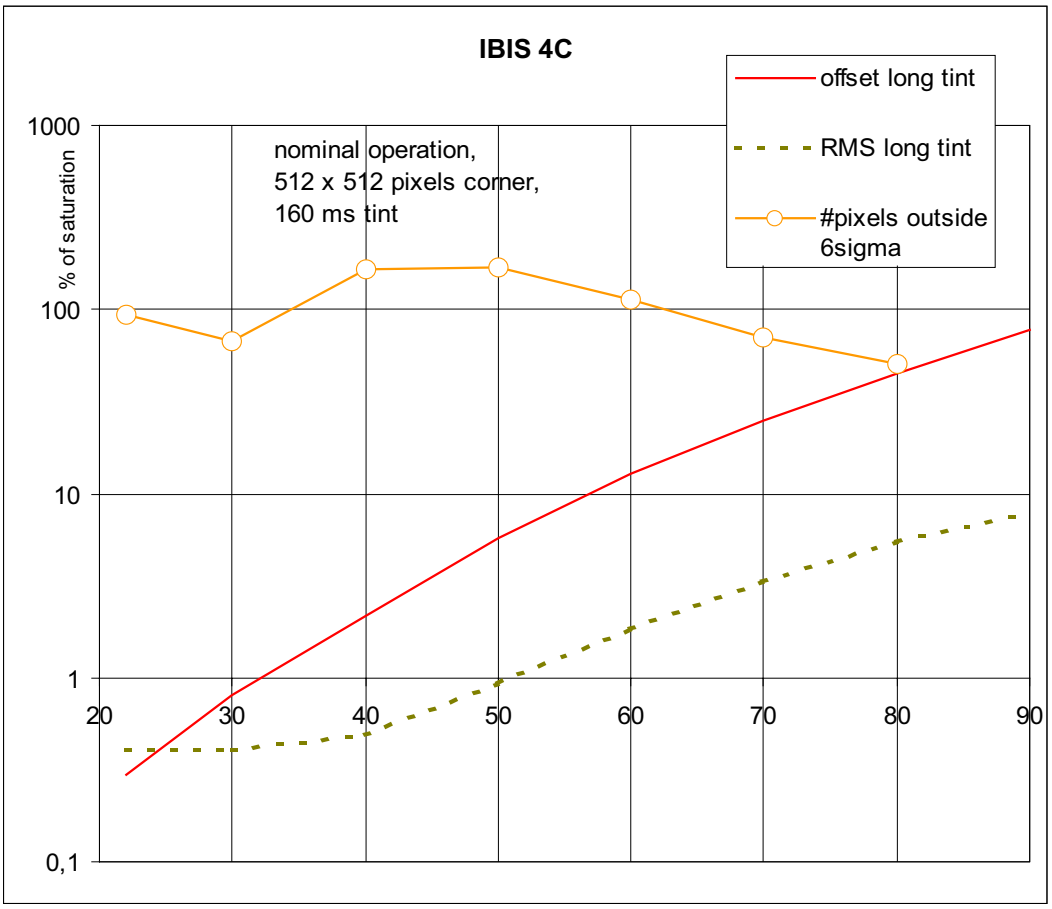
Ordering Information

Table 10. FillFactory and Cypress part numbers

FillFactory Part Number	Cypress Semiconductor Part Number
IBIS4-1300-C1-2	CYII4SD1300AA-QAC - Preliminary
IBIS4-1300-M-1	CYII4SM1300AA-HBC - Preliminary
IBIS4-1300-M-2	CYII4SM1300AA-QBC - Preliminary

FAQ

Temperature dependence of dark signal



The above graph is measured on an IBIS4-1300 under nominal operation, using breadboard. This particular sensor has about 100 "bad pixels" at RT.

Average offset (=dark signal) and RMS (=FPN of dark signal) are measured versus temperature. Offset is referred to the "short tint" offset at 20 C. Integration time was 160 ms (= "long tint").

Y-axis is the output signal (100% = ADC range)

Useful range of "double slope"

Which total dynamic range can reasonably be obtained with the dual slope feature of the IBIS4-1300?

Assuming that the "regular" S/N is 2000:1, and that one can put the knee point halfway the voltage range, the each piecewise linear halve has 1000:1 S/N. If the ratio between slopes is a, then the total dynamic range becomes (1000+a*1000):1.

Example, is a=10, then the total dynamic range becomes 11000:1.

In practice, acceptable images are obtained with a up to 10. Larger a's are useable, but near the knee, contrast artifacts become annoying.

Skipping rows or columns

Although these modes are not described in the datasheets, it is possible to skip rows or columns by simply applying additional CLK_YR + CLR_YL, or CLK_X pulses. The maximum clock frequency is not documented. But it is probable that one can reach at least 10 MHz in Y and 40 MHz in X.

Disclaimer

FillFactory image sensors are only warranted to meet the specifications as described in the production data sheet. Specifications are subject to change without notice.

Document History Page

Document Title: 1.3 MPxl Rolling Shutter CMOS Image Sensor Document Number: 38-05707				
REV.	**ECN.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	310213	See ECN	SIL	Initial Cypress release
*A	509557	See ECN	QGS	Converted to Frame file
*B	642577	See ECN	FPW	Ordering information update