IBC Module

IB0xxE120T40xx-xx

4:1 Intermediate Bus Converter Module: Up to 500 W Output



Size:
2.30 x 0.9 x 0.38 in
58,4 x 22,9 x 9,5 mm

Applications

- Enterprise networks
- Optical access networks
- Storage networks
- Automated test equipment

Features

- Input: 36 – 60 Vdc
  (38 – 55 Vdc for IB048x)
- Output: 12.0 Vdc at 48 Vin
- Output current up to 40 A
- Output power: up to 500 W [A]
- 2,250 Vdc isolation
  (1,500 Vdc isolation for IB048x)
- 97.8% peak efficiency
- Low profile: 0.38" height above board
- Industry standard 1/8 Brick pinout
- Sine Amplitude Converter
- Low noise 1 MHz ZVS/ZCS

[A] For lower power applications see 300 W model IB0xxE120T32xx-xx

Product Overview

The Intermediate Bus Converter (IBC) Module is a very efficient, low profile, isolated, fixed ratio converter for power system applications in enterprise and optical access networks. Rated at up to 360 W from 38 Vin and up to 500 W from 50 to 55 Vin, the IBC conforms to an industry standard eighth brick footprint while supplying the power of a quarter brick. Its leading efficiency enables full load operation at 55°C with only 200 LFM airflow. Its small cross section facilitates unimpeded airflow — above and below its thin body — to minimize the temperature rise of downstream components.

PART NUMBER DESIGNATION

Function		Input Voltage			Package	Output Voltage (Nom.) x 10			Temperature Grade	Output Current		Enable Logic	Pin Length		Options	
I	B	0	x	x	E	1	2	0	T	4	0	x	x	-	x	x

- **IB** = Intermediate Bus Converter
- **048** = 38 - 55 Vdc; **050** = 36 - 60 Vdc; **054** = 36 - 60 Vdc* (*w/operating transient to 75 Vdc)
- **E** = Eighth Brick Format
- **120** = (V_{OUT} nominal @ V_{IN} = 48 Vdc) X 10 (4:1 transfer ratio)
- **T** = -40°C ≤ $T_{OPERATING}$ ≤ +100°C; -40°C ≤ $T_{STORAGE}$ ≤ +125°C
- **40** = Max Rated Output Current
- **N** = Negative; **P** = Positive
- **1** = 0.145 in; **2** = 0.210 in; **3** = 0.180 in
- **00** = Open frame

SPECIFICATIONS

All specifications valid at 48 V_{IN}, 100% rated load and 25°C ambient, unless otherwise indicated.

Absolute Maximum Ratings

	Min	Max	Unit	Notes
Input voltage (+In to –In)	-0.5	75	Vdc	See Input Range Specific Characteristics for details
Input voltage slew rate		5	V/µs	
EN to –IN	-0.5	20	Vdc	
Output voltage (+Out to –Out)	-0.5	See note	Vdc	See OVP setpoint max
Output current		40	A	Pout ≤ 500 W
Dielectric withstand (input to output)		2,250 (1,500 for IB048x)	Vdc	1 min.
Temperature				
Operating junction	-40	125	°C	Hottest Semiconductor
Storage	-55	125	°C	

Electrical Characteristics

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
INPUT RANGE SPECIFIC CHARACTERISTICS						
IB048E120T40xx-xx						
Operating input voltage			38	48	55	Vdc
Non-operating input surge withstand		<100 ms			75	Vdc
Operating input dv/dt			0.003		5	V/µs
Undervoltage protection						
Turn-on			33		38	Vdc
Turn-off			31		36	Vdc
Turn-on/Turn-off hysteresis			2			Vdc
Time constant					7	µs
Undervoltage blanking time		UV blanking time is enabled after start up	50	100	200	µs
Overvoltage protection						
Turn-off			60		64	Vdc
Turn-on			55		64	Vdc
Time constant					4	µs
Peak short circuit input current					30	A
DC Output voltage band		No load, over Vin range	9.5	12.0	13.75	Vdc
Output OVP set point		Module will shut down	16.2			Vdc
Dielectric withstand		Input to output; 1 min	1,500			Vdc
Insulation resistance		Input to output		30		MΩ

SPECIFICATIONS (CONT.)

All specifications valid at 48 V_{IN}, 100% rated load and 25°C ambient, unless otherwise indicated.

Electrical Characteristics *(Continued)*

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
INPUT RANGE SPECIFIC CHARACTERISTICS CONT.						
IB050E120T40xx-xx						
Operating input voltage			36	48	60	Vdc
Non-operating input surge withstand		<100 ms			75	Vdc
Operating input dv/dt			0.003		5	V/µs
Undervoltage protection						
Turn-on			31		36	Vdc
Turn-off			29		34	Vdc
Turn-on/Turn-off hysteresis			2			Vdc
Time constant					7	µs
Undervoltage blanking time		UV blanking time is enabled after start up	50	100	200	µs
Overvoltage protection						
Turn-off			65		69	Vdc
Turn-on			60		69	Vdc
Time constant					4	µs
Peak short circuit input current					40	A
DC Output voltage band		No load, over Vin range	9	12	15	Vdc
Output OVP set point		Module will shut down	16.2			Vdc
Dielectric withstand		Input to output; 1 min	2,250			Vdc
Insulation resistance		Input to output		30		MΩ
IB054E120T40xx-xx						
Operating input voltage			36	48	60	Vdc
Operating input surge withstand		<100 ms			75	Vdc
Operating input dv/dt			0.003		5	V/µs
Undervoltage protection						
Turn-on			31		36	Vdc
Turn-off			29		34	Vdc
Turn-on/Turn-off hysteresis			2			Vdc
Time constant					7	µs
Undervoltage blanking time		UV blanking time is enabled after start up	50	100	200	µs
Overvoltage protection						
Turn-off			76		79.5	Vdc
Turn-on			75		78	Vdc
Time constant					4	µs
Peak short circuit input current					30	A
DC Output voltage band		No load, over Vin range	9	12	15	Vdc
Output OVP set point		Module will shut down	16.2			Vdc
Dielectric withstand		Input to output; 1 min	2,250			Vdc
Insulation resistance		Input to output		30		MΩ
COMMON INPUT SPECIFICATIONS						
Turn ON delay						
Start up inhibit		V_{IN} reaching turn-on voltage to enable function operational, see Figure 6	20	25	30	ms
Turn-on delay		Enable to 10% V_{OUT}; pre-applied V_{IN}, see Figure 7, 0 load capacitance			50	µs

SPECIFICATIONS (CONT.)

All specifications valid at 48 V_{IN}, 100% rated load and 25°C ambient, unless otherwise indicated.

Electrical Characteristics *(Continued)*

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
COMMON INPUT SPECIFICATIONS CONT.						
Output voltage rise time		From 10% to 90% V_{OUT}, 10% load, 0 load capacitance. See Figure 8			50	µs
Restart turn-on delay		See page 12 for restart after EN pin disable			250	ms
No Load power dissipation						
Enabled				3.0	3.9	W
Disabled				0.17	2.4	W
Input current		Low line, full load			10.1	A
Inrush current overshoot		Using test circuit in Figure 21, 15% load, high line			18	A
Input reflected ripple current		At max power; Using test circuit in Figure 22, See Figure 5			400	mArms
Repetitive short circuit peak current					25	A
Internal input capacitance				8.8		µF
Internal input inductance				5		nH
Recommended external input capacitance		200 nH maximum source inductance	47		470	µF
OUTPUT						
Output power [a]			0		500	W
Output current					40	A
Output start up load		of Iout max, maximum output capacitance			15	%
Effective output resistance				4.8		mΩ
Line regulation (K factor)		$V_{OUT} = K \bullet V_{IN}$ @ no load	0.247	0.250	0.253	
Current share accuracy		Full power operation; See Parallel Operation on page 13; up to 3 units			10	%
Efficiency						
50% load		See Figure 1	97.4	97.8		%
Full load		See Figure 1	97.0	97.4		%
Internal output inductance				1.6		nH
Internal output capacitance				55		µF
Load capacitance			0		3000	µF
Output voltage ripple		20 MHz bandwidth (Figure 16), using test circuit in Figure 23		60	150	mVp-p
Output Overload protection threshold		Of Iout max., will not shutdown when started into max Cout; and 15% load Auto restart with duty cycle <10%	105		150	%
Over current protection time constant					1.2	ms
Short circuit current response time					1.5	µs
Switching frequency				1.0		MHz
Dyanmic response - Load		Load change: +/- 25% of I_{OUT} Max,				
Vo overshoot/undershoot		Slew rate (di/dt) = 1 A/µs.			100	mV
Vo response time		See Figures: 11-14		1		µs
Dyanmic response - Line		Line step of 5 V in 1 µs, within V_{IN} operating				
Vo overshoot		range. (C_{IN} = 500 uF, C_O = 350 uF) (Figure 15 illustrates similar converter response when subjected to a more severe line transient.)			1.25	V

[a] Does not exceed IPC-9592 derating guidelines. At 70°C ambient, full power operation may exceed IPC-9592 guidelines, but does not exceed component ratings, does not activate OTP and does not compromise reliability.

SPECIFICATIONS (CONT.)

Electrical Characteristics *(Continued)*

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
OUTPUT CONT.						
Pre-bias voltage		Unit will start up into a pre-bias voltage on the output.	0		15	Vdc

Control & Interface Specifications

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Enable (negative logic)		Referenced to –IN				
Module enable threshold			0.8			Vdc
Module enable current		V_{EN} = 0.8 V		130	200	µA
Module disable threshold					2.4	Vdc
Module disable current		V_{EN} = 2.4 V			130	µA
Disable hysteresis				500		mV
Enable pin open circuit voltage				2.5	3.0	Vdc
EN to –IN resistance		Open circuit, 10 V applied between EN and -IN		35		kΩ
Enable (positive logic)		Referenced to –IN				
Module enable threshold			2.0	2.5	3.0	Vdc
Module disable threshold					1.45	Vdc
EN source current (operating)		V_{EN} = 5 V			2	mA
EN voltage (operating)			4.7	5	5.3	Vdc

General Characteristics

Conditions: 25°C case, 75% rated load and specified input voltage range unless otherwise specified.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
MTBF		Calculated per Telcordia SR-332, 40°C	1.0			Mhrs
Service life		Calculated at 30°C	7			Years
Over temperature shut down		T_J; Converter will reset when over temperature condition is removed	125	130	135	°C
Dielectric withstand		Input to output	1,500			Vdc
Insulation resistance		Input to output		30		MΩ
Mechanical						
Weight				0.71 / 20.3		oz/g
Length				2.30 /58.4		in/mm
Width				0.9/22.9		in/mm
Height above customer board				0.38/9.5		in/mm
Pin Solderability		Storage life for normal solderability			1	Years
Moisture Sensitivity Level	MSL	Not applicable, for wave soldering only	N/A			
Clearance to customer board		From lowest component on IBC	0.12/0.30			in/mm
Agency approvals		UL60950-1		cURus		
		EN60950-1, IEC60950-1		cTUVus		
Altitude, operating		Derate operating temp 1°C per 1,000 feet above sea level	-500		10,000	Feet
Relative humidity, Operating		Non condensing	10		90	%
RoHS compliance		Compatible with RoHS directive 2002/95/EC				

SPECIFICATIONS (CONT.)

IPC-9592A, Based on Class II Category 2 the following detail is applicable. – Pre-conditioning required

Environmental Qualification

Test Description	Test Detail	Quantity Tested
5.2.3 HALT (Highly Accelerated Life testing)	Low Temp	3
	High Temp	3
	Rapid Thermal Cycling	3
	6 DOF Random Vibration Test	3
	Input Voltage Test	3
	Output Load Test	3
	Combined Stresses Test	3
5.2.4 THB (Temp. Humidity Bias)	(72 hr presoak required) 1000 hrs – Continuous Bias	30
5.2.5 HTOB (High Temp. Operating Bias)	Power cycle - On 42 minutes Off 1 minute, On 1 minute, Off 1 minute, On 1 minute, Off 1 minute, On 1 minute, Off 1 minute, On 1 minute, Off 10 minutes. Alternating between maximum and minimum operating Voltage every hour.	30
5.2.6 TC (Temp. Cycling)	700 cycles , 30 minute dwell at each extreme – 20C minimum ramp rate.	30
5.2.7 Power Cycling	Reference IPC-9592A	3
5.2.8 – 5.2.13 Shock and Vibration	Random Vibration – Operating IEC 60068-2-64 (normal operation vibration)	3
	Random Vibration Non-operating (transportation) IEC 60068-2-64	3
	Shock Operating - normal operation shock IEC 60068-2-27	3
	Free fall - IEC 60068-2-32	3
	Drop Test 1 full shipping container (box)	12
5.2.14 Other Environmental Tests	5.2.14.1 Corrosion Resistance – Not required	N/A
	5.2.14.2 Dust Resistance – Unpotted class II GR-1274-CORE	3
	5.2.14.3 SMT Attachment Reliability IPC-9701 - J-STD-002	3
	5.2.14.4 Through Hole solderability – J-STD-002	5
ESD Classification Testing	Sample size assumes CDM testing	12
Total Quantity (est.)		**161**

SPECIFICATIONS (CONT.)

WAVEFORMS

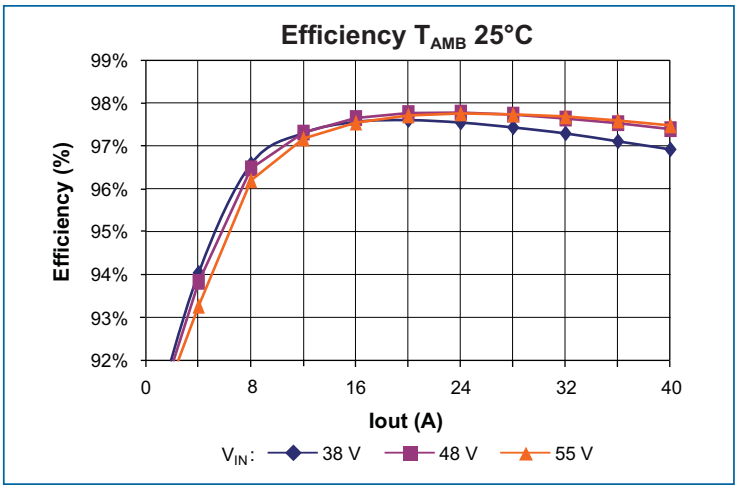


Figure 1 — Efficiency vs. output current, 25°C ambient

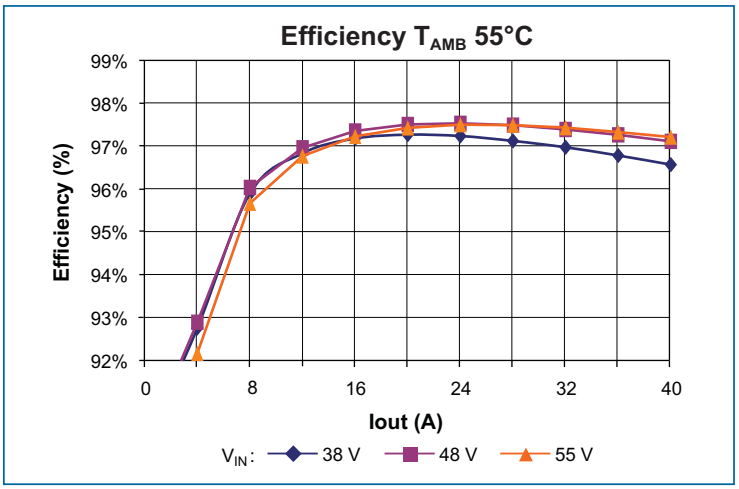


Figure 2 — Efficiency vs. output current, 55°C ambient

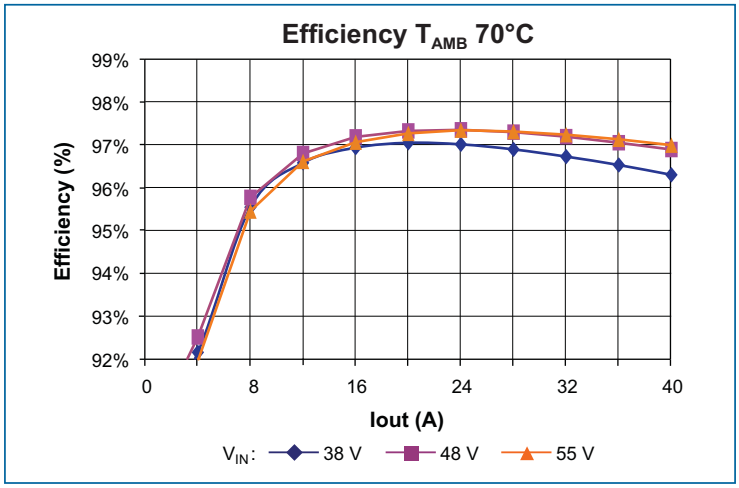


Figure 3 — Efficiency vs. output current, 70°C ambient

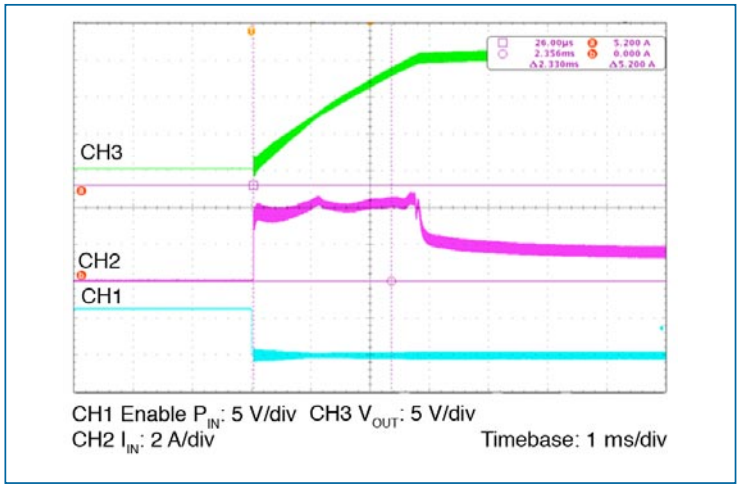


Figure 4 — Inrush current at high line 15% load; 5 A/div

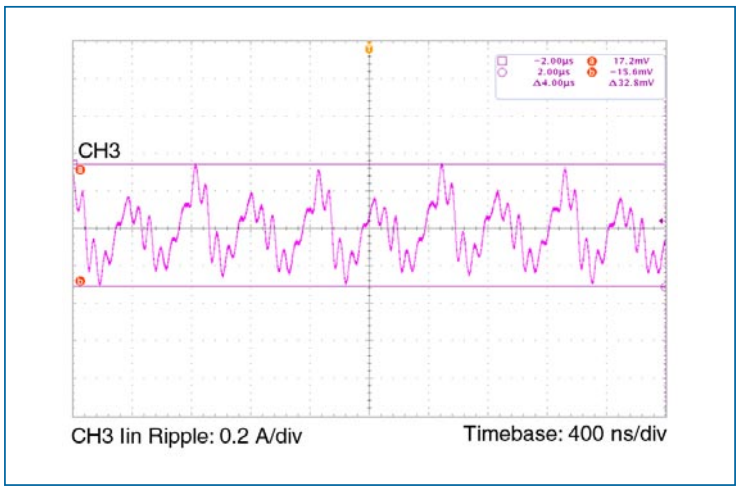


Figure 5 — Input reflected ripple current at nominal line, full load

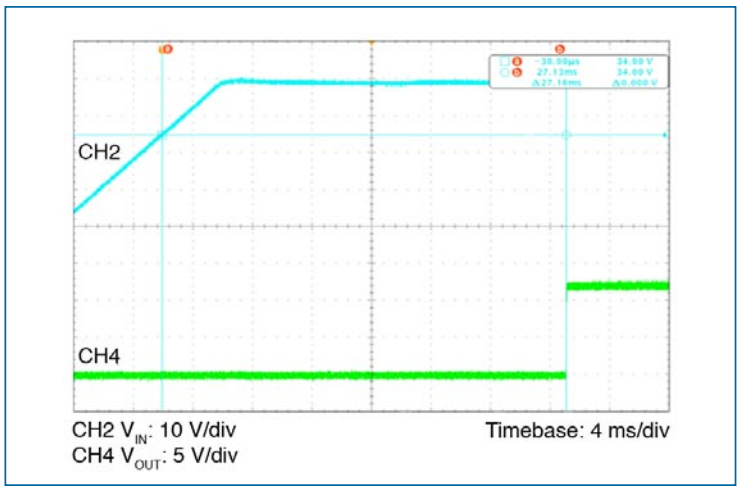


Figure 6 — Turn on delay time;
V_{IN} turn on delay at nominal line, 15% load

SPECIFICATIONS (CONT.)

WAVEFORMS (CONT.)

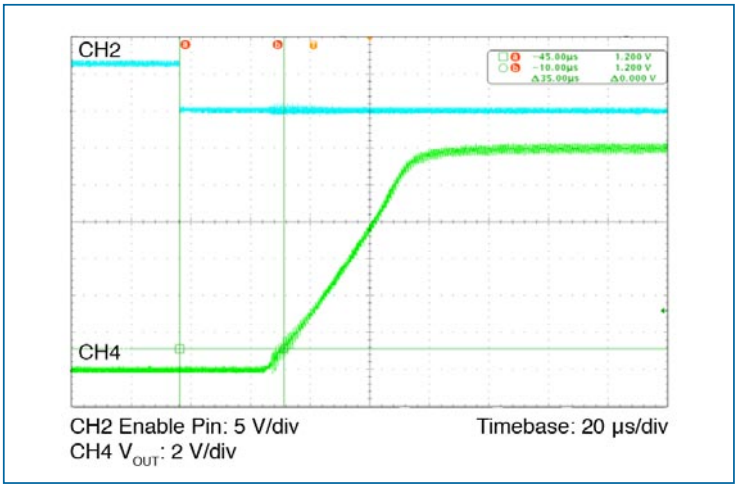


Figure 7 — Turn on delay time;
Enable turn on delay at nominal line, 15% load

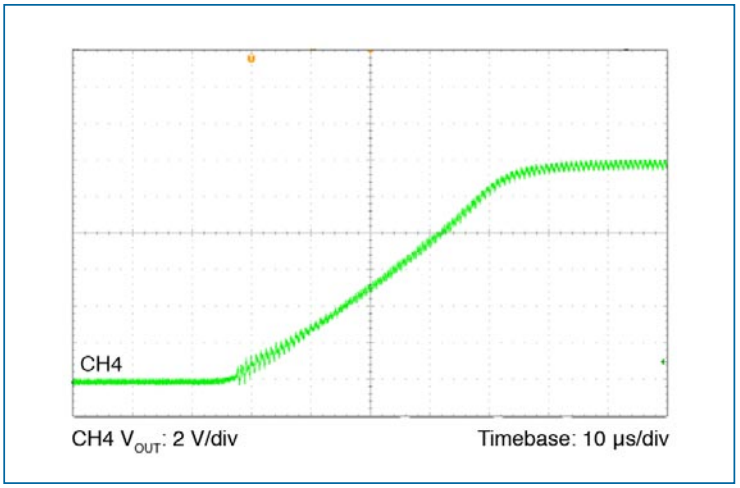


Figure 8 — Output voltage rise time at nominal line, 10% load

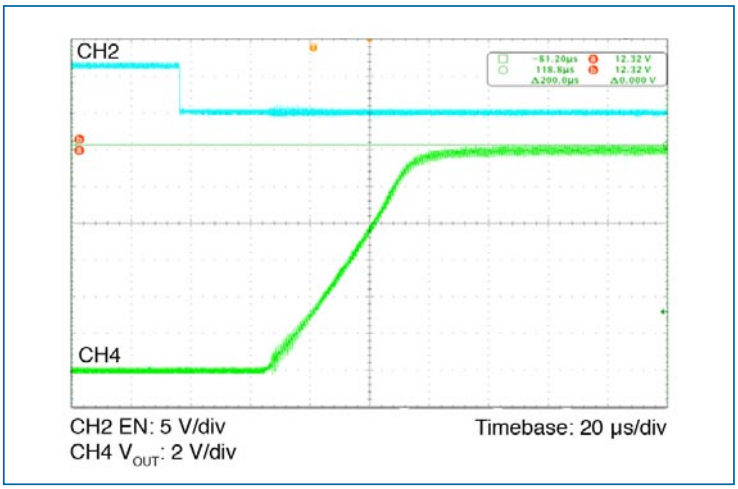


Figure 9 — Overshoot at turn on at nominal line, 15% load

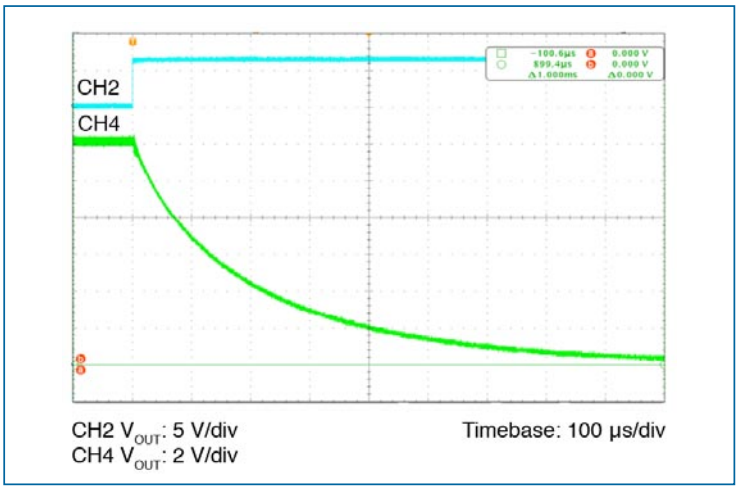


Figure 10 — Undershoot at turn off at nominal line, 10% load

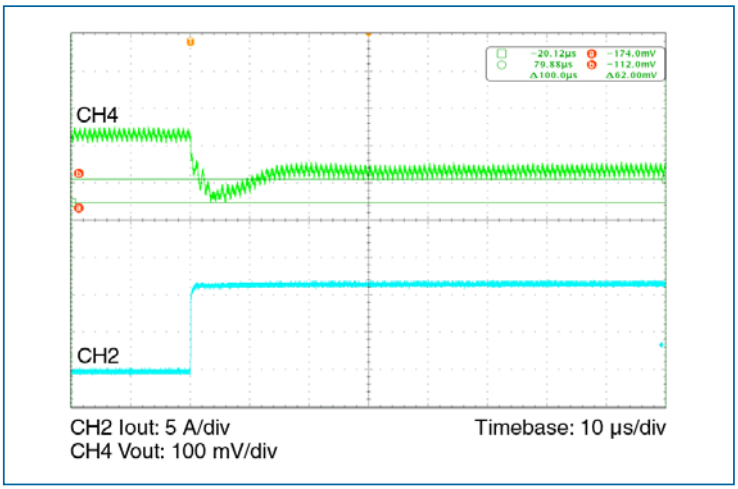


Figure 11 — Load transient response; nominal line
Load step 75–100%

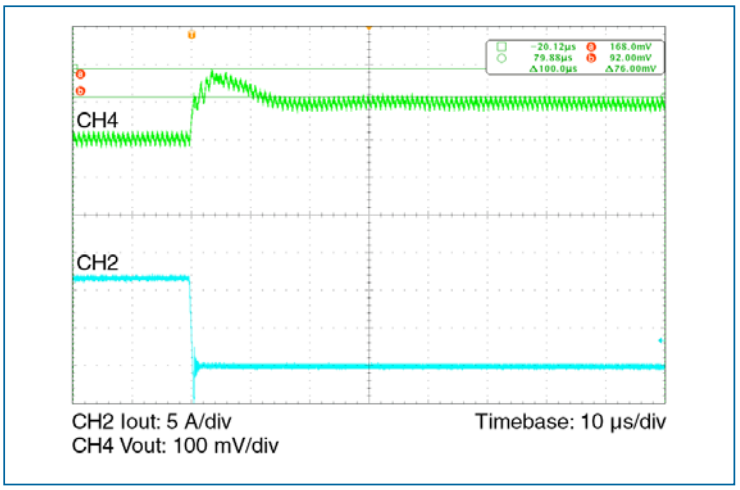


Figure 12 — Load transient response; Full load to 75%; nominal line

SPECIFICATIONS (CONT.)

WAVEFORMS (CONT.)

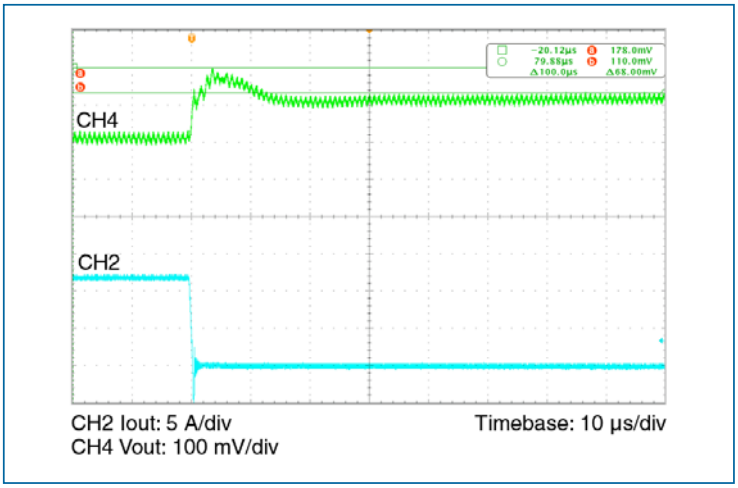


Figure 13 — Load transient response; nominal line Load step 0–25%

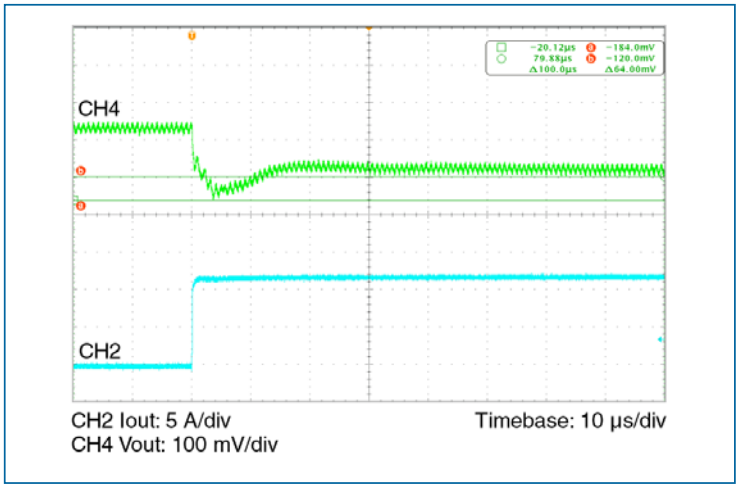


Figure 14 — Load transient response; 25–0%; nominal line

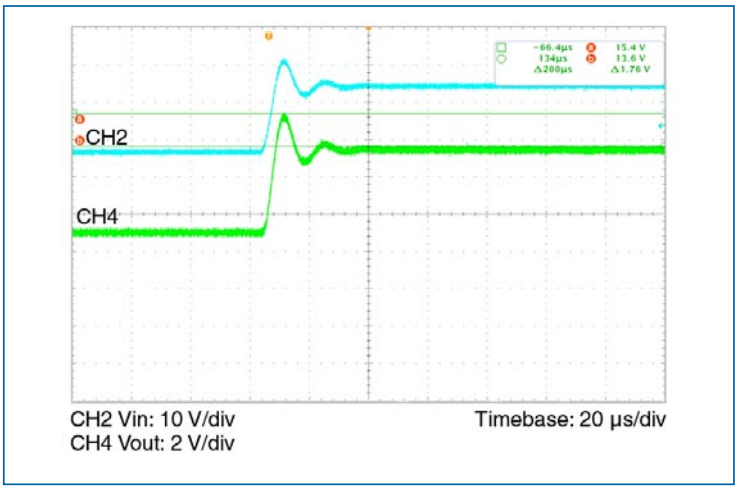


Figure 15 — Input transient response; Vin step low line to high line at full load

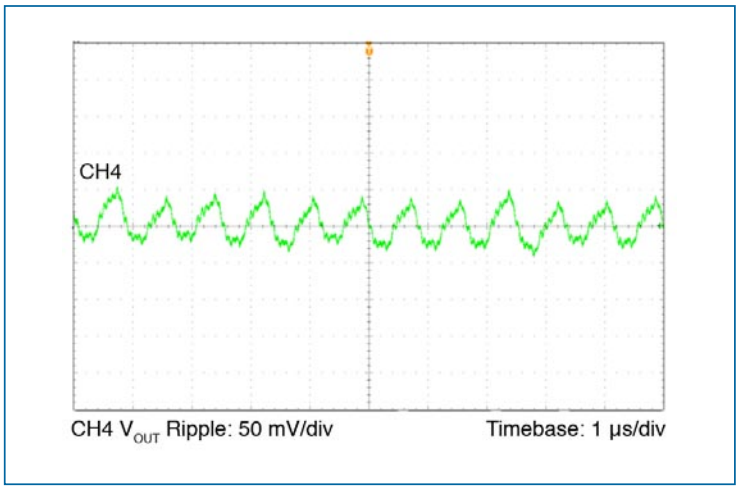


Figure 16 — Output ripple; Nominal line, full load

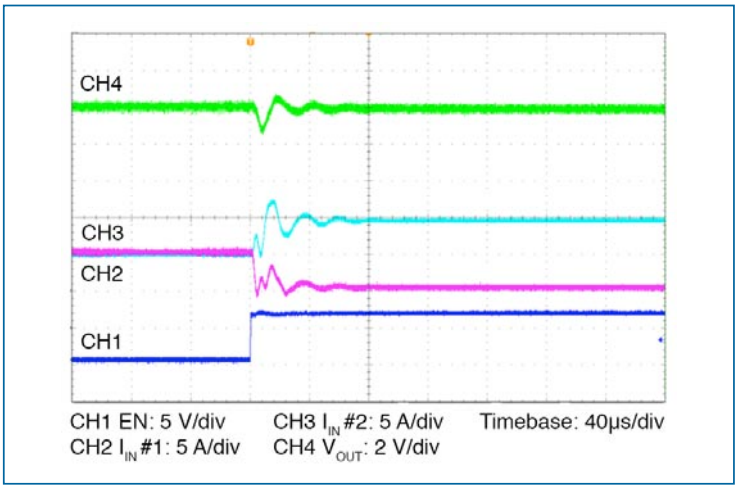


Figure 17 — Two modules parallel array test. V_{OUT} and I_{IN} change when one module is disabled. Nominal V_{IN}, I_{OUT} = 40 A

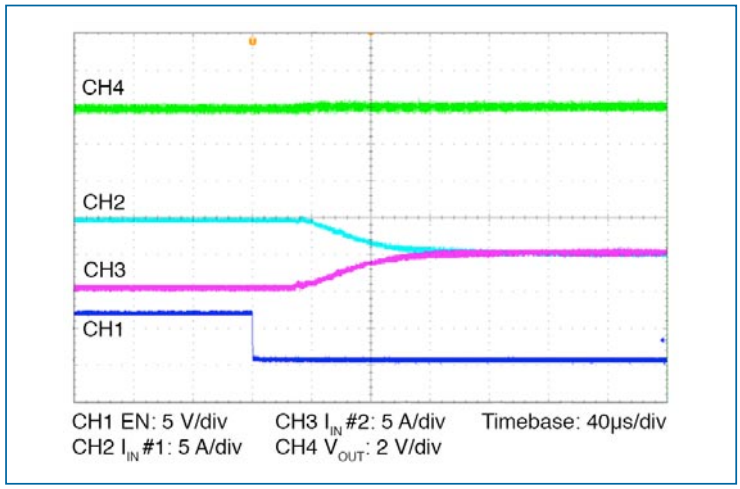


Figure 18 — Two modules parallel array test. V_{OUT} and I_{IN} change when one module is enabled. Nominal V_{IN}, I_{OUT} = 40 A

SPECIFICATIONS (CONT.)

WAVEFORMS (CONT.)

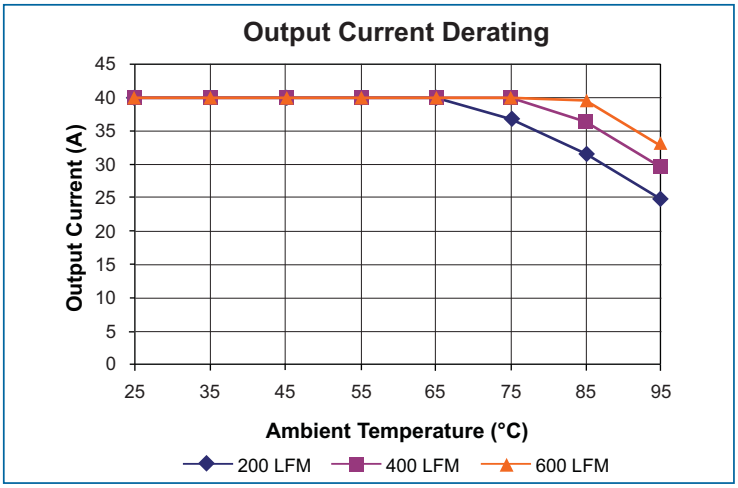


Figure 19 — Maximum output current derating vs ambient air temperature. Transverse airflow, Board and junction temperatures within IPC-9592 derating guidelines

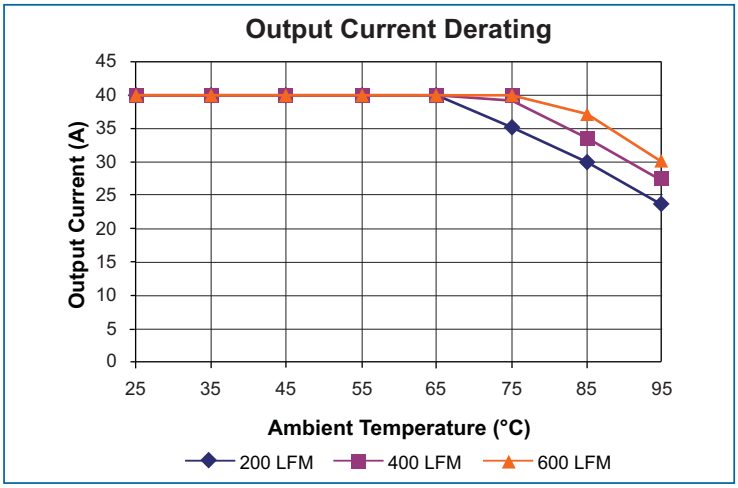


Figure 20 — Maximum output current derating vs ambient air temperature. Longitudinal airflow, Board and junction temperatures within IPC-9592 derating guidelines

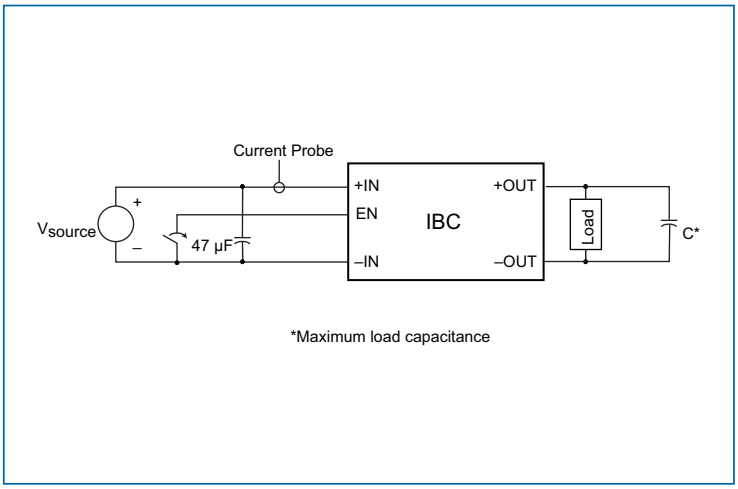


Figure 21 — Inrush current overshoot

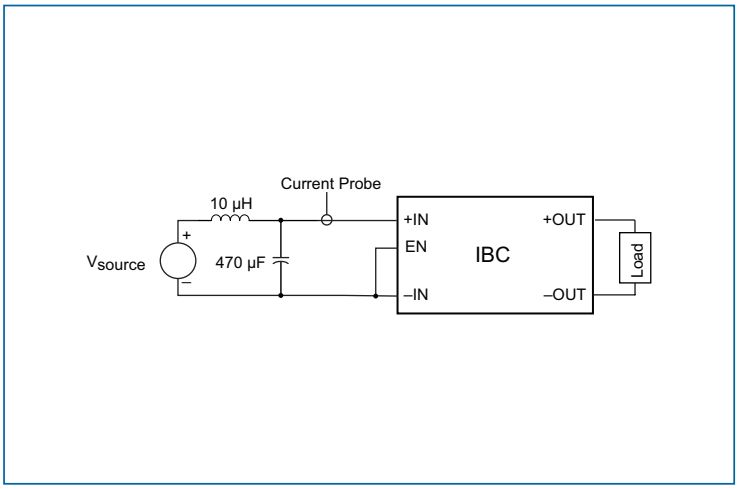


Figure 22 — Input reflected ripple current

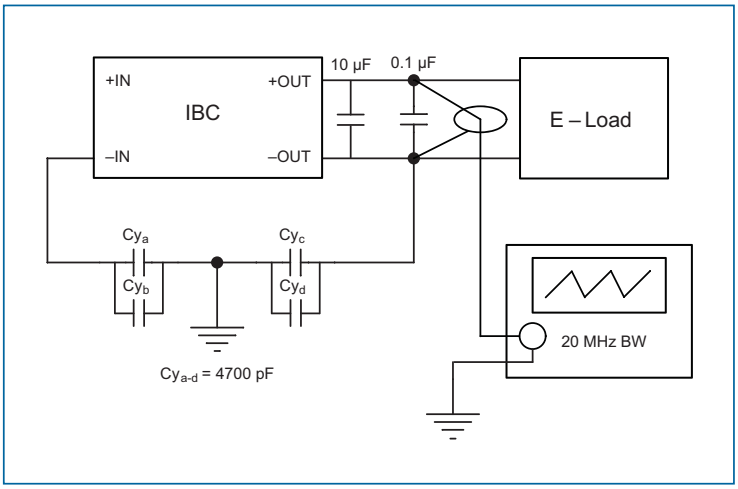


Figure 23 — Test circuit; output voltage ripple

SPECIFICATIONS (CONT.)

THERMAL DATA

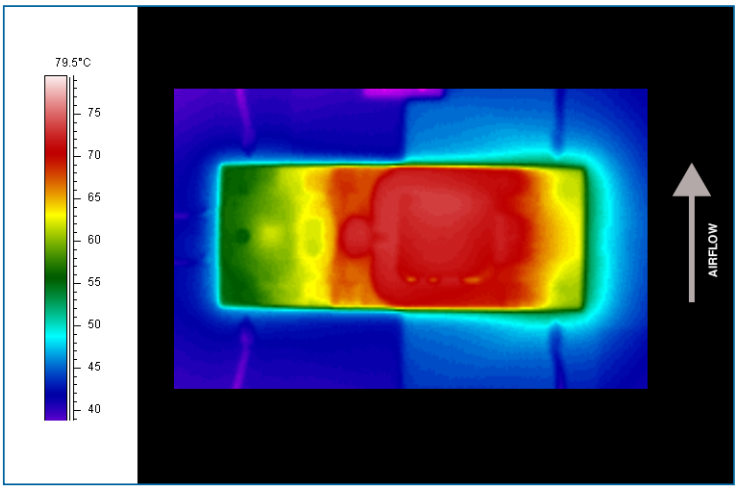


Figure 24 — Thermal plot, 200 LFM, 25°C, 48 Vin, 450 W output power

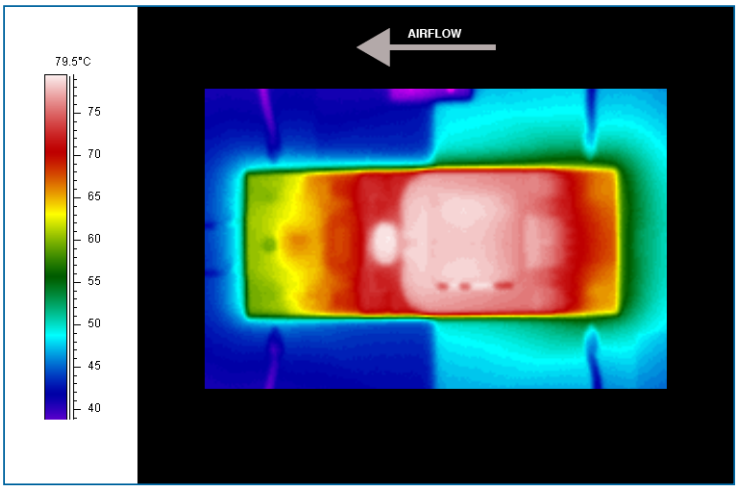


Figure 25 — Thermal plot, 200 LFM, 25°C, 48 Vin, 450 W output power

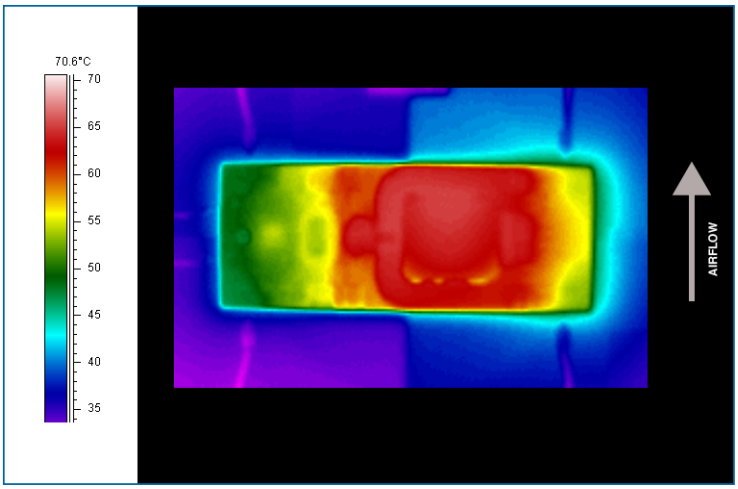


Figure 26 — Thermal plot, 400 LFM, 25°C, 48 Vin, 450 W output power

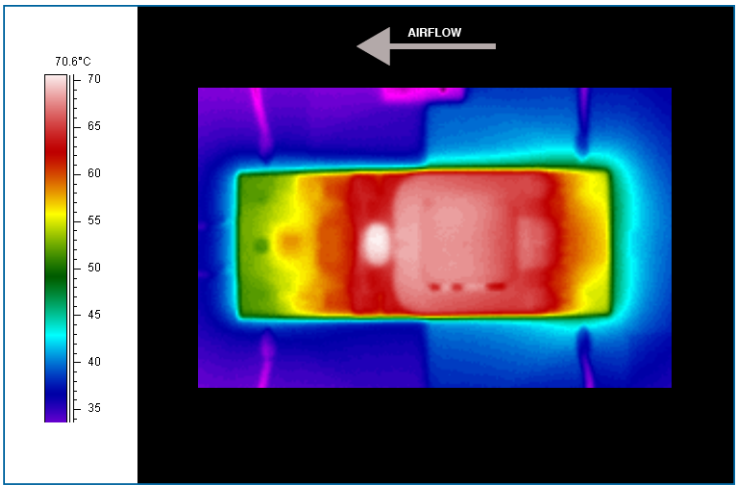


Figure 27 — Thermal plot, 400 LFM, 25°C, 48 Vin, 450 W output power

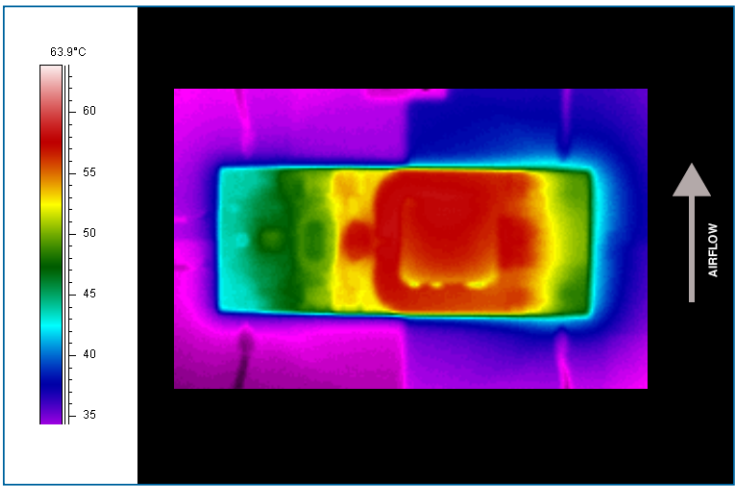


Figure 28 — Thermal plot, 600 LFM, 25°C, 48 Vin, 450 W output power

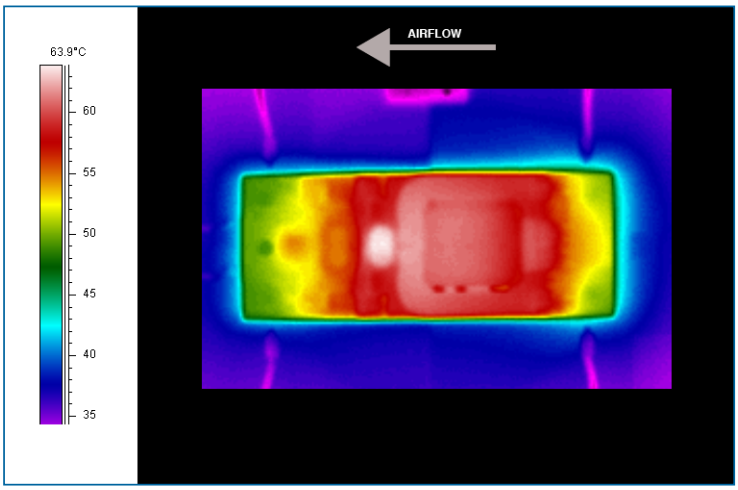


Figure 29 — Thermal plot, 600 LFM, 25°C, 48 Vin, 450 W output power

PIN / CONTROL FUNCTIONS

+In / -In – DC Voltage Input Pins

The IBC input voltage range should not be exceeded. An internal undervoltage/overvoltage lockout function prevents operation outside of the normal operating input range. The IBC turns on within an input voltage window bounded by the "Input under-voltage turn-on" and "Input over-voltage turn-off" levels, as specified. The IBC may be protected against accidental application of a reverse input voltage by the addition of a rectifier in series with the positive input, or a reverse rectifier in shunt with the positive input located on the load side of the input fuse.

The connection of the IBC to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100 nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200 nH, the RC damper may be 47 µF in series with 0.3 Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

EN - Enable/Disable

Negative Logic Option

If the EN port is left floating, the IBC output is disabled. Once this port is-pulled lower than 0.8 Vdc with respect to –In, the output is enabled. The EN port can be driven by a relay, opto-coupler, or open collector transistor. Refer to Figures 6 and 7 for the typical enable / disable characteristics. This port should not be toggled at a rate higher than 1 Hz. The EN port should also not be driven by or pulled up to an external voltage source.

Positive Logic Option

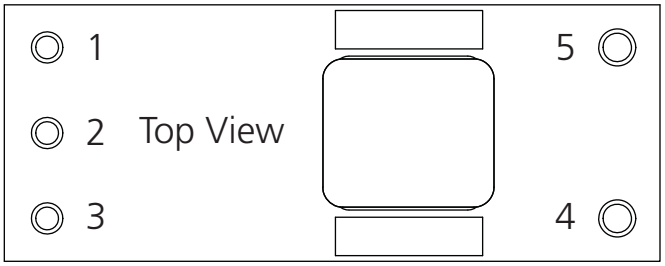
If the EN port is left floating, the IBC output is enabled. Once this port is pulled lower than 1.4 Vdc with respect to –In, the output is disabled. This action can be realized by employing a relay, opto-coupler, or open collector transistor. This port should not be toggled at a rate higher than 1 Hz.

The EN port should also not be driven by or pulled up to an external voltage source. The EN port can source up to 2 mA at 5 Vdc. The EN port should never be used to sink current.

If the IBC is disabled using the EN pin, the module will attempt to restart approximately every 250ms. Once the module has been disabled for at least 250ms, the turn on delay after the EN pin is enabled will be as shown in Figure 7.

+Out / -Out – DC Voltage Output Pins

Total load capacitance at the output of the IBC should not exceed the specified maximum. Owing to the wide bandwidth and low output impedance of the IBC, low frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the input of the IBC.



Pin	Function
1	Vin+
2	Enable
3	Vin-
4	Vout-
5	Vout+

Figure 30 — IBC Pin Designations

APPLICATIONS NOTE

Parallel Operation

The IBC will inherently current share when operated in an array. Arrays may be used for higher power or redundancy in an application. Current sharing accuracy is maximized when the source and load impedance presented to each IBC within an array are equal. The recommended method to achieve matched impedances is to dedicate common copper planes within the PCB to deliver and return the current to the array, rather than rely upon traces of varying lengths. In typical applications the current being delivered to the load is larger than that sourced from the input, allowing narrower traces to be utilized on the input side if necessary. The use of dedicated power planes is, however, preferable.

One or more IBCs in an array may be disabled without adversely affecting operation or reliability as long as the load does not exceed the rated power of the enabled IBCs.

The IBC power train and control architecture allow bi-directional power transfer, including reverse power processing from the IBC output to its input. The IBC's ability to process power in reverse improves the IBC transient response to an output load dump.

Thermal Considerations

The temperature distribution of the VI Brick can vary significantly with its input/output operating conditions, thermal management and environmental conditions. Although the PCB is UL rated to 130°C, it is recommended that PCB temperatures be maintained at or below 125°C. For maximum long term reliability, lower PCB temperatures are recommended for continuous operation, however, short periods of operation at 125°C will not negatively impact performance or reliability.

WARNING: Thermal and voltage hazards. The IBC can operate with surface temperatures and operating voltages that may be hazardous to personnel. Ensure that adequate protection is in place to avoid inadvertent contact.

Input Impedance Recommendations

To take full advantage of the IBC capabilities, the impedance presented to its input terminals must be low from DC to approximately 5 MHz. The source should exhibit low inductance and should have a critically damped response. If the interconnect inductance is excessive, the IBC input pins should be bypassed with an RC damper (e.g., 47 µF in series with 0.3 Ω) to retain low source impedance and proper operation. Given the wide bandwidth of the IBC, the source response is generally the limiting factor in the overall system response.

Anomalies in the response of the source will appear at the output of the IBC multiplied by its K factor. The DC resistance of the source should be kept as low as possible to minimize voltage deviations. This is especially important if the IBC is operated near low or high line as the overvoltage/undervoltage detection circuitry could be activated.

Input Fuse Recommendations

The IBC is not internally fused in order to provide flexibility in configuring power systems. However, input line fusing of VI Bricks must always be incorporated within the power system. A fast acting fuse should be placed in series with the +In port. See safety agency approvals.

Application Notes

For IBC and VI Brick application notes on soldering, thermal management, board layout, and system design visit vicorpower.com.

IBC BLOCK DIAGRAM

The Sine Amplitude Converter™ (SAC™) uses a high frequency resonant tank to transfer energy from input to output. The resonant tank is formed by Cr and leakage inductance from the main transformer, Lr, as shown in the block diagram. The controller regulates switching frequency of the FET drivers, monitors current sensing, and provides undervoltage and overvoltage protection.

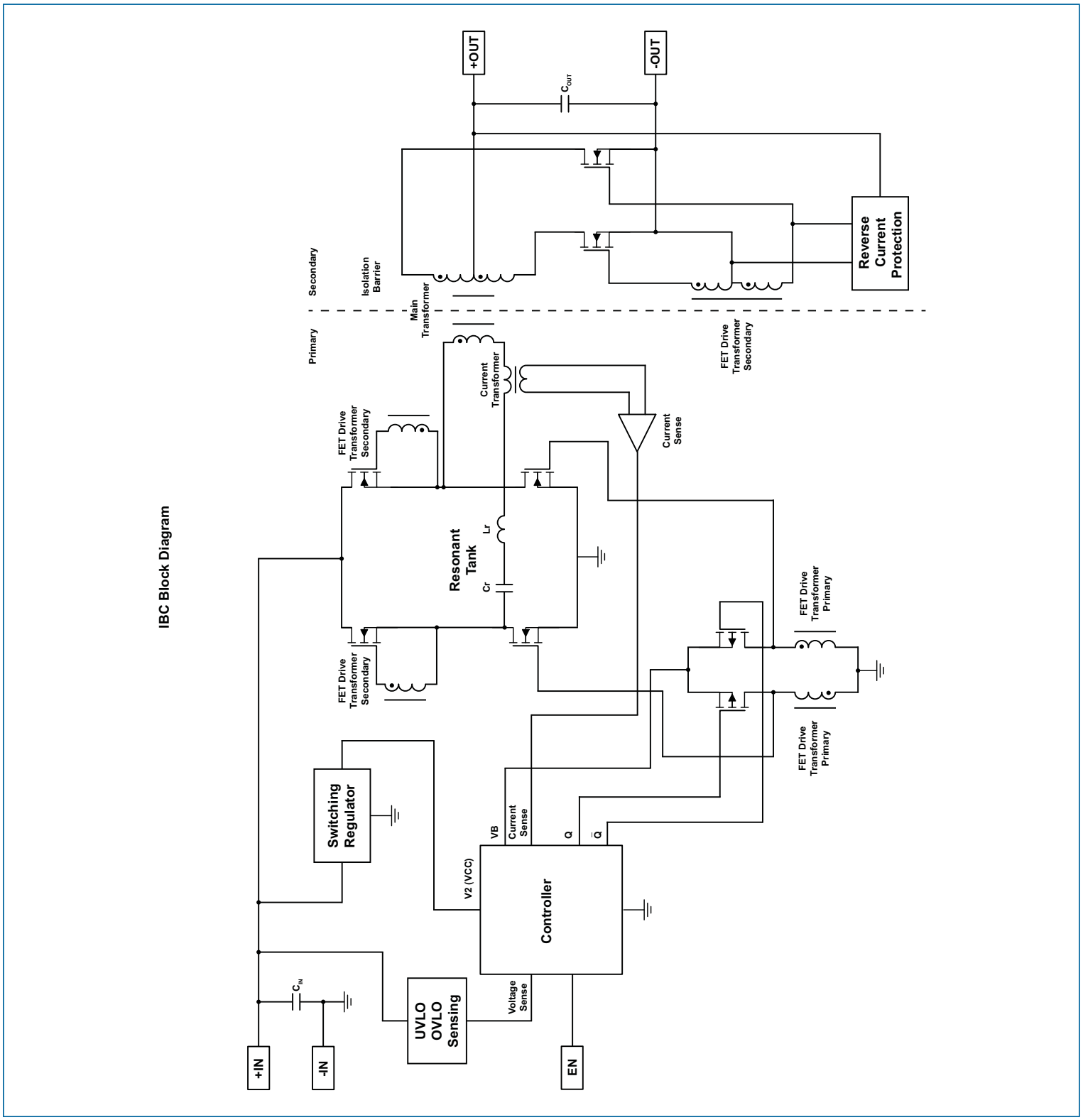
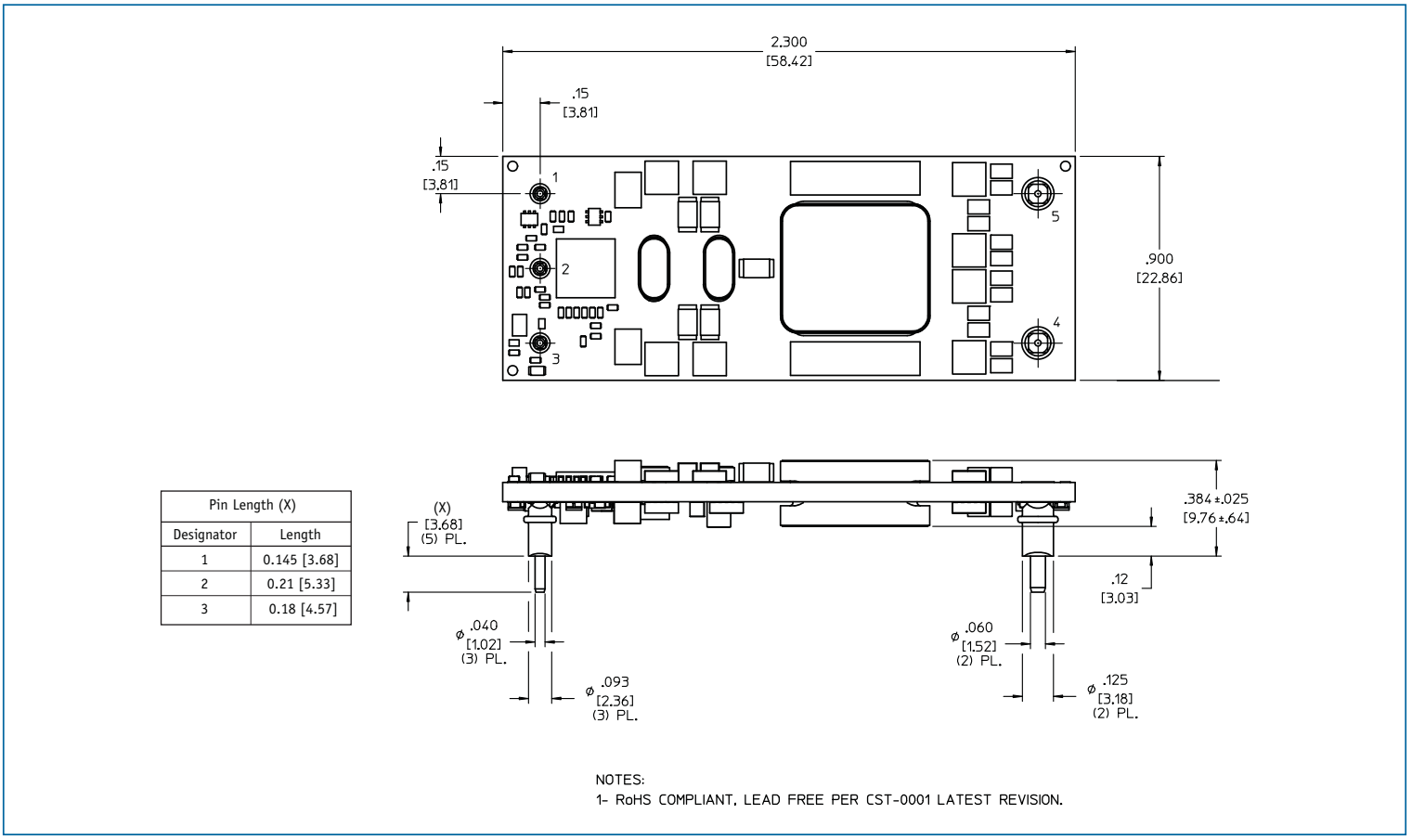


Figure 31 — IBC Block diagram

MECHANICAL DRAWINGS



Pin Length (X)	
Designator	Length
1	0.145 [3.68]
2	0.21 [5.33]
3	0.18 [4.57]

Figure 32 — IBC outline drawing

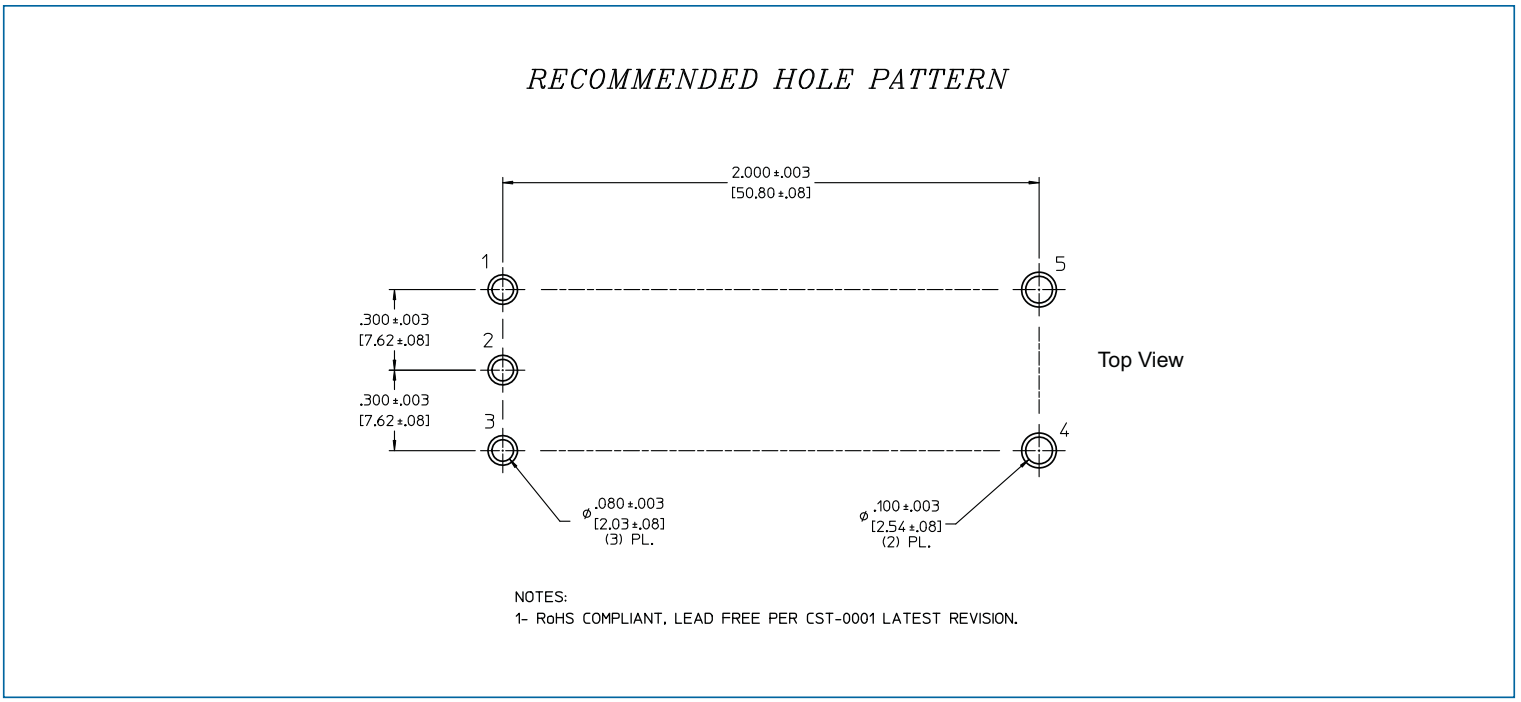


Figure 33 — IBC PCB recommended hole pattern

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