Innovasic®
Semiconductor
Extended Life Semiconductor Solutions

IA8044/IA8344
SDLC Communications Controller
Data Sheet

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1. Introduction

The Innovasic Semiconductor IA8044 and IA8344 are "plug-and-play" drop-in replacements and are form, fit, and function compatible parts to the Intel® 8044 and 8344 (see Chapter 4, Innovasic/Intel Part Number Cross-Reference Tables). These devices are produced using Innovasic's Managed IC Lifetime Extension System (MILES™). This cloning technology, which produces replacement ICs beyond simple emulations, ensures complete compatibility with the original device, including any "undocumented features." Additionally, the MILES™ process captures the clone design in such a way that production of the clone can continue even as silicon technology advances. The IA8044 and IA8344 replace the obsolete Intel 8044 and 8344, allowing users to retain existing board designs, software compilers/assemblers, and emulation tools—thus avoiding expensive redesign efforts.

The IA8044 and IA8344 are Fast Single-Chip 8-Bit Microcontrollers with an integrated SDLC/HDLC serial interface controller. They are fully functional 8-Bit Embedded Controllers that execute all ASM51 instructions and have the same instruction set as the Intel 80C51. The IA8044 and IA8344 can access the instructions from two types of program memory, serve software and hardware interrupts, and provide interface for serial communications and a timer system. The IA8044 and IA8344 are fully compatible with the Intel® 8X44 series.

This data sheet documents all necessary engineering information about the IA8044 and IA8344 including functional and I/O descriptions, electrical characteristics, and applicable timing.

1.1 Features

- Form, fit, and function compatible with the Intel 8044 and 8344
- Packaging options available in both leaded and RoHS versions:
  - 40-Pin Plastic Dual In-Line Package (PDIP) (see IA8044 40-Lead PDIP Package Diagram)
  - 44-Pin Plastic Leaded Chip Carrier (PLCC) (see IA8344 44-Pin PLCC Package Diagram)

- 8-bit control unit (see Functional Block Diagram)
- 8-bit arithmetic-logic unit with 16-bit multiplication and division
- 12-MHz clock
- Four 8-bit input/output ports
- Two 16-bit timer/counters
- Serial interface unit with SDLC/HDLC compatibility
- 2.4-Mbps maximum serial data rate
- Two-level priority interrupt system
- 5 interrupt sources
- Internal clock prescaler and phase generator
- 192 bytes of read/write data memory space
- 64-Kbyte external program memory space

- 64-Kbyte external data memory space
- 4-Kbyte internal ROM (IA8044 only)

1.2 Variants

- IA8044
  - 4-Kbyte internal ROM with R0117 version 2.3 firmware
  - 192-byte internal RAM
  - 64-Kbyte external program and data space

- IA8344
  - 192-byte internal RAM
  - 64-Kbyte external program and data space

2. Packaging, Pin Descriptions, and Physical Dimensions

The Innovasic Semiconductor IA8044 and IA8344 serial controllers are available in the following packages:

- 40-Pin Plastic Dual In-Line Package (PDIP), equivalent to original PDIP package (see Physical Package Dimensions)

- 44-Lead Plastic Leaded Chip Carrier (PLCC), equivalent to original PLCC package (see Physical Package Dimensions)

2.1 PDIP Package

The pinout for the IA8044 and IA8344 40 PDIP package is as shown in Figure 1. Although Figure 1 shows "IA8X44," each device has a complete part number marked on its face (see Chapter 8, Innovasic/Intel Part Number Cross-Reference Tables). The corresponding pinout is provided in Table 1.

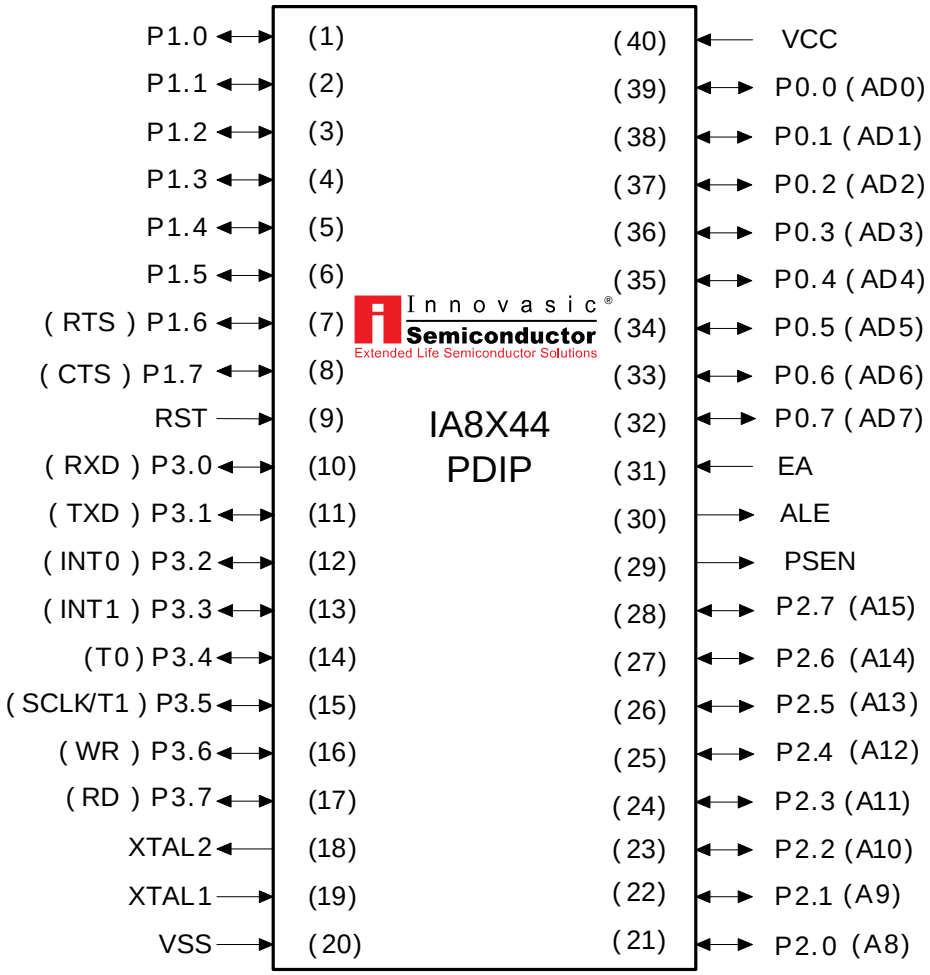


Figure 1. IA8044 and IA8344 40-Lead PDIP Package Diagram

Table 1. IA8044 and IA8344 40-Lead PDIP Pin Listing

Pin	Name
1	P1.0
2	P1.1
3	P1.2
4	P1.3
5	P1.4
6	P1.5
7	P1.6 (RTS)
8	P1.7 (CTS)
9	RST
10	P3.0 (RXD)

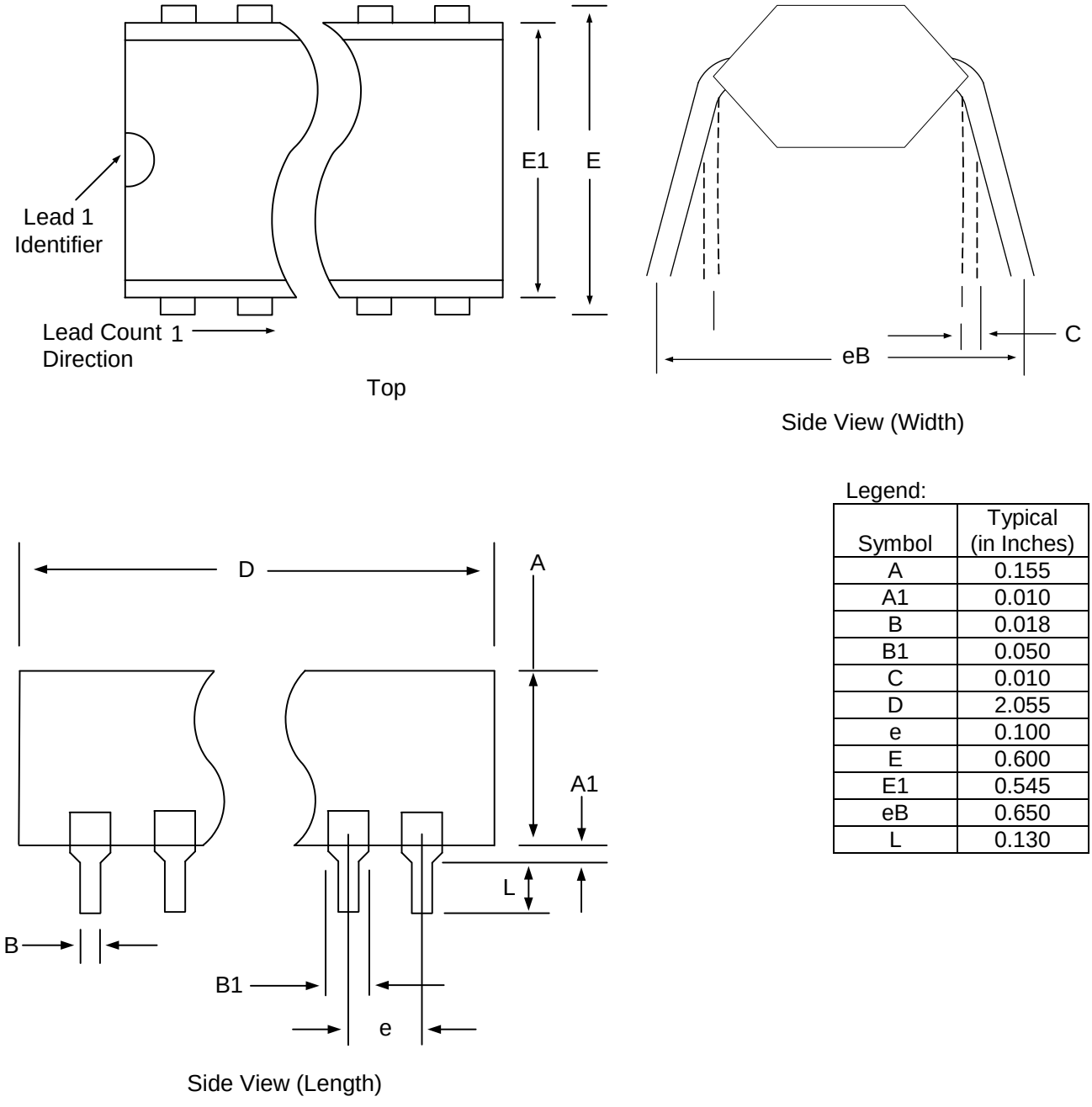
Pin	Name
11	P3.1 (TXD)
12	P3.2 (INT0)
13	P3.3 (INT1)
14	P3.4 (T0)
15	P3.5 (SCLK/T1)
16	P3.6 (WR)
17	P3.7 (RD)
18	XTAL2
19	XTAL1
20	VSS

Pin	Name
21	P2.0 (A8)
22	P2.1 (A9)
23	P2.2 (A10)
24	P2.3 (A11)
25	P2.4 (A12)
26	P2.5 (A13)
27	P2.6 (A14)
28	P2.7 (A15)
29	PSEN
30	ALE

Pin	Name
31	EA
32	P0.7 (AD7)
33	P0.6 (AD6)
34	P0.5 (AD5)
35	P0.4 (AD4)
36	P0.3 (AD3)
37	P0.2 (AD2)
38	P0.1 (AD1)
39	P0.0 (AD0)
40	VCC

2.2 PDIP Physical Dimensions

The physical dimensions for the 40 PDIP are as shown in Figure 2.



Legend:

Symbol	Typical (in Inches)
A	0.155
A1	0.010
B	0.018
B1	0.050
C	0.010
D	2.055
e	0.100
E	0.600
E1	0.545
eB	0.650
L	0.130

Figure 2. PDIP Physical Package Dimensions

2.3 PLCC Package

The pinout for the IA8044 and IA8344 44 PLCC package is as shown in Figure 3. Although Figure 3 shows "IA8X44," each device has a complete part number marked on its face (see Chapter 8, Innovasic/Intel Part Number Cross-Reference Tables). The corresponding pinout is provided in Table 2.

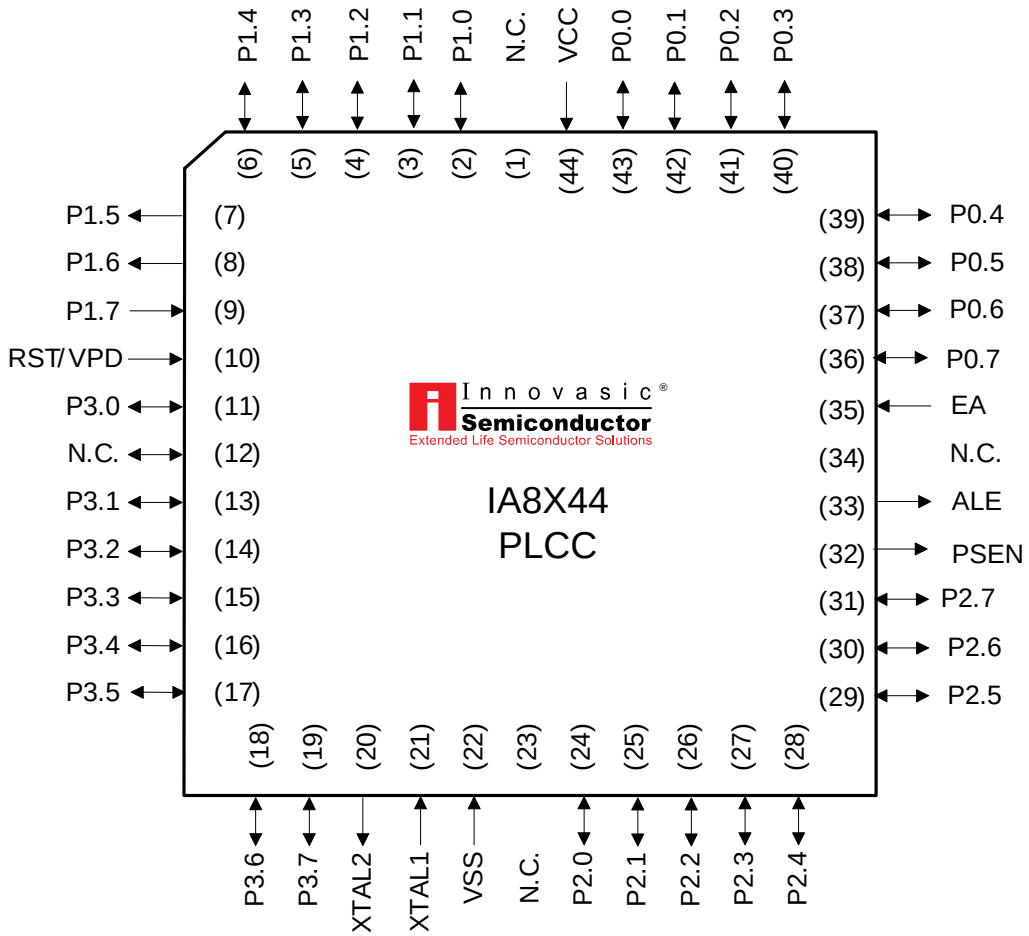


Figure 3. IA8044 and IA8344 44-Pin PLCC Package Diagram

Table 2. IA8044 and IA8344 44-Pin PLCC Pin Listing

Pin	Name
1	N.C.
2	P1.0
3	P1.1
4	P1.2
5	P1.3
6	P1.4
7	P1.5
8	P1.6
9	P1.7
10	RST/VPD
11	P3.0

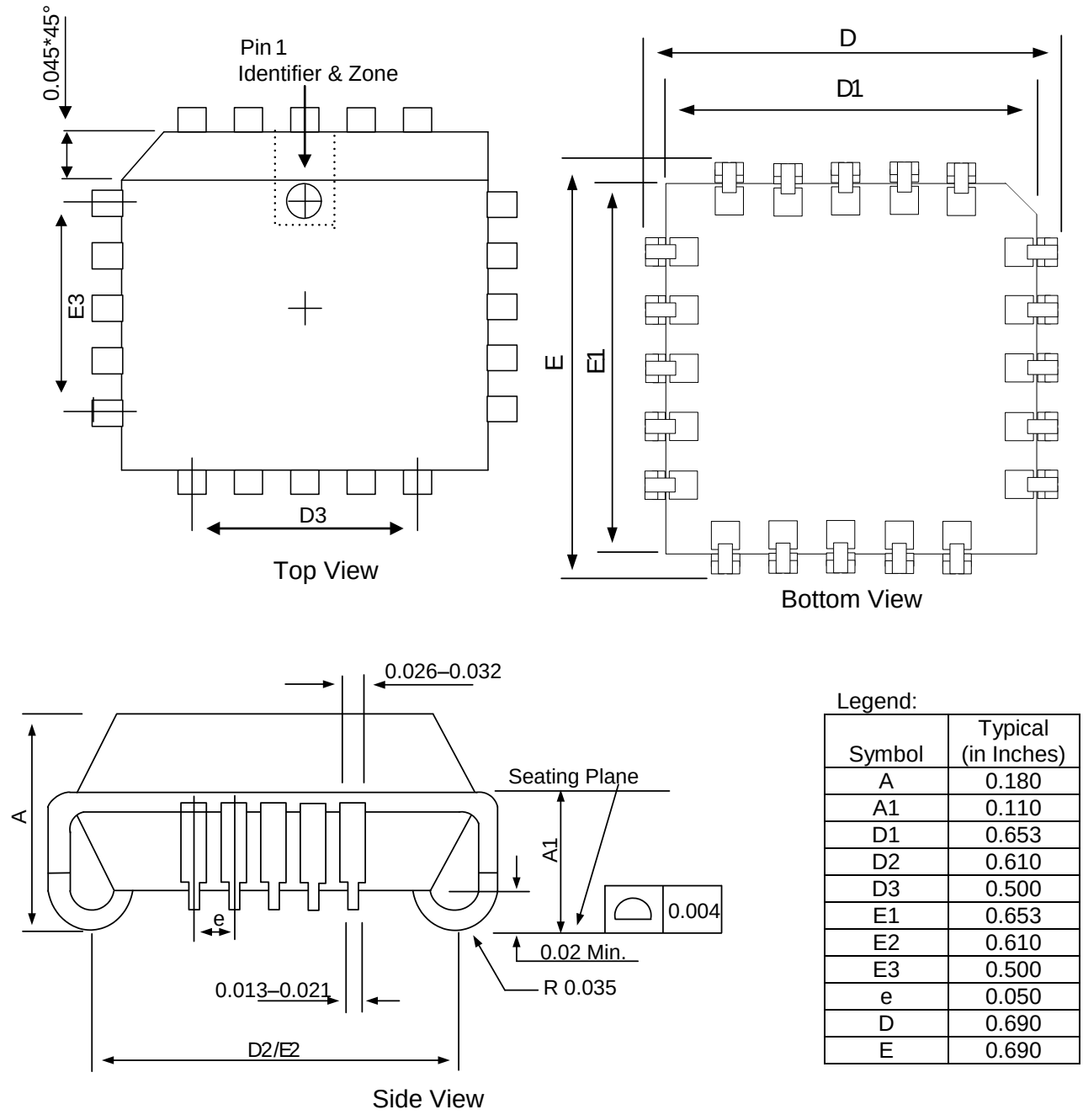
Pin	Name
12	N.C.
13	P3.1
14	P3.2
15	P3.3
16	P3.4
17	P3.5
18	P3.6
19	P3.7
20	XTAL2
21	XTAL1
22	VSS

Pin	Name
23	N.C.
24	P2.0
25	P2.1
26	P2.2
27	P2.3
28	P2.4
29	P2.5
30	P2.6
31	P2.7
32	PSEN
33	ALE

Pin	Name
34	N.C.
35	EA
36	P0.7
37	P0.6
38	P0.5
39	P0.4
40	P0.3
41	P0.2
42	P0.1
43	P0.0
44	VCC

2.4 PLCC Physical Dimensions

The physical dimensions for the 44 PLCC are as shown in Figure 4.



Legend:

Symbol	Typical (in Inches)
A	0.180
A1	0.110
D1	0.653
D2	0.610
D3	0.500
E1	0.653
E2	0.610
E3	0.500
e	0.050
D	0.690
E	0.690

Figure 4. PLCC Physical Package Dimensions

3. Maximum Ratings and DC Characteristics

The IA8044/IA8344 absolute maximum ratings and DC characteristics are provided in Tables 3 and 4, respectively.

Table 3. IA8044 and IA8344 Absolute Maximum Ratings

Parameter	Rating
Ambient temperature under bias	−40°C to +85°C
Storage temperature	−40°C to +150°C
Power supply (V_{DD})	−0.3 to +6VDC
Voltage on any pin to VSS	−0.3 to (V_{DD} +0.3)[a]
Power dissipation	2W

[a]This device does not contain EPROM or its related programming circuitry. Therefore, this limit must be adhered to especially for input pin EA, which is used as the programming voltage pin in the Intel device. Exceeding the listed maximum voltage will cause damage to the device.

Table 4. IA8044 and IA8344 DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VIL	Input Low Voltage	–	–	0.8	V
VIH	Input High Voltage	2.0	–	–	V
VOL	Output Low Voltage (IOL= 4mA)	–	–	0.4	V
VOH	Output High Voltage (IOH= 4mA)	3.5	–	–	V
RPU	Pull-Up Resistance (Ports 1, 2, 3)	–	50	–	KW
RPD	Pull-Down Resistance (RST)	–	50	–	KW
IIL	Input Low Current (Ports 1, 2, 3)	−200	–	1	µA
IIL1	Input Low Current (PO, EA)	−1	–	1	µA
IIH	Input High Current (RST)	−1	–	200	µA
IIH1	Input High Current (PO, EA)	−1	–	1	µA
IOZ	Tri-state Leakage Current (Port 0)	−10	–	10	µA
ICC	Power Supply Current (@ 12 MHz)	–	–	50	mA
CIO	Pin Capacitance	–	4	–	pF

4. Functional Description

4.1 Functional Block Diagram

A functional block diagram of the IA8044 and IA8344 is shown in Figure 5. Descriptions of the functional modules are provided in the following subsections.

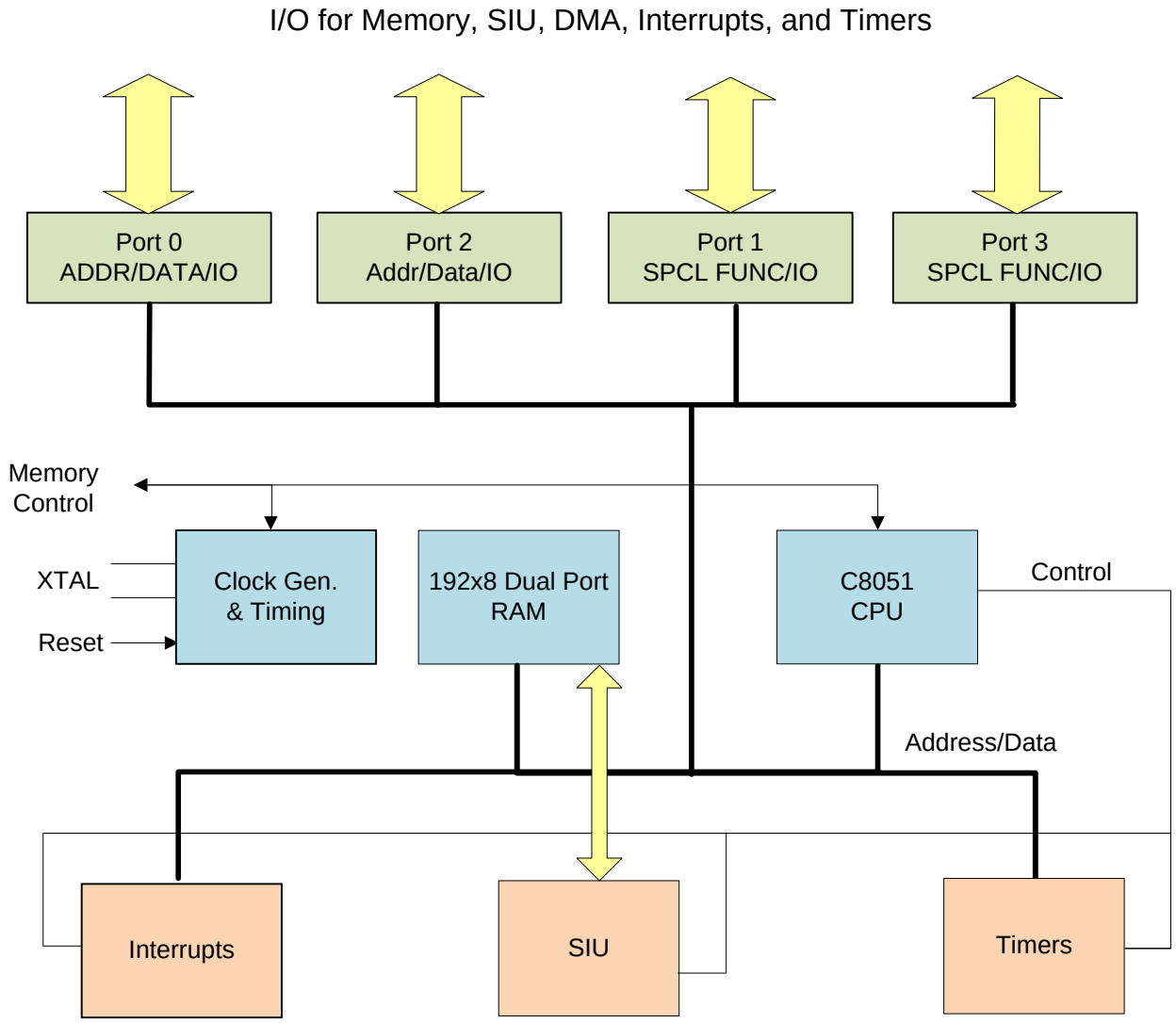


Figure 5. Functional Block Diagram

4.2 Input/Output Characteristics

Table 5 describes the I/O characteristics for each signal on the IC. The signal names correspond to those on the pinout diagrams provided. The table provides the I/O description of the IA8044 and the IA8344.

Table 5. Input/Output Characteristics of IC Signals

Name	Type	Description
RST	I	Reset—This pin will cause the chip to reset when held high for two machine cycles while the oscillator is running.
ALE	O	Address Latch Enable—Used to latch the address on the falling edge for external memory accesses.
PSEN	O	Program Store Enable—When low, acts as an output enable for external program memory.
EA	I	External Access—When held low, EA will cause the IA8044/IA8344 to fetch instructions from external memory.
P0.7–P0.0	I/O	Port 0—8-bit I/O port and low order multiplexed address/data byte for external accesses.
P1.7–P1.0	I/O	Port 1—8-bit I/O port. Two bits have alternate functions, P1.6 (RTS) and P1.7 (CTS).
P2.7–P2.0	I/O	Port 2—8-bit I/O port. It also functions as the high order address byte during external accesses.
P3.7–P3.0	I/O	Port 3—8-bit I/O port. Port 3 bits also have alternate functions as described below. P3.0 (RXD)—Receives data input for SIU or direction control for P3.1 dependent upon data link configuration. P3.1 (TXD)—Transmits data output for SIU or data input/output dependent upon data link configuration. Also enables diagnostic mode when cleared. P3.2 (INT0)—Interrupt 0 input or gate control input for Counter 0. P3.3 (INT1)—Interrupt 1 input or gate control input for Counter 1. P3.4 (T0)—Input to Counter 0. P3.5 (SCLK/T1)—SCLK input to SIU or input to Counter 1. P3.6 (WR)—External memory write signal. P3.7 (RD)—External memory read signal.
XTAL1	I	Crystal Input 1—Connects to VSS when external clock is used on XTAL2. May be connected to a crystal (with XTAL2) or may be driven directly with a clock source (XTAL2 not connected).
XTAL2	O	Crystal Input 2—May be connected to a crystal (with XTAL1) or may be driven directly with an inverted clock source (XTAL1 tied to ground).
VSS	P	Ground.
VCC	P	+5V power.

4.3 Memory Organization

4.3.1 Program Memory

Program Memory includes interrupt and Reset vectors. The interrupt vectors are spaced at 8-byte intervals, starting from 0003H for External Interrupt 0.

Table 6. Reset Vectors

Location	Service
0003H	External Interrupt 0
000BH	Timer 0 overflow
0013H	External Interrupt 1
001BH	Timer 1 overflow
0023H	SIU Interrupt

These locations may be used for program code, if the corresponding interrupts are not used (disabled). The program memory space is 64K, from 0000H to FFFFH. The lowest 4K of program code (0000H to 0FFFH) can be fetched from external or internal program memory. This selection is made by strapping pin "EA" (External Address) to GND or VCC. If during reset "EA" is held low, all the program code is fetched from external memory. If during reset "EA" is held high, the lowest 4K of program code (0000H to 0FFFH) is fetched from internal memory (ROM). Program memory addresses above 4K (0FFFH) will cause the program code to be fetched from external memory regardless of the setting of "EA."

4.3.2 External Data Memory

The IA8044/IA8344 Microcontroller core incorporates the Harvard architecture, with separate code and data spaces. The code from external memory is fetched by "psen" strobe, while data is read from RAM by Bit [7] of P3 (read strobe) and written to RAM by Bit [6] of P3 (write strobe). The External Data Memory space is active only by addressing through use of the MOVX instruction and the 16-bit Data Pointer Register (DPTR). A smaller subset of external data memory (8-bit addressing) may be accessed by using the MOVX instruction with register indexed addressing.

4.3.3 Internal Data Memory

As presented in Figure 6, the Internal Data Memory address is always one byte wide. The memory space is 192 bytes large (00H to BFH), and can be accessed by either direct or indirect addressing. The special function registers (SFRs) occupy the upper 128 bytes. This SFR area is available only by direct addressing. Internal memory that overlaps the SFR address space is only accessible by indirect addressing.

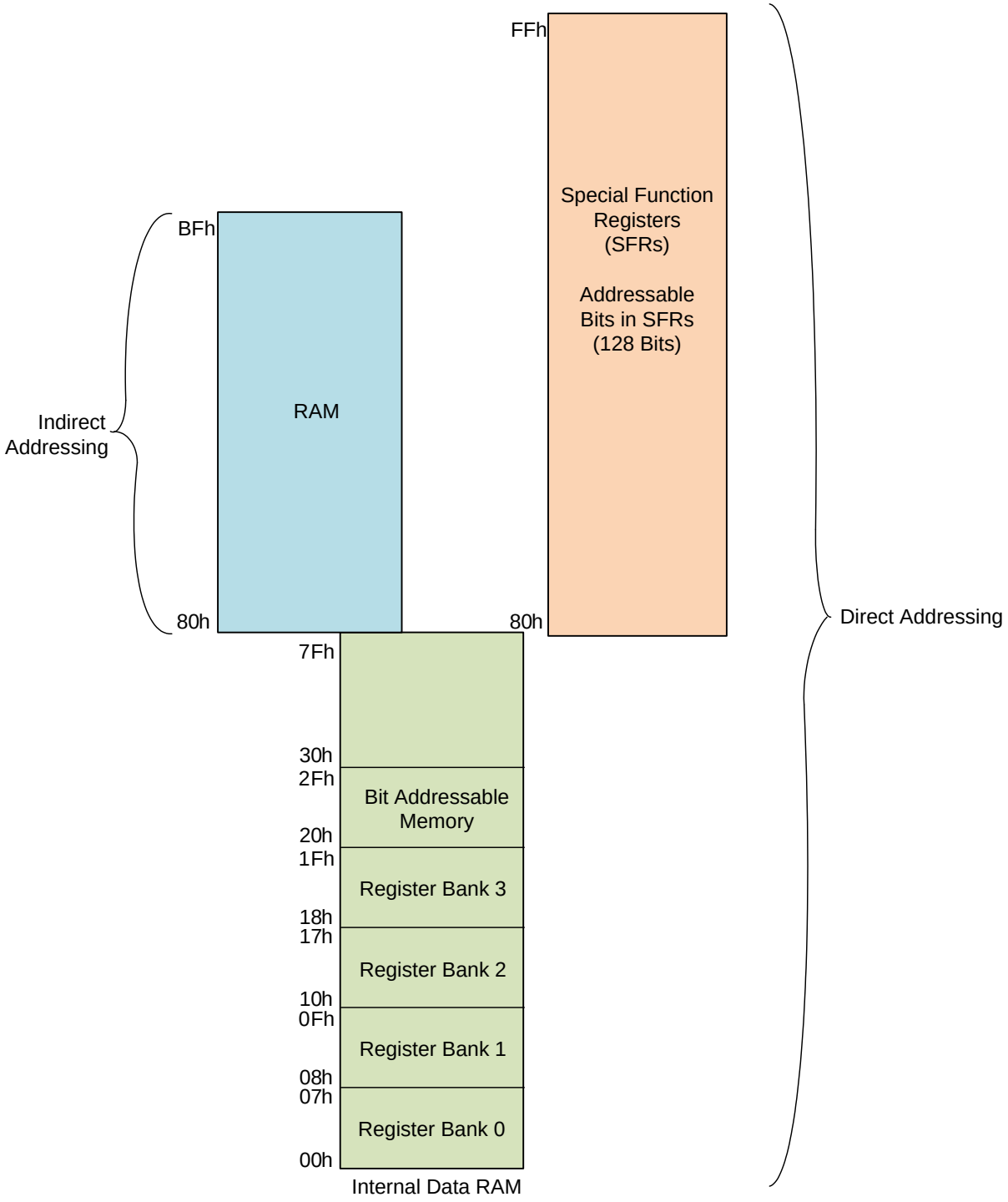


Figure 6. Internal Data Memory Addresses 00h to FFh

4.3.4 Bit Addressable Memory

Both the internal RAM and the SFRs have locations that are bit addressable in addition to the byte addressable locations (see Tables 7 and 8).

Table 7. SFR Bit Addressable Locations

Byte Address	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]	Register
F0h	F7h	F6h	F5h	F4h	F3h	F2h	F1h	F0h	B
E0h	E7h	E6h	E5h	E4h	E3h	E2h	E1h	E0h	ACC
D8h	DFh	DEh	DDh	DCh	DBh	DAh	D9h	D8h	NSNR
D0h	D7h	D6h	D5h	D4h	D3h	D2h	D1h	D0h	PSW
C8h	CFh	CEh	CDh	CCh	CBh	CAh	C9h	C8h	STS
B8h	–	–	–	BCh	BBh	BAh	B9h	B8h	IP
B0h	B7h	B6h	B5h	B4h	B3h	B2h	B1h	B0h	P3
A8h	AFh	–	–	ACh	ABh	AAh	A9h	A8h	IE
A0h	A7h	A6h	A5h	A4h	A3h	A2h	A1h	A0h	P2
90h	97h	96h	95h	94h	93h	92h	91h	90h	P1
88h	8Fh	8Eh	8Dh	8Ch	8Bh	8Ah	89h	88h	TCON
80h	87h	86h	85h	84h	83h	82h	81h	80h	P0

Table 8. Internal RAM Bit Addressable Locations

Byte Address	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
30h-BFh	Upper Internal RAM Locations							
2Fh	7Fh	7Eh	7Dh	7Ch	7Bh	7Ah	79h	78h
2Eh	77h	76h	75h	74h	73h	72h	71h	70h
2Dh	6Fh	6Eh	6Dh	6Ch	6Bh	6Ah	69h	68h
2Ch	67h	66h	65h	64h	63h	62h	61h	60h
2Bh	5Fh	5Eh	5Dh	5Ch	5Bh	5Ah	59h	58h
2Ah	57h	56h	55h	54h	53h	52h	51h	50h
29h	4Fh	4Eh	4Dh	4Ch	4Bh	4Ah	49h	48h
28h	47h	46h	45h	44h	43h	42h	41h	40h
27h	3Fh	3Eh	3Dh	3Ch	3Bh	3Ah	39h	38h
26h	37h	36h	35h	34h	33h	32h	31h	30h
25h	2Fh	2Eh	2Dh	2Ch	2Bh	2Ah	29h	28h
24h	27h	26h	25h	24h	23h	22h	21h	20h
23h	1Fh	1Eh	1Dh	1Ch	1Bh	1Ah	19h	18h
22h	17h	16h	15h	14h	13h	12h	11h	10h
21h	0Fh	0Eh	0Dh	0Ch	0Bh	0Ah	09h	08h
20h	07h	06h	05h	04h	03h	02h	01h	00h
18h-1Fh	Register Bank 3							
10h-17h	Register Bank 2							
08h-0Fh	Register Bank 1							
00h-07h	Register Bank 0							

4.4 Special Function Registers

Table 9 presents the SFRs of the IA8044 and IA8344.

Table 9. Special Function Registers

Symbol	Register Description	Byte Address (Hex)	Bit Addresses (Hex) (MSB–LSB)
ACC	Accumulator	E0h	E7h–E0h
B	B register	F0h	F7h–F0h
PSW	Program Status Word	D0h	D7h–D0h
SP	Stack Pointer	81h	–
DPH	Data Pointer High Byte	82h	–
DPL	Data Pointer Low Byte	83h	–
P0	Port 0	80h	87h–80h
P1	Port 1	90h	97h–90h
P2	Port 2	A0h	A7h–A0h
P3	Port 3	B0h	B7h–B0h
IP	Interrupt Priority	B8h	BCh–B8h
IE	Interrupt Enable	A8h	AFh,ACh–A8h
TMOD	Timer/Counter Mode	89h	–
TCON	Timer/Counter Control	88h	8Fh–88h
TH0	Timer/Counter 0 high byte	8Ch	–
TL0	Timer/Counter 0 low byte	8Ah	–
TH1	Timer/Counter 1 high byte	8Dh	–
TL1	Timer/Counter 1 low byte	8Bh	–
SMD	Serial Mode	C9h	–
STS	SIU Status and Command	C8h	CFh–C8h
NSNR	SIU Send/Receive Count	D8h	DFh–D8h
STAD	SIU Station Address	CEh	–
TBS	Transmit Buffer Start Address	DCh	–
TBL	Transmit Buffer Length	DBh	–
TCB	Transmit Control Byte	DAh	–
RBS	Receive Buffer Start Address	CCh	–
RBL	Receive Buffer Length	CBh	–
RFL	Receive Field Length	CDh	–
RCB	Receive Control Byte	CAh	–
DMA CNT	DMA Count	CFh	–
FIFO	FIFO contents (3 bytes)	DF,DE,DDh	–
SIUST	SIU State Counter	D9h	–

4.5 Ports

Ports P0, P1, P2, and P3 are SFRs. The contents of the SFR can be observed on corresponding pins on the chip. Writing a "1" to any of the ports causes the corresponding pin to be at high level (VCC), and writing a "0" causes the corresponding pin to be held at low level (GND).

All four ports on the chip are bi-directional. Each of them consists of a Latch (SFR P0 to P3), an output driver, and an input buffer, so the CPU can output or read data through any of these ports if they are not used for alternate purposes.

Ports P0, P1, P2, and P3 can perform some alternate functions. Ports P0 and P2 are used to access external memory. In this case, port "p0" outputs the multiplexed lower eight bits of address with "ALE" strobe high and then reads/writes eight bits of data. Port P2 outputs the higher eight bits of address. Keeping "ea" pin low (tied to GND) activates this alternate function for Ports P0 and P2.

Port P3 and P1 can perform some alternate functions. The pins of Port P3 are multifunctional. They can perform the additional functions described in Table 10.

Table 10. Additional Functions of Port P3

Pin	Symbol	Function
P3.0	RxD, I/O	In point-to-point or multipoint configurations (SMD.3 = 0) this pin is I/O and signals the direction of data flow on DATA (P3.1). In loop mode (SMD.3 = 1) and diagnostic mode this pin is RxD, Receive Data input.
P3.1	TxD, DATA	In point-to-point or multipoint configurations (SMD.3 = 0) this pin is DATA and is the transmit/receive data pin. In loop mode (SMD.3 = 1) this pin is the transmit data, TxD pin. Writing a "0" to this port buffer bit enables the diagnostic mode.
P3.2	INT0	External Interrupt 0 input. Also gate control input for Counter 0.
P3.3	INT1	External Interrupt 1 input. Also gate control input for Counter 1.
P3.4	T0	Timer/Counter 0 external input. Setting the appropriate bits in the Special Function Registers TCON and TMOD activates this function.
P3.5	T1, SCLK	Timer/Counter 1 external input. Setting the appropriate bits in the SFRs TCON and TMOD activates this function. Can also function as the external clock source for the SIU.
P3.6	WR	External Data Memory write strobe, active LOW. This function is activated by a CPU write access to External Data Memory (i.e., MOVX @DPTR, A).
P3.7	RD	External Data Memory read strobe, active LOW. This function is activated by a CPU read access from External Data Memory (i.e., MOVX A, @DPTR).
P1.6	RTS	Request To Send output, active low.
P1.7	CTS	Clear To Send input, active low.

4.6 Port Registers

4.6.1 Port 0 (P0)

Table 11 presents the values for Port 0 (P0), a general purpose, 8-bit, I/O port and multiplexed low order address and data bus with open-drain output buffers.

Table 11. Port 0 Register

7	6	5	4	3	2	1	0
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

4.6.2 Port 1 (P1)

Table 12 presents the values for Port 1 (P1), a general purpose, eight-bit, I/O port with pullups and auxiliary functions.

Table 12. Port 1 Register

7	6	5	4	3	2	1	0
CTS/P1.7	RTS/P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

- Bit [7]—P1.7/Clear To Send input
- Bit [6]—P1.6/Request To Send output
- Bit [5]—P1.5
- Bit [4]—P1.4
- Bit [3]—P1.3
- Bit [2]—P1.2
- Bit [1]—P1.1
- Bit [0]—P1.0

4.6.3 Port 2 (P2)

Table 13 presents the values for Port 2, a general purpose, 8-bit, I/O port with pullups and high order address bus.

Table 13. Port 2 Register

7	6	5	4	3	2	1	0
P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

4.6.4 Port 3 (P3)

Table 14 presents the values for Port 2, a general purpose, 8-bit I/O port with pullups and auxiliary functions. Bits on this port also function as the SIU data transmit/receive I/O, external interrupt inputs, timer inputs and the read and write strobes for external memory accesses.

Table 14. Port 3 Register

7	6	5	4	3	2	1	0
RD	WR	T1	T0	INT1	INT0	TxD	RxD

- Bit [7]—RD → (P3.7) External Data Memory read strobe, active LOW
- Bit [6]—WR → (P3.6) External Data Memory write strobe, active LOW
- Bit [5]—T1 → (P3.5) Timer/Counter 1 external input
- Bit [4]—T0 → (P3.4) Timer/Counter 0 external input
- Bit [3]—INT1 → (P3.3) External Interrupt 1
- Bit [2]—INT0 → (P3.2) External Interrupt 0
- Bit [1]—TxD → (P3.1) Serial output pin
- Bit [0]—RxD → (P3.0) Serial input pin

4.7 Timers/Counters

4.7.1 Timers 0 and 1

The IA8X44 has two 16-bit timer/counter registers, Timer 0 and Timer 1. Both can be configured for counter or timer operations. In timer mode, the register is incremented every machine cycle, which means that it counts up after every 12 oscillator periods. In counter mode, the register is incremented when the falling edge is observed at the corresponding input pin T0 or T1. Because it takes two machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least one machine cycle (12 clock periods).

Four operating modes can be selected for Timer 0 and Timer 1. Two SFRs (TMOD and TCON) are used to select the appropriate mode.

4.7.2 Mode 0

In Mode 0 the timers operate as an 8-bit timer (TH0/1) with a divide by 32-bit prescalar (TL0/1). Mode 0 uses all eight bits of TH0/1 and the lower five bits of TL0/1. The upper three bits of TL0/1 are unknowns. Setting TR0/1 does not reset the registers TH0/1 and TL0/1. As the timer rolls over from all 1s to all 0s it will set the interrupt flag TF0/1.

4.7.3 Mode 1

Mode 1 is the same as Mode 0 except that all eight bits of TL0/1 are used instead of just the lower five bits.

4.7.4 Mode 2

Mode 2 configures TL0/1 as an 8-bit counter with automatic reload from the contents of TH0/1. Overflow of TL0/1 causes the interrupt TF0/1 to be set and the reload to occur. The contents of TH0/1 are not affected by the reload.

4.7.5 Mode 3

Mode 3 creates two separate 8-bit counters from TL0 and TH0. TL0 uses the Timer 0 mode bits from TMOD, TMOD.0 through TMOD.3. TH0 is a timer only (not a counter) and uses Timer 1's control bits, TR1 and TF1, for operation. Timer 1 can still be used if an interrupt is not required by switching it in and out of its own Mode 3. With TMOD.4 and TMOD.5 both high, Timer 1 will stop and hold its count.

4.7.6 Timer Mode (TMOD)

Table 15 presents the values for the Timer Mode register, which contains bits that select the mode that the timers are to be operated in. The lower nibble controls Timer 0 and the upper nibble controls Timer 1. Table 16 presents the timer mode select bits.

Table 15. Timer Mode Register

7	6	5	4	3	2	1	0
GATE	C/T	M1	M0	GATE	C/T	M1	M0

- Bit [7]—GATE → (TMOD.7) If set, enables external gate control for Counter/Timer 1 (pin INT1 for Counter 1). When INT1 is high, and TR1 bit is set (see TCON register), the counter is incremented every falling edge on T1 input pin.
- Bit [6]—C/T → (TMOD.6) C/T selects Timer 1 or Counter 1 operation. When set to 1, the counter operation is performed. When cleared to 0, the register will function as a timer.
- Bit [5]—M1 → (TMOD.5) Timer 1 mode selector bit.
- Bit [4]—M0 → (TMOD.4) Timer 1 mode selector bit.
- Bit [3]—GATE → (TMOD.3) If set, enables external gate control for Counter/Timer 0 (pin INT0 for Counter 0). When INT0 is high, and TR0 bit is set (see TCON register), the counter is incremented every falling edge on T0 input pin.

- Bit [2]—C/T → (TMOD.2) C/T selects Timer 0 or Counter 0 operation. When set to 1, the counter operation is performed. When cleared to 0, the register will function as a timer.
- Bit [1]—M1 → (TMOD.1) Timer 0 mode selector bit.
- Bit [0]—M0 → (TMOD.0) Timer 0 mode selector bit.

Table 16. Timer Mode Select Bits

M1	M0	Operating Mode	
0	0	0	13-bit timer
0	1	1	16-bit timer/counter
1	0	2	8-bit auto-reload timer/counter
1	1	3	Timer 0–TL0 is a standard 8-bit timer/counter controlled by Timer 0 control bits. TH0 is an 8-bit timer function only, controlled by Timer 1 control bits.
1	1	3	Timer/Counter 1 stopped and holds its count. Can be used to start/stop Timer 1 when Timer 0 is in Mode 3.

4.7.7 Timer Control (TCON)

Table 17 presents the timer control register, which provides control bits that start and stop the counters. It also contains bits to select the type of external interrupt desired, edge or level. Additionally, TCON contains status bits showing when a timer overflows and when an interrupt edge has been detected.

Table 17. Timer Control Register

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

- Bit [7]—TF1 → (TCON.7) Timer 1 overflow flag set by hardware when Timer 1 overflows. This flag should be cleared by software. In Mode 3 this bit is controlled by TH0.
- Bit [6]—TR1 → (TCON.6) Timer 1 run control bit. If cleared, Timer 1 stops. In Mode 3 this bit controls TH0.
- Bit [5]—TF0 → (TCON.5) Timer 0 overflow flag set by hardware when Timer 0 overflows. This flag should be cleared by software.
- Bit [4]—TR0 → (TCON.4) Timer 0 run control bit. If cleared, Timer 0 stops.
- Bit [3]—IE1→ (TCON.3) Interrupt 1 edge flag. Set by hardware, when falling edge on external pin INT1 is detected cleared when interrupt is processed.

- Bit [2]—IT1→ (TCON.2) Interrupt 1 type control bit. Selects falling edge or low level on input pin to cause interrupt.
- Bit [1]—IE0→ (TCON.1) Interrupt 0 edge flag. Set by hardware, when falling edge on external pin INT1 is observed. Cleared when interrupt is processed.
- Bit [0]—IT0→ (TCON.0) Interrupt 0 type control bit. Selects falling edge or low level on input pin to cause interrupt.

4.7.8 Timer 0 High Byte (TH0)

Table 18 presents the high-order byte of Timer/Counter 0.

Table 18. Timer 0 High Byte Register

7	6	5	4	3	2	1	0
TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

4.7.9 Timer 0 Low Byte (TL0)

Table 19 presents the low-order byte of Timer/Counter 0.

Table 19. Timer 0 Low Byte Register

7	6	5	4	3	2	1	0
TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

4.7.10 Timer 1 High Byte (TH1)

Table 20 presents the high-order byte of Timer/Counter 1.

Table 20. Timer 1 High Byte Register

7	6	5	4	3	2	1	0
TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

4.7.11 Timer 1 Low Byte (TL1)

Table 21 presents the low order byte of Timer/Counter 1.

Table 21. Timer 1 Low Byte Register

7	6	5	4	3	2	1	0
TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

4.7.12 Timer/Counter Configuration

Figures 7, 8, 9, and 10 present the configurations of Timer 0 Mode 0, Timer 0 Mode 1, Timer 0 Mode 2, and Timer 0 Mode 3, respectively.

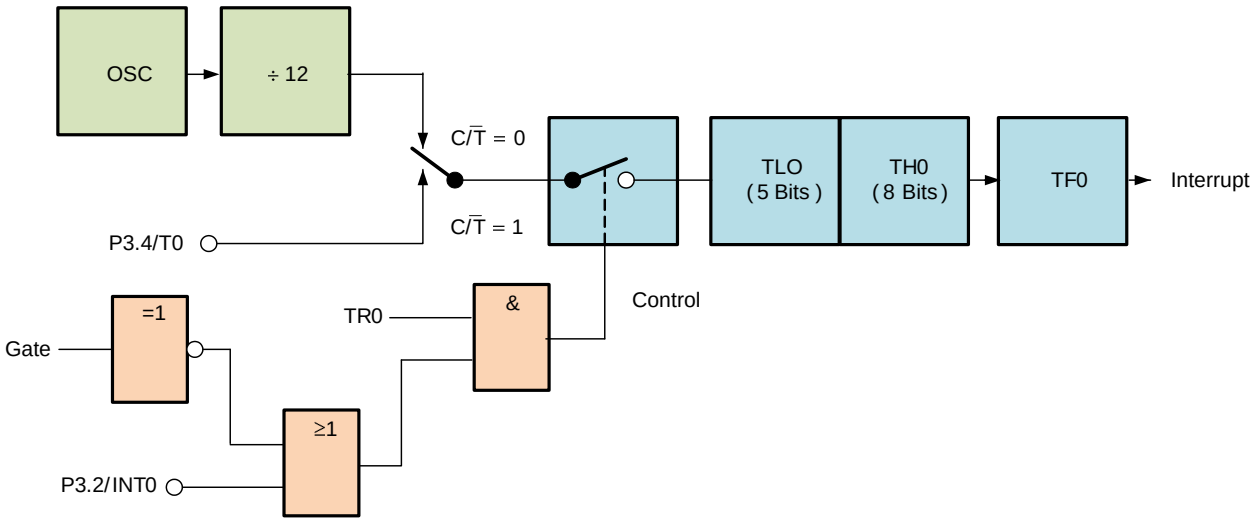


Figure 7. Timer 0 Mode 0

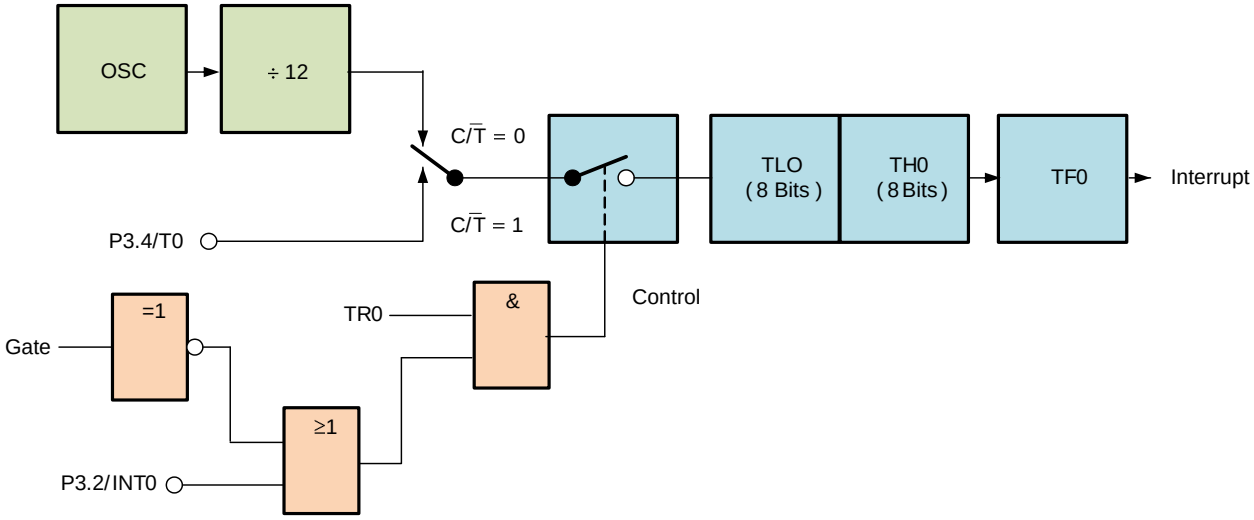


Figure 8. Timer 0 Mode 1

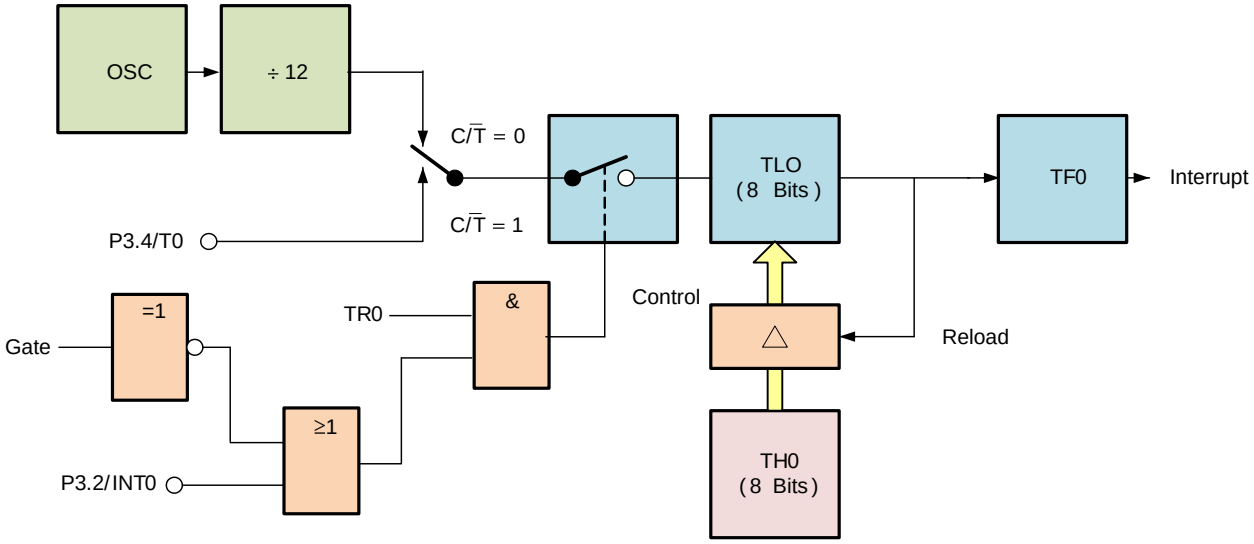


Figure 9. Timer 0 Mode 2

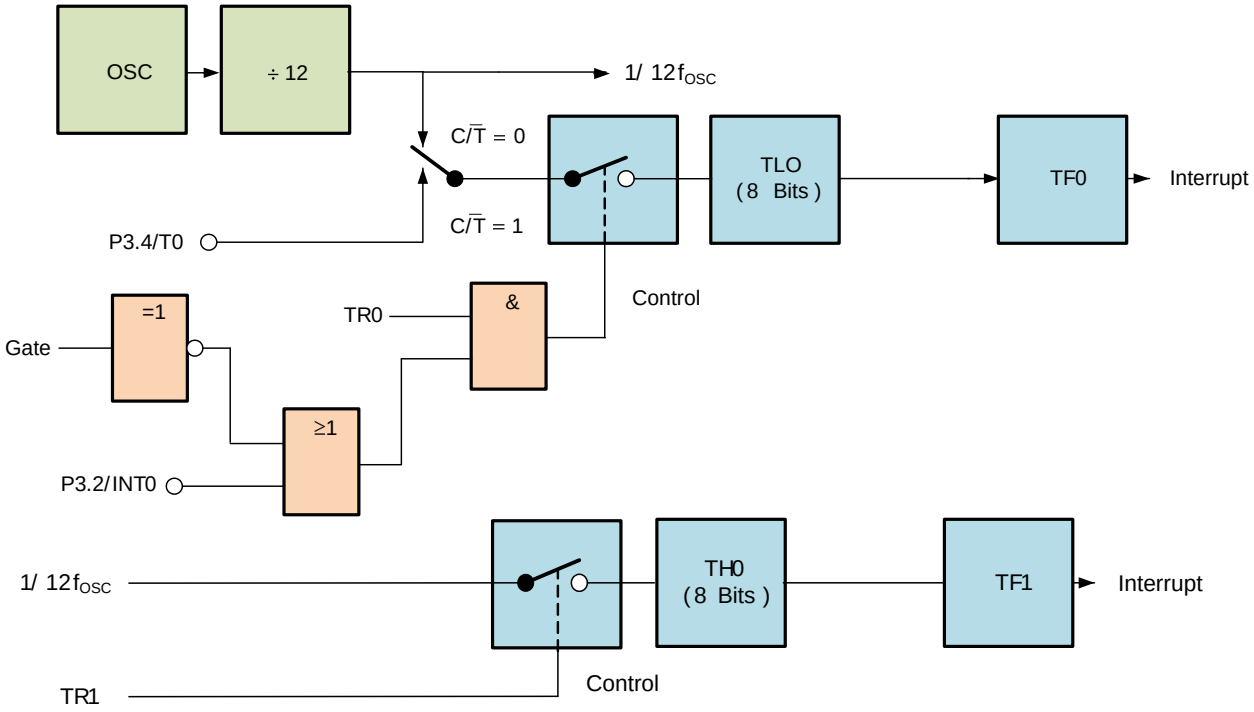


Figure 10. Timer 0 Mode 3

4.8 General CPU Registers

4.8.1 Accumulator (ACC)

Table 22 presents the Accumulator Register. Most instructions use the accumulator to hold the operand. The mnemonics for accumulator-specific instructions refer to accumulator as A, not ACC.

Table 22. Accumulator Register

7	6	5	4	3	2	1	0
ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

4.8.2 B Register (B)

Table 23 presents the B register, which is used during multiply and divide instructions. It can also be used as a scratch-pad register to hold temporary data.

Table 23. B Register

7	6	5	4	3	2	1	0
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

4.8.3 Program Status Word (PSW)

Table 24 presents program status word, which contains CPU status flags, register select bits, and user flags.

Table 24. Program Status Word Register

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	–	P

- Bit [7]—CY → (PSW.7) Carry flag for carry out of or into Bit [7]
- Bit [6]—AC → (PSW.7) Auxiliary carry flag for carry out of or into Bit [3]
- Bit [5]—F0 → (PSW.7) General purpose Flag 0 available for user
- Bit [4]—RS1 → (PSW.7) Register bank select control Bit [1], used to select working register bank
- Bit [3]—RS0 → (PSW.7) Register bank select control Bit [0], used to select working register bank

- Bit [2]—OV → (PSW.7) Overflow flag
- Bit [1]—(PSW.7) User defined flag
- Bit [0]—P → (PSW.7) Parity flag, affected by hardware to indicate odd/even number of "one" bits in the Accumulator (i.e., even parity)

The state of Bits RS1 and RS0 selects the working registers bank as presented in Table 25.

Table 25. RS1/RS0 Bank Selections by State

RS1/RS0	Bank selected location
00	Bank 0 (00H–07H)
01	Bank 1 (08H–0FH)
10	Bank 2 (10H–17H)
11	Bank 3 (18H–1FH)

4.8.4 Stack Pointer (SP)

Table 26 presents the stack pointer, which is a 1-byte register initialized to 07H after reset. This register is incremented before PUSH and CALL instructions, causing the stack to begin at location 08H. The stack pointer points to a location in internal RAM.

Table 26. Stack Pointer

7	6	5	4	3	2	1	0
SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

4.8.5 Data Pointer (DPTR)

The data pointer (DPTR) is two bytes wide. Table 27 presents the highest, which is DPH. Table 28 presents the lower part, DPL. It can be loaded as a 2-byte register (MOV DPTR,#data16) or as two registers (MOV DPL,#data8 each). It is generally used to access external code (MOVC A,@A+DPTR each) or data space (MOV A,@DPTR).

Table 27. Data Pointer (High) Register

7	6	5	4	3	2	1	0
DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Table 28. Data Pointer (Low) Register

7	6	5	4	3	2	1	0
DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

4.9 Interrupts

The IA8044/IA8344 provides five interrupt sources. There are two external interrupts accessible through pins INT0 and INT1, edge or level sensitive (falling edge or low level). There are also internal interrupts associated with Timer 0 and Timer 1 and an internal interrupt from the SIU.

4.9.1 External Interrupts

The choice between external interrupt level or transition activity is made by setting IT1 and IT0 bits in the SFR TCON. When the interrupt event happens, a corresponding Interrupt Control Bit is set (IT0 or IT1). This control bit triggers an interrupt if the appropriate interrupt bit is enabled. When the interrupt service routine is vectored, the corresponding control bit (IT0 or IT1) is cleared, provided that the edge triggered mode was selected. If level mode is active, the external requesting source controls flags IT0 or IT1 by the logic level on pins INT0 or INT1 (0 or 1).

4.9.2 Timer 0 and Timer 1 Interrupts

Timer 0 and 1 interrupts are generated by TF0 and TF1 flags, which are set by the rollover of Timers 0 and 1, respectively. When an interrupt is generated, the flag that caused this interrupt is cleared by the hardware if the CPU accessed the corresponding interrupt service vector. This can be done only if this interrupt is enabled in the IE register.

4.9.3 Serial Interface Unit Interrupt

The SIU generates an interrupt when a frame is received or transmitted. No interrupts are generated for a received frame with errors.

4.9.4 Interrupt Priority Level Structure

There are two priority levels in the IA8044/IA8344—any interrupt can be individually programmed to a high or low priority level. Modifying the appropriate bits in the SFR IP can accomplish this. A low-priority interrupt service routine will be interrupted by a high-priority interrupt. However, the high-priority interrupt cannot be interrupted.

If two interrupts of the same priority level occur, an internal polling sequence determines which will be processed first. This polling sequence is a second priority structure defined as follows:

- IE0 1—highest
- TF0 2
- IE1 3
- TF1 4
- SIU—lowest

4.9.5 Interrupt Handling

The interrupt flags are sampled during each machine cycle. The samples are polled during the next machine cycle. If an interrupt flag is captured, the interrupt system will generate an LCALL instruction to the appropriate service routine, provided that this is not disabled by the following conditions:

- An interrupt of the same or higher priority is processed.
- The current machine cycle is not the last cycle of the instruction (the instruction cannot be interrupted).
- The instruction in progress is RETI or any write to IE or IP registers.

Note: If an interrupt is disabled and the interrupt flag is cleared before the blocking condition is removed, no interrupt will be generated because the polling cycle will not sample any active interrupt condition. In other words, the interrupt condition is not remembered; every polling cycle is new.

4.9.6 Interrupt Priority Register (IP)

This register sets the interrupt priority to high or low for each interrupt. When the bit is set, it selects high priority. Within each level the interrupts are prioritized as follows:

- External Interrupt 0
- Timer/Counter 0
- External Interrupt 1
- Timer/Counter 1
- SIU

An interrupt process routine cannot be interrupted by an interrupt of lesser or equal priority (see Table 29).

Table 29. Interrupt Priority Register

7	6	5	4	3	2	1	0
–	–	–	PS	PT1	PX1	PT0	PX0

- Bit [7]—(IP.7)
- Bit [6]—(IP.6)
- Bit [5]—(IP.5)
- Bit [4]—PS → (IP.4) SIU interrupt priority bit

- Bit [3]—PT1 → (IP.3) Timer 1 interrupt priority bit
- Bit [2]—PX1 → (IP.2) External Interrupt 1 interrupt priority bit
- Bit [1]—PT0 → (IP.1) Timer 0 interrupt priority bit
- Bit [0]—PX0 → (IP.0) External Interrupt 0 interrupt priority bit

4.9.7 Interrupt Enable Register (IE)

Table 30 presents the interrupt enable register, which contains the global interrupt enable bit and individual interrupt enable bits. Setting a bit enables the corresponding interrupt.

Table 30. Interrupt Enable Register

7	6	5	4	3	2	1	0
EA	–	–	ES	ET1	EX1	ET0	EX0

- Bit [7]—EA → (PCON.7) Enable all interrupts bit
- Bit [6]—(PCON.6)
- Bit [5]—(PCON.5)
- Bit [4]—ES → (PCON.4) SIU interrupt enable bit
- Bit [3]—ET1 → (PCON.3) Timer 1 interrupt enable bit
- Bit [2]—EX1→ (PCON.2) External Interrupt 1 interrupt enable bit
- Bit [1]—ET0→ (PCON.1) Timer 0 interrupt enable bit
- Bit [0]—EX0→ (PCON.7) External Interrupt 0 interrupt enable bit

4.10 SIU—Serial Interface Unit

The SIU is a serial interface customized to support SDLC/HDLC protocol. As such, it supports Zero Bit insertion/deletion, flags automatic access recognition and a 16-bit CRC. The SIU has two modes of operation AUTO and FLEXIBLE. The AUTO mode uses a subset of the SDLC protocol implemented in hardware. This frees the CPU from having to respond to every frame but limits the frame types. In the FLEXIBLE mode every frame is under CPU control and therefore more options are available. The SIU is controlled by and communicates to the CPU by using several SFRs. Data transmitted by or received by the SIU is stored in the 192-byte internal RAM in blocks referred to as the transmit and receive buffers. The SIU can support operation in one of

three serial data link configurations, 1) half-duplex, point-to-point, 2) half-duplex, multipoint, or 3) loop mode.

4.10.1 SIU Special Function Registers

The CPU controls the SIU and receives status from the SIU via 11 SFRs. The Serial Interface Unit Control Registers are detailed in the sections that follow.

4.10.2 Serial Mode Register (SMD)

Table 31 presents the serial mode register, which sets the operational mode of the SIU. The CPU can read and write SMD. The SIU can read SMD. To prevent conflicts between CPU and SIU, accesses to SMD the CPU should write SMD only when RTS and RBE bits in the STS register are both zero. SMD is normally only accessed during initialization. This register is byte addressable. Table 32 presents the serial mode select clock mode bits.

Table 31. Serial Mode Register

7	6	5	4	3	2	1	0
SCM2	SCM1	SCM0	NRZI	LOOP	PFS	NB	NFCS

- Bit [7]—SCM2 → (SMD.7) Select clock mode—Bit [2].
- Bit [6]—SCM1 → (SMD.6) Select clock mode—Bit [1].
- Bit [5]—SCM0 → (SMD.5) Select clock mode—Bit [0].
- Bit [4]—NRZI → (SMD.4) When set selects NRZI encoding otherwise NRZ.
- Bit [3]—LOOP → (SMD.3) When set, selects loop configuration, else point-to-point mode.
- Bit [2]—PFS → (SMD.2) Pre-frame sync mode. When set, causes two bytes to be transmitted before the first flag of the frame for DPLL synchronization. If NRZI is set, 00H is transmitted, otherwise 55H. This ensures that 16 transitions are sent before the opening flag.
- Bit [1]—NB → (SMD.1) Non-buffered mode. No control field contained in SDLC frame.
- Bit [0]—NFCS → (SMD.0) When set, selects No FCS field contained in the SDLC frame.

Table 32. Serial Mode Select Clock Mode Bits

SCM 2 1 0	Clock Mode	Data Rate (bits/sec)[a]
0 0 0	Externally clocked	0–2.4M[b]
0 0 1	Undefined	
0 1 0	Self clocked, timer overflow	244–62.5K
0 1 1	Undefined	
1 0 0	Self clocked, external 16X	0–375K
1 0 1	Self clocked, external 32X	0–187.5K
1 1 0	Self clocked, internal fixed	375K
1 1 1	Self clocked, internal fixed	187.5K

[a]Based on a12-MHz crystal frequency.
[b]0–1 Mbps in loop configuration.

4.10.3 Status/Command Register (STS)

Table 33 presents the Status/Command Register, which provides SIU control from and status to the CPU. The SIU can read the STS and can write certain bits in the STS. The CPU can read and write the STS. Accessing the STS by the CPU via two cycle instructions—JBC bit,rel and MOV bit,C—should not be used. STS is bit addressable.

Table 33. Status/Command Register

7	6	5	4	3	2	1	0
TBF	RBE	RTS	SI	BOV	OPB	AM	RBP

- Bit [7]—TBF → (STS.7) Transmit buffer full. TBF is set by the CPU to indicate that the transmit buffer is ready and TBF is cleared by the SIU.

- Bit [6]—RBE → (STS.6) Receive buffer empty. RBE is set by the CPU when it is ready to receive a frame or has just read the buffer. RBE is cleared by the SIU when a frame has been received. Can be thought of as a Receive Enable.

- Bit [5]—RTS → (STS.5) Request to send. This bit is set when the SIU is ready to transmit or is transmitting. May be written by the SIU in AUTO mode. RTS is only applied to the external pin in non-loop mode. Can be thought of as a Transmit Enable.

  Note: RTS signal at the pin (P1.6) is the inverted version of this bit.

- Bit [4]—SI → (STS.4) SIU interrupt. This bit is set by the SIU and should be cleared by the CPU before returning from the interrupt routine.

- Bit [3]—BOV → (STS.3) Receive buffer overrun. The SIU can set or clear BOV.

- Bit [2]—OPB → (STS.2) Optional poll bit. When set, the SIU will AUTO respond to an optional poll (UP with P=0). The SIU can set or clear the OPB.
- Bit [1]—AM → (STS.1) Auto mode. Dual purpose bit depending upon the setting of bit NB (SMD.1). If NB is cleared, AM selects the AUTO mode when set, Flexible mode when clear. If NB is set, AM selects the addressed mode when set and the non-addressed mode when clear. The SIU can clear AM.
- Bit [0]—RBP → (STS.0) Receive buffer protect. When set, prevents writing of data into the receive buffer. Causes RNR response instead of RR in AUTO mode.

4.10.4 Send/Receive Count Register (NSNR)

Table 34 presents the Send/Receive Count Register, which contains both the transmit and receive sequence numbers in addition to the tally error indications. The CPU can read and write the STS. Accessing the STS by the CPU via two cycle instructions—JBC bit,rel and MOV bit,C—should not be used. The SIU can read and write the NSNR. The NS and NR counters are not used in non-AUTO mode. NSNR is bit addressable.

Table 34. Send/Receive Count Register

7	6	5	4	3	2	1	0
NS2	NS1	NS0	SES	NR2	NR1	NR0	SER

- Bit [7]—NS2 → (NSNR.7) Send sequence counter, Bit [2].
- Bit [6]—NS1 → (NSNR.6) Send sequence counter, Bit [1].
- Bit [5]—NS0 → (NSNR.5) Send sequence counter, Bit [0].
- Bit [4]—SES → (NSNR.4) Sequence error send. NR (P) ≠ NS (S) and NR (P) ≠ NS (S) + 1.
- Bit [3]—NR2 → (NSNR.3) Receive sequence counter, Bit [2].
- Bit [2]—NR1 → (NSNR.2) Receive sequence counter, Bit [1].
- Bit [1]—NR0 → (NSNR.1) Receive sequence counter, Bit [0].
- Bit [0]—SER → (NSNR.0) Sequence error receive. NS (P) ≠ NR (S).

4.10.5 Station Address Register (STAD)

Table 35 presents the Station Address Register, which contains the station address (node address) of the chip. The CPU can read or write STAD but should access STAD only when RTS = 0 and RBE = 0. Normally STAD is accessed only during initialization. STAD is byte addressable.

Table 35. Station Address Register

7	6	5	4	3	2	1	0
STAD.7	STAD.6	STAD.5	STAD.4	STAD.3	STAD.2	STAD.1	STAD.0

4.10.6 Transmit Buffer Start Address Register (TBS)

Table 36 presents the Transmit Buffer Start Address Register, which contains the address in internal RAM where the frame to be transmitted (starting with the I-field) is stored. The CPU should access TBS only when the SIU is not transmitting a frame, TBF = 0. TBS is byte addressable.

Table 36. Transmit Buffer Start Address Register

7	6	5	4	3	2	1	0
TBS.7	TBS.6	TBS.5	TBS.4	TBS.3	TBS.2	TBS.1	TBS.0

4.10.7 Transmit Buffer Length Register (TBL)

Table 37 presents the Transmit Buffer Length Register, which contains the length, in number of bytes, of the I-field to be transmitted. TBL = 0 is valid (no I-field). The CPU should access TBL only when the SIU is not transmitting a frame, TBF = 0. The transmit buffer will not wrap around after address 191 (BFH). A buffer end is automatically generated when address 191 is reached. TBL is byte addressable.

Table 37. Transmit Buffer Length Register

7	6	5	4	3	2	1	0
TBL.7	TBL.6	TBL.5	TBL.4	TBL.3	TBL.2	TBL.1	TBL.0

4.10.8 Transmit Control Byte Register (TCB)

Table 38 presents the Transmit Control Byte Register, which contains the byte to be placed in the control field of the transmitted frame during non-AUTO-mode transmission. The CPU should access TCB only when the SIU is not transmitting a frame, TBF = 0. TCB is byte addressable.

Table 38. Transmit Control Byte Register

7	6	5	4	3	2	1	0
TCB.7	TCB.6	TCB.5	TCB.4	TCB.3	TCB.2	TCB.1	TCB.0

4.10.9 Receive Buffer Start Address Register (RBS)

Table 39 presents the Receive Buffer Start Address Register, which contains the address in internal RAM where the frame (starting with the I-field) being received is to be stored. The CPU should write RBS only when the SIU is not receiving a frame, RBE = 0. RBS is byte addressable.

Table 39. Receive Buffer Start Address Register

7	6	5	4	3	2	1	0
RBS.7	RBS.6	RBS.5	RBS.4	RBS.3	RBS.2	RBS.1	RBS.0

4.10.10 Receive Buffer Length Register (RBL)

Table 40 presents the Receive Buffer Length Register, which contains the length, in number of bytes, of the I-field storage area in internal RAM. RBL = 0 is valid (no I-field). The CPU should write RBL only when the SIU is not receiving a frame, RBE = 0. The receive buffer will not wrap around after address 191 (BFH). A buffer end is automatically generated when address 191 is reached. RBL is byte addressable.

Table 40. Receive Buffer Length Register

7	6	5	4	3	2	1	0
RBL.7	RBL.6	RBL.5	RBL.4	RBL.3	RBL.2	RBL.1	RBL.0

4.10.11 Receive Field Length Register (RFL)

Table 41 presents the Receive Field Length Register, which contains the length, in number of bytes, of the I-field of the frame received and stored in internal RAM. RFL = 0 is valid (no I-field). The CPU should access RFL only when the SIU is not receiving a frame, RBE = 0. RFL is loaded by the SIU. RFL is byte addressable.

Table 41. Receive Field Length Register

7	6	5	4	3	2	1	0
RFL.7	RFL.6	RFL.5	RFL.4	RFL.3	RFL.2	RFL.1	RFL.0

4.10.12 Receive Control Byte Register (RCB)

Table 42 presents the Receive Control Byte Register, which contains the control field of the frame received and stored in internal RAM. RCB is only readable by the CPU and the CPU should access RCB only when the SIU is not receiving a frame, RBE = 0. RCB is loaded by the SIU. RCB is byte addressable.

Table 42. Receive Control Byte Register

7	6	5	4	3	2	1	0
RCB.7	RCB.6	RCB.5	RCB.4	RCB.3	RCB.2	RCB.1	RCB.0

4.10.13 DMA Count Register (DMA CNT)

Table 43 presents the DMA Count Register (DMA CNT), which contains the number of bytes remaining for the information field currently being used. This register is an ICE support register. DMA CNT is byte addressable.

Table 43. DMA Count Register (DMA CNT)

7	6	5	4	3	2	1	0
DMA CNT.7	DMA CNT.6	DMA CNT.5	DMA CNT.4	DMA CNT.3	DMA CNT.2	DMA CNT.1	DMA CNT.0

4.10.14 DMA Count Register (FIFO)

Table 44 presents the DMA Count Register (FIFO), which is actually three registers that make a three-byte FIFO. These are used as temporary storage between the eight-bit shift register and the receive buffer when an information field is received. This register is an ICE support register. FIFO is byte addressable.

Table 44. DMA Count Register (FIFO)

7	6	5	4	3	2	1	0
FIFO#[a].7	FIFO#[a].6	FIFO#[a].5	FIFO#[a].4	FIFO#[a].3	FIFO#[a].2	FIFO#[a].1	FIFO#[a].0

[a]1, 2, or 3 for FIFO1, FIFO2, or FIFO3, respectively.

4.10.15 SIU State Counter (SIUST)

Table 45 presents the SIU State Counter Register, which indicates what state the SIU state machine is currently in. This in turn indicates what task the SIU is performing or which field is expected next by the SIU. This register should not be written to. This register is an ICE support register. SIUST is byte addressable.

Table 45. SIU State Counter

7	6	5	4	3	2	1	0
SIUST .7	SIUST .6	SIUST .5	SIUST .4	SIUST .3	SIUST .2	SIUST .1	SIUST .0

4.11 Data Clocking Options

The SIU may be clocked in one of two ways, with an external clock or in a self-clocked mode. In the external clocked mode, a serial clock must be provided on SCLK. This clock must be synchronized to the serial data. Incoming data is sampled at the rising edge of SCLK. Outgoing data is shifted out at the falling edge of SCLK.

In the self-clocked mode, the SIU uses a reference clock and the serial data to reproduce the serial data clock. The reference clock can be an external source applied to SCLK, the IA8044/IA8344's internal clock or the Timer 1 overflow. The reference clock must be 16× or 32× the data rate. A DPLL uses the reference clock and the serial data to adjust the sample time to the center of the serial bit. It does this by adjusting from a serial data transition in increments of 1/16 of a bit time.

The maximum data rate in the externally clocked mode is 2.4 Mbps in a point-to-point configuration and 1.0 Mbps in a loop configuration. With a 12-MHz CPU clock, the maximum data rate in the self-clocked mode with an external clock is 375 Kbps. The maximum data rate in the self-clocked mode with an internal clock will depend on the frequency of the IA8044/IA8344's input clock. An IA8044/IA8344 using a 12-MHz input clock can operate at a maximum data rate of 375 Kbps.

The Serial mode register Bits [5], [6], and [7] select the clocking option for the SIU (see SMD register description).

4.12 Operational Modes

The SIU operates in one of two modes, AUTO or FLEXIBLE. The mode selected determines how much intervention is required by the CPU when receiving and transmitting frames. In both modes, short frames, aborted frames, and frames with CRC errors will be ignored.

AUTO mode allows the SIU to recognize and respond to specific SDLC frames without the CPU's intervention. This provides for a faster turnaround time but restricts the operation of the SIU. When in AUTO mode, the SIU can only act as a normal response secondary station and responses will adhere to IBM's SDLC definitions.

When receiving in the AUTO mode, the SIU receives the frame and examines the control byte. It will then take the appropriate action for that frame. If the frame is an information frame, the SIU will load the receive buffer, interrupt the CPU and make the required response to the primary station. The SIU in AUTO mode can also respond to the following commands from the primary station:

- RR (Receive ready)
- RNR (Receive Not Ready)
- REJ (Reject)

- UP (Unnumbered Poll) also called NSP, (Non-Sequenced Poll), or ORP (Optional Response Poll)

In AUTO mode when the transmit buffer is full, the SIU can transmit an information frame when polled for information. After transmission the SIU waits for acknowledgement from the receiving station. If the response is positive, the SIU interrupts the CPU. If the response is negative, the SIU retransmits the frame. The SIU can send the following responses to the primary station:

- RR (Receive Ready)
- RNR (Receive Not Ready)

The FLEXIBLE mode requires the CPU to control the SIU for both transmitting and receiving. This slows response time but allows full SDLC and limited HDLC compatibility as well as variations. In FLEXIBLE mode, the SIU can act as a primary station. The SIU will interrupt the CPU after completion of a transmission without waiting for a positive acknowledgement from the receiving station (see Table 46).

Table 46. Basic SDLC Frame

FLAG	ADDRESS	CONTROL	INFORMATION	FCS	FLAG

IA8044/IA8344 frame parameters:

- Flag—8 bits
- Address—8 bits
- Control—8 bits
- Information—n bytes (where n ≤ 192)
- FCS—16 bits
- Flag—8 bits

4.13 Frame Format Options

The various frame formats available with the IA8044/IA8344 are the standard SDLC format, the no-control field format, the no-control field and no-address field formats, and the no-FCS field format.

The standard SDLC format consists of an opening flag, an 8-bit address field, an 8-bit control field, an n-byte information field, a 16-bit frame check sequence field, and a closing flag. The FCS is generated by the CCIT-CRC polynomial (X16 + X12 + X5 + 1). The FCS is calculated on the address, control, and information fields. The address and control fields may not be extended. The address is contained in STAD and the control filed is contained in either RCB or TCB. This format is supported by both AUTO and FLEXIBLE modes.

The no-control field format is only supported by the FLEXIBLE mode. In this format, TCB and RCB are not used and the information field starts immediately after the address field. A control field may still be used in the frame but the SIU will treat it as a byte of the information field.

The no-control field and no-address field formats are supported only by the FLEXIBLE mode. In this format STAD, TCB, and RCB are not used and the information field starts immediately after the opening flag. This option can only be used with the no-control field option. A control field and address field may still be used in the frame but the SIU will treat each as a byte of the information field.

The no FCS field format prevents an FCS from being generated during transmission or being checked during reception. This option may be used in conjunction with the other frame format options. This option will work with both FLEXIBLE and AUTO modes. In AUTO mode, it could cause protocol violations. An FCS field may still be used in the frame but the SIU will treat it as a byte of the information field.

All the possible Frame Format combinations are presented in Table 47, along with the bit settings that select a given format.

Table 47. Frame Format Options

Frame Option	NFCS	NB	AM	Frame Format
Standard SDLC FLEXIBLE Mode	0	0	0	Fl | Ad | Co | Inf | FCS | Fl
Standard SDLC AUTO Mode	0	0	1	Fl | Ad | Co | Inf | FCS | Fl
No-Control Field FLEXIBLE Mode	0	1	1	Fl | Ad | Inf | FCS | Fl
No-Control Field No-Address Field FLEXIBLE Mode	0	1	0	Fl | Inf | FCS | Fl
No-FCS Field FLEXIBLE Mode	1	0	0	Fl | Ad | Co | Inf | Fl
No-FCS Field AUTO Mode	1	0	1	Fl | Ad | Co | Inf | Fl

Frame Option	NFCS	NB	AM	Frame Format
No-Control Field No-FCS Field FLEXIBLE Mode	1	1	1	Fl | Ad | Inf | Fl
No-Control Field No-Address Field No-FCS Field FLEXIBLE Mode	1	1	0	Fl | Inf | Fl

Ad = Address field
Co = Control field
FCS = Frame check sequence
Fl = Flag
Inf = Information field

4.14 HDLC Restrictions

The IA8044/IA8344 supports a subset of the HDLC protocol. The differences include the restriction by the IA8044/IA8344 of the serial data to be in 8-bit increments. In contrast, HDLC allows for any number of bits in the information field. HDLC provides an unlimited address field and an extended frame number sequencing. HDLC does not support loop configuration.

4.15 SIU Details

The SIU is composed of two functional blocks with each having several sub blocks. The two blocks are called the bit processor (BIP) and the byte processor (BYP) (see Figure 11).

4.15.1 BIP

The BIP consists of the DPLL, NRZI encoder/decoder, serial/parallel shifter, zero insertion/deletion, shutoff logic, and FCS generation/checking. The NRZI logic compares the current bit to the previous bit to determine if the bit should be inverted. The serial shifter converts the outgoing byte data to bit data and incoming bit data to byte data. The zero insert/delete circuitry inserts and deletes zeros and also detects flags (01111110), go-aheads (GA) (01111111), and aborts (1111111). The pattern 1111110 is detected as an early go-ahead that can be turned into a flag in loop configurations. The shutoff detector is a three-bit counter that is used to detect a sequence of eight zeros, which is the shutoff command in loop-mode transmissions. It is cleared whenever a “1” is detected. The FCS logic performs the generation and checking of the FCS value according to the polynomial described above. The FCS register is set to all 1s prior to each calculation. If a CRC error is generated on a receive frame, the SIU will not interrupt the CPU and the error will be cleared upon receiving an opening flag.

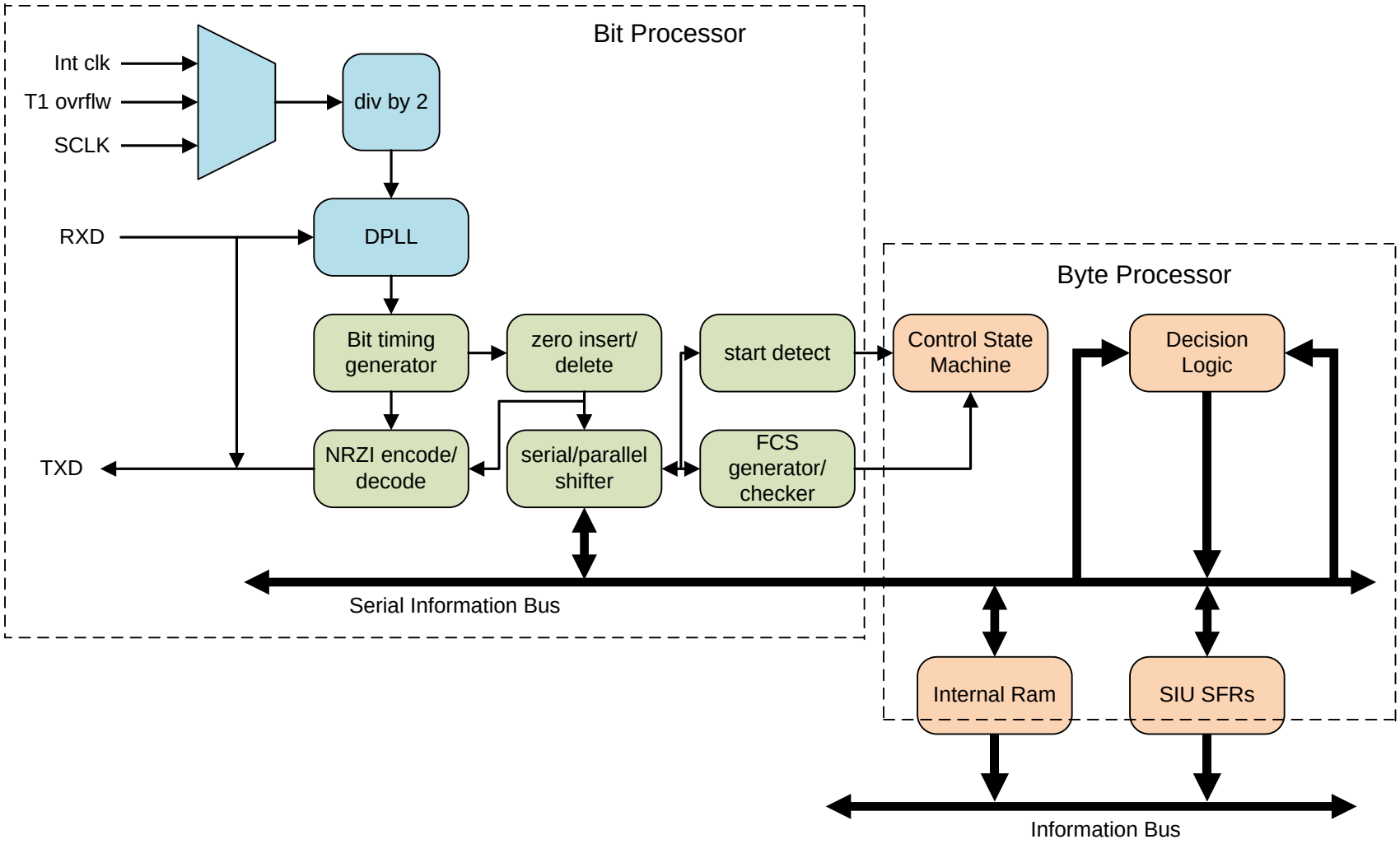


Figure 11. Bit and Byte Processors

4.15.2 BYP

The BYP contains registers and controllers used to perform the manipulations required for SDLC communications. The BYP registers may be accessed by the CPU (see Table 7, SFR Bit Addressable Locations). The BYP contains the SIU state machine that controls transmission and reception of frames.

4.16 Diagnostics

A diagnostic mode is included with the IA8044/IA8344 to allow testing of the SIU. Diagnostics use port pins P3.0 and P3.1. Writing a "0" to P3.1 enables the diagnostic mode. When P3.1 is cleared, writing data to P3.0 has the effect of writing a serial data stream to the SIU. P3.0 is the serial data and any write to Port 3 will clock SCLK. The transmit data may be monitored on P3.1 with any write to Port 3, again clocking SCLK. In the test mode P3.0 and P3.1 pins are placed in the high impedance state (see Figure 12).

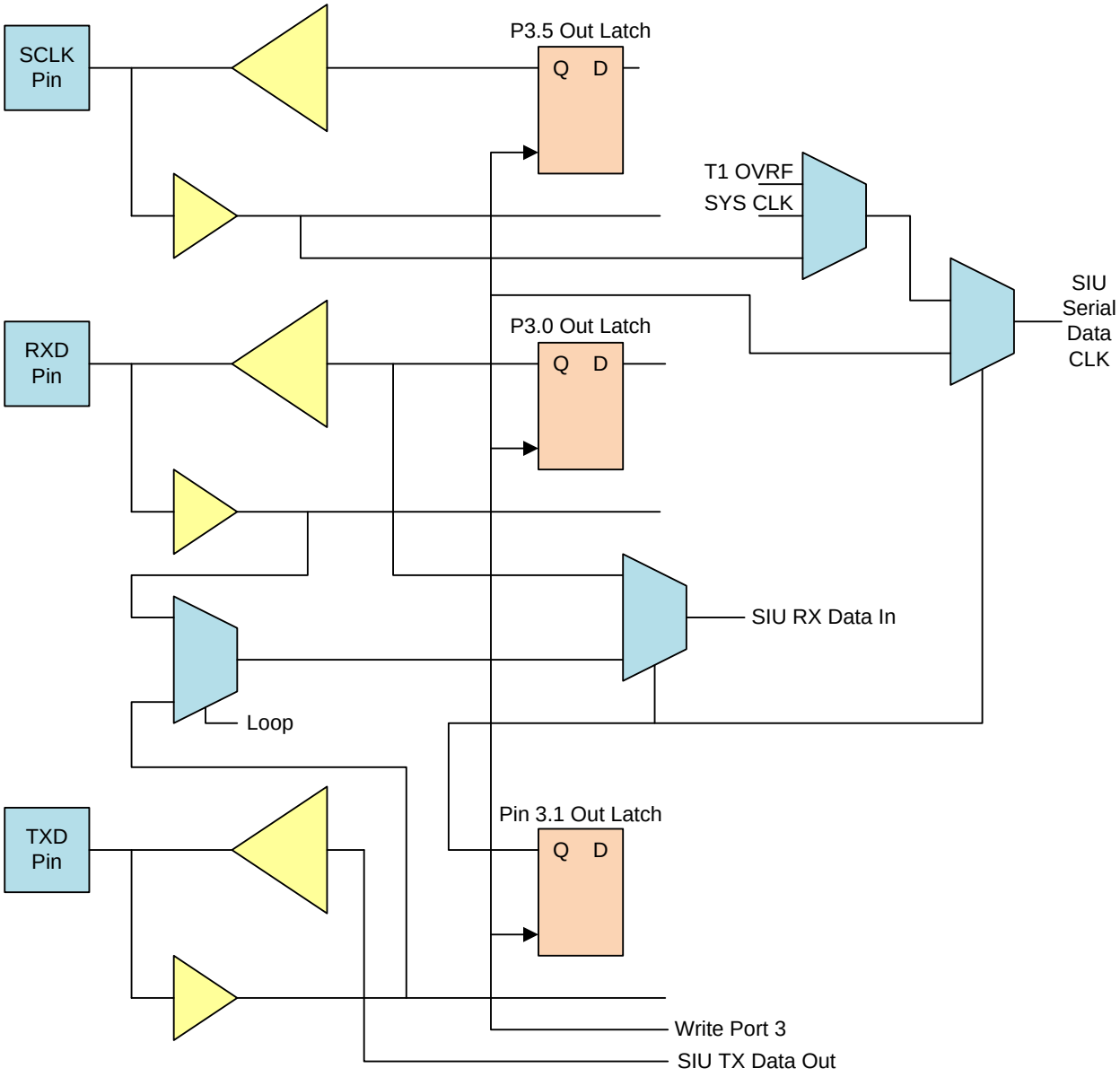


Figure 12. Diagnostic Signal Routing

5. AC Specifications

AC characteristics, external data memory characteristics, serial interface characteristics, and external clock drive characteristics are provided in Tables 48 through 51, respectively.

T_A = −40°C to +85°C, VDD = 5V ± 10%, VSS = 0V, Load Capacitance = 87pF

Table 48. External Program Memory Characteristics

Symbol	Parameter	12 MHz Osc		Variable Clock 1/TCLCL = 3.5 MHz to 12 MHz		Unit
		Min	Max	Min	Max	
TLHLL	ALE Pulse Width	171	–	2TCLCL+4	–	ns
TAVLL	Address Valid to ALE Low	75	–	TCLCL-8	–	ns
TLLAX	Address Hold After ALE Low	74	–	TCLCL-9	–	ns
TLLIV	ALE Low to Valid Instr. In.	–	298	–	4TCLCL-35	ns
TLLPL	ALE Low to PSENn Low	83	–	TCLCL	–	ns
TPLPH	PSENn Pulse Width	254	–	3TCLCL+4	–	ns
TPLIV	PSENn Low to Valid Instr. In	–	215	–	3TCLCL-35	ns
TPXIX	Input Instr. Hold After PSENn	0	–	0	–	ns
TPXIZ	Input Instr. Float After PSENn	–	76	–	TCLCL-7	ns
TPXAV	PSENn to Address Valid	91	–	TCLCL+8	–	ns
TAVIV	Address to Valid Instr. In	–	373	–	5TCLCL-43	ns
TAZPL	Address Float to PSENn	-9	–	-9	–	ns
TCY	Machine cycle	996	–	12TCLCL	–	ns

Table 49. External Data Memory Characteristics

Symbol	Parameter	12 MHz Osc		Variable Clock 1/TCLCL = 3.5 MHz to 12 MHz		Unit
		Min	Max	Min	Max	
TRLRH	RDn Pulse Width	487	–	6TCLCL-13	–	ns
TWLWH	WRn Pulse Width	487	–	6TCLCL-13	–	ns
TLLAX	Address Hold After ALE	74	–	TCLCL-9	–	ns
TRLDV	RDn Low to Valid Data In	–	383	–	5TCLCL-35	ns
TRHDX	Data Hold After RDn	0	–	0	–	ns
TRHDZ	Data Float After RDn	–	165	–	2TCLCL-2	ns
TLLDV	ALE Low to Valid Data In	–	633	–	8TCLCL-34	ns
TAVDV	Address to Valid Data In	–	708	–	9TCLCL-42	ns
TLLWL	ALE Low to RDn or WRn Low	250	250	3TCLCL	3TCLCL	ns
TAVWL	Address to RDn or WRn Low	325	–	4TCLCL-8	–	ns
TQVWX	Data Valid to WRn Transition	76	–	TCLCL-7	–	ns
TQVWH	Data Setup Before WRn High	563	–	7TCLCL-20	–	ns
TWHQX	Data Held After WRn	86	–	TCLCL+3	–	ns

TRLAZ	RDn Low to Address Float	–	9	–	9	ns
TWHLH	RDn or WRn High to ALE High	83	83	TCLCL	TCLCL	ns

Table 50. Serial Interface Characteristics

Symbol	Parameter	Min	Max	Unit
TDCY	Data Clock	420	–	ns
TDCL	Data Clock Low	184	–	ns
TDCH	Data Clock High	184	–	ns
tTD	Transmit Data Delay	–	125	ns
tDSS	Data Setup Time	26	–	ns
tDHS	Data Hold Time	58	–	ns

Table 51. External Clock Drive Characteristics

Symbol	Parameter	Min	Max	Unit
TCLCL	Oscillator Period	52	–	ns

5.1 Memory Access Waveforms

The IA8044/IA8344 program memory read cycle, data memory read cycle, and data memory write cycle are presented in Figures 13 through 15, respectively.

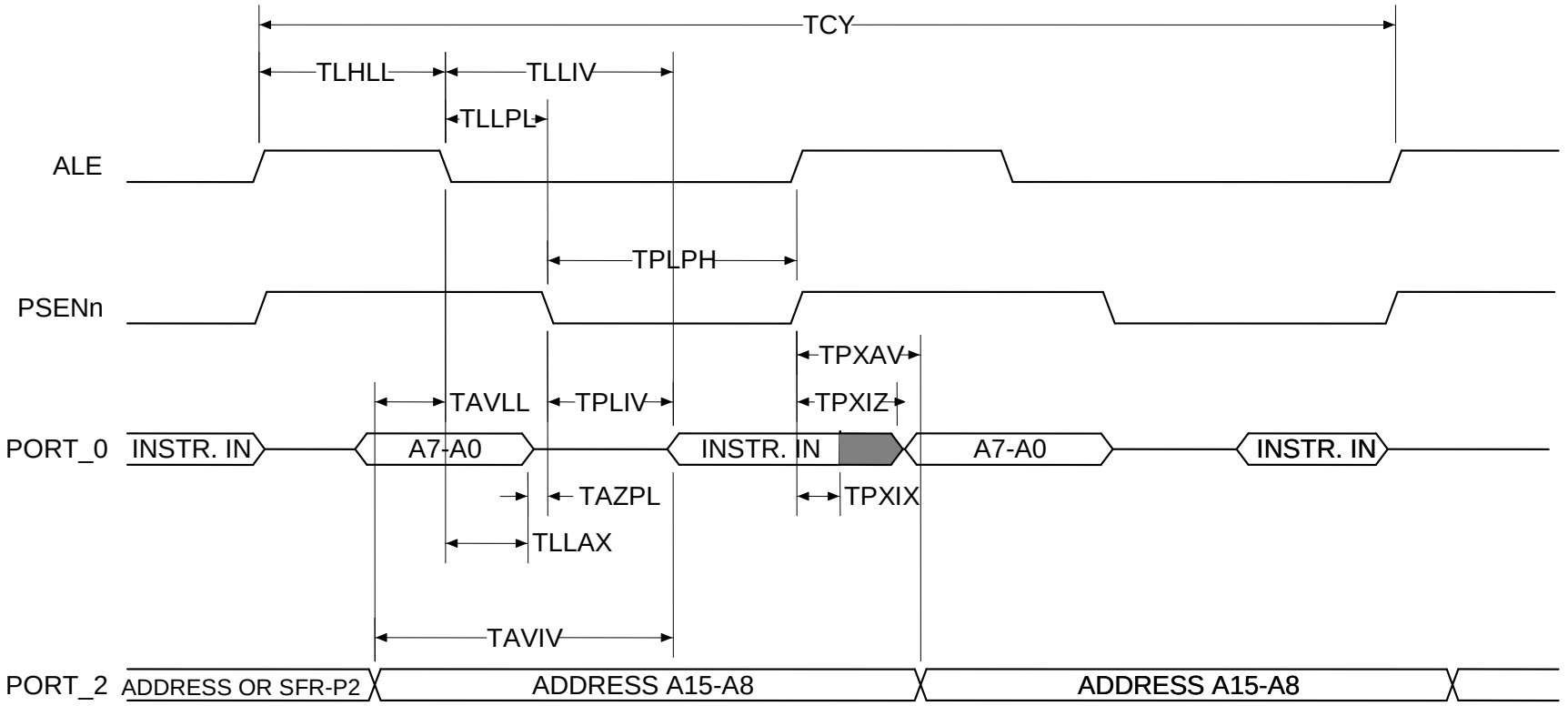


Figure 13. Program Memory Read Cycle

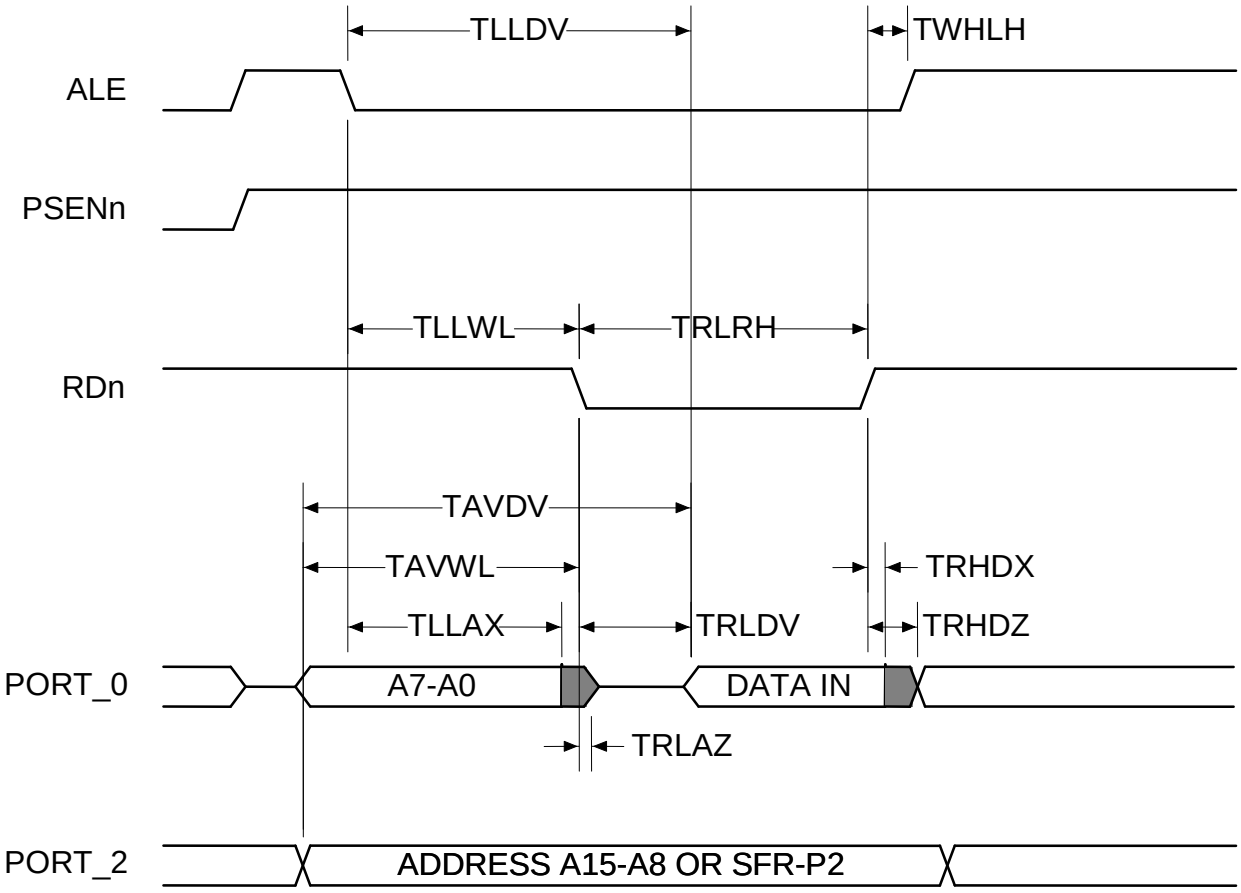


Figure 14. Data Memory Read Cycle

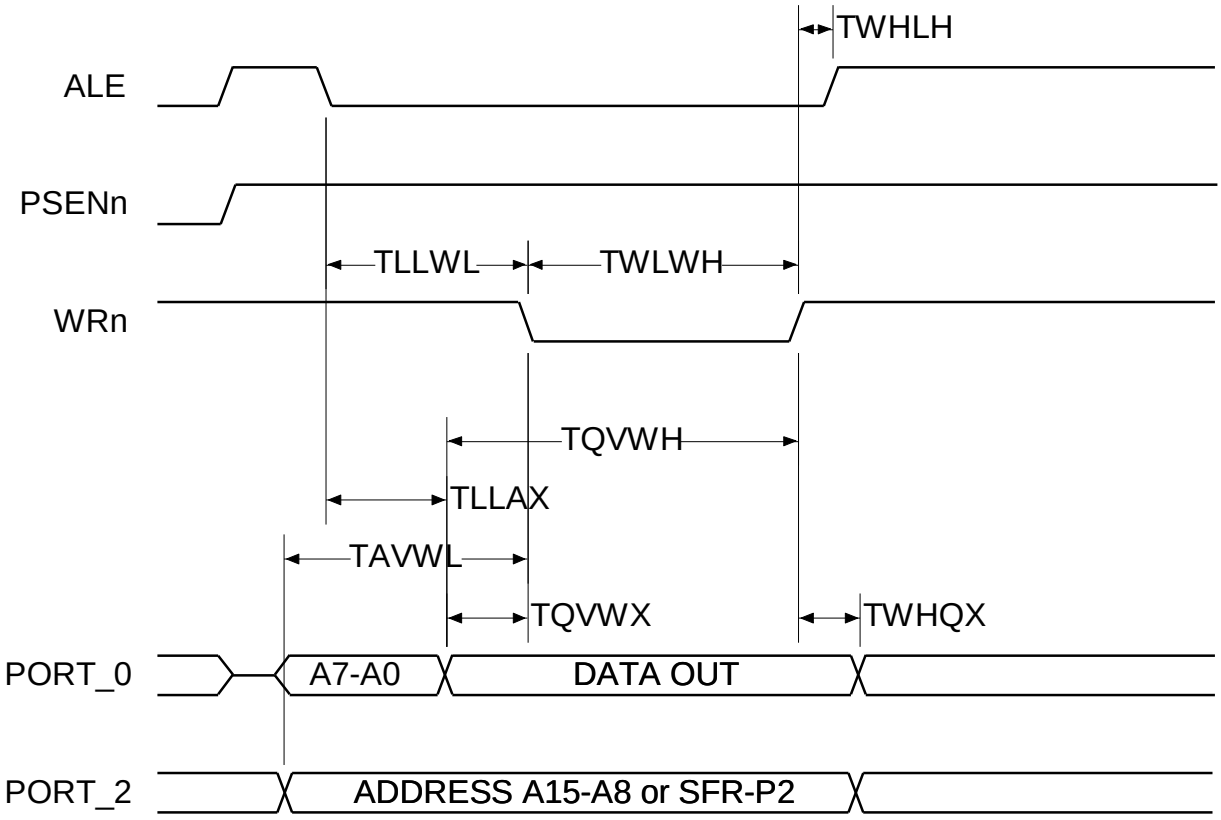


Figure 15. Data Memory Write Cycle

5.2 Serial I/O Waveforms

The IA8044/IA8344 synchronous data transmission and synchronous data reception are presented in Figures 16 and 17, respectively.

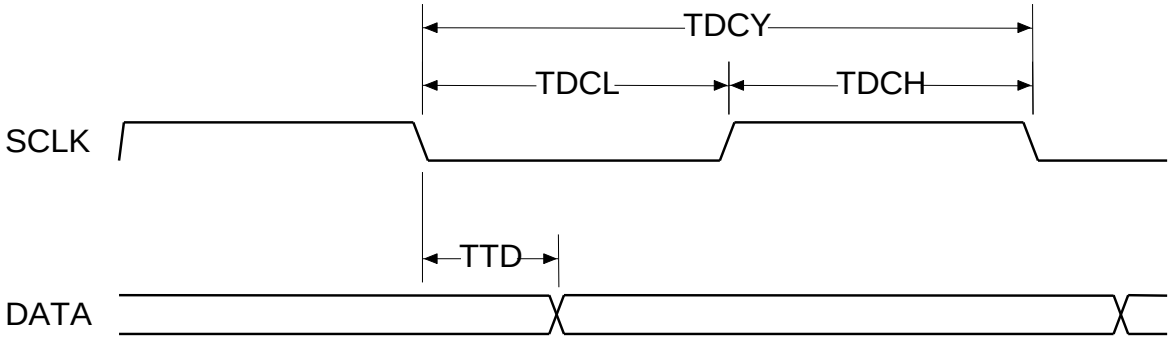


Figure 16. Synchronous Data Transmission

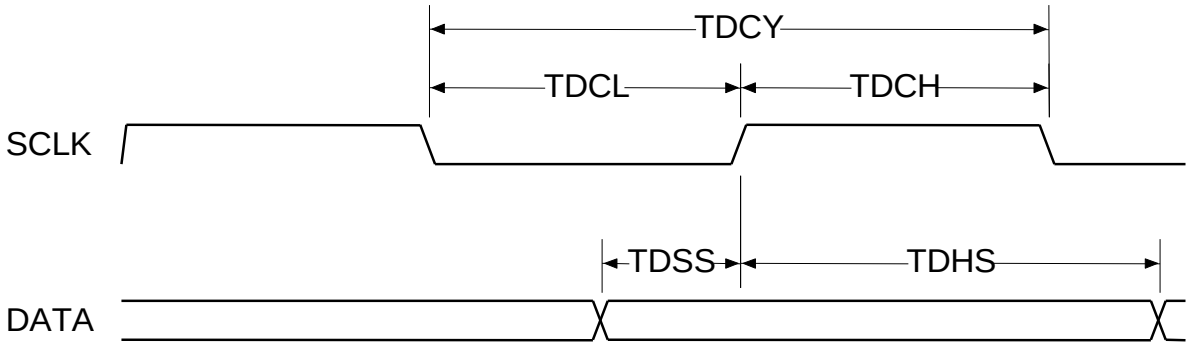


Figure 17. Synchronous Data Reception

6. Reset

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods) while the oscillator is running. The CPU responds by generating an internal reset, which is executed during the second cycle in which RST is high.

The internal reset sequence affects all SFRs as shown in Table 52. The internal reset sequence does not affect the contents of internal RAM.

Table 52. Reset Values Register

Register	Reset value
PC	0000H
ACC	00000000B
B	00000000B
PSW	00000000B
SP	00000111B
DPTR	0000H
P0–P3	11111111B
IP	XXX00000B
IE	0XX00000B
TMOD	00000000B
TCON	00000000B
TH0	00000000B
TL0	00000000B
TH1	00000000B
TL1	00000000B
SMD	00000000B
STS	00000000B
NSNR	00000000B
STAD	XXXXXXXXB
TBS	XXXXXXXXB
TBL	XXXXXXXXB
TCB	XXXXXXXXB
RBS	XXXXXXXXB
RBL	XXXXXXXXB
RFL	XXXXXXXXB
RCB	XXXXXXXXB
DMA CNT	00000000B
FIFO1	00000000B
FIFO2	00000000B
FIFO3	00000000B
SIUST	00000001B

7. Instruction Set

The IA8044 and IA8344 architecture and instruction set are identical to the Intel 8051's. Tables 53 through 57 present the instruction set of the IA8044/IA8344 microcontroller core.

Table 53. Arithmetic Operations

Mnemonic	Description	Byte	Cycle
ADD A,Rn	Add register to accumulator	1	1
ADD A, direct	Add direct byte to accumulator	2	1
ADD A,@Ri	Add indirect RAM to accumulator	1	1
ADD A,#data	Add immediate data to accumulator	2	1
ADDC A,Rn	Add register to accumulator with carry flag	1	1
ADDC A,direct	Add direct byte to A with carry flag	2	1
ADDC A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC A,#data	Add immediate data to A with carry flag	2	1
SUBB A,Rn	Subtract register from A with borrow	1	1
SUBB A,direct	Subtract direct byte from A with borrow	2	1
SUBB A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB A,#data	Subtract immediate data from A with borrow	2	1
INC A	Increment accumulator	1	1
INC Rn	Increment register	1	1
INC direct	Increment direct byte	2	1
INC @ Ri	Increment indirect RAM	1	1
DEC A	Decrement accumulator	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	1
DEC @Ri	Decrement indirect RAM	1	1
INC DPTR	Increment data pointer	1	2
MUL A,B	Multiply A and B	1	4
DIV A,B	Divide A by B	1	4
DA A	Decimal adjust accumulator	1	1

Table 54. Logic Operations

Mnemonic	Description	Byte	Cycle
ANL A,Rn	AND register to accumulator	1	1
ANL A,direct	AND direct byte to accumulator	2	1
ANL A,@Ri	AND indirect RAM to accumulator	1	1
ANL A,#data	AND immediate data to accumulator	2	1
ANL direct,A	AND accumulator to direct byte	2	1
ANL direct,#data	AND immediate data to direct byte	3	2
ORL A,Rn	OR register to accumulator	1	1
ORL A,direct	OR direct byte to accumulator	2	1
ORL A,@Ri	OR indirect RAM to accumulator	1	1
ORL A,#data	OR immediate data to accumulator	2	1
ORL direct,A	OR accumulator to direct byte	2	1
ORL direct,#data	OR immediate data to direct byte	3	2
XRL A,Rn	Exclusive OR register to accumulator	1	1
XRL A,direct	Exclusive OR direct byte to accumulator	2	1
XRL A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL A,#data	Exclusive OR immediate data to accumulator	2	1
XRL direct,A	Exclusive OR accumulator to direct byte	2	1
XRL direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR A	Clear accumulator	1	1
CPL A	Complement accumulator	1	1
RL A	Rotate accumulator left	1	1
RLC A	Rotate accumulator left through carry	1	1
RR A	Rotate accumulator right	1	1
RRC A	Rotate accumulator right through carry	1	1
SWAP A	Swap nibbles within the accumulator	1	1

Table 55. Data Transfer

Mnemonic	Description	Byte	Cycle
MOV A,Rn	Move register to accumulator	1	1
MOV A,direct	Move direct byte to accumulator	2	1
MOV A,@Ri	Move indirect RAM to accumulator	1	1
MOV A,#data	Move immediate data to accumulator	2	1
MOV Rn,A	Move accumulator to register	1	1
MOV Rn,direct	Move direct byte to register	2	2
MOV Rn,#data	Move immediate data to register	2	1
MOV direct,A	Move accumulator to direct byte	2	1
MOV direct,Rn	Move register to direct byte	2	2
MOV direct,direct	Move direct byte to direct byte	3	2
MOV direct,@Ri	Move indirect RAM to direct byte	2	2
MOV direct,#data	Move immediate data to direct byte	3	2
MOV @Ri,A	Move accumulator to indirect RAM	1	1
MOV @Ri,direct	Move direct byte to indirect RAM	2	2
MOV @ Ri, #data	Move immediate data to indirect RAM	2	1
MOV DPTR, #data16	Load data pointer with a 16-bit constant	3	2
MOVC A,@A + DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC A,@A + PC	Move code byte relative to PC to accumulator	1	2
MOVX A,@Ri	Move external RAM (8-bit address) to A	1	2
MOVX A,@DPTR	Move external RAM (16-bit address) to A	1	2
MOVX @Ri,A	Move A to external RAM (8-bit address)	1	2
MOVX @DPTR,A	Move A to external RAM (16-bit address)	1	2
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A,Rn	Exchange register with accumulator	1	1
XCH A,direct	Exchange direct byte with accumulator	2	1
XCH A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD X,@ Ri	Exchange low-order nibble indirect RAM with A	1	1

Table 56. Boolean Manipulation

Mnemonic	Description	Byte	Cycle
CLR C	Clear carry flag	1	1
CLR bit	Clear direct bit	2	1
SETB C	Set carry flag	1	1
SETB bit	Set direct bit	2	1
CPL C	Complement carry flag	1	1
CPL bit	Complement direct bit	2	1
ANL C,bit	AND direct bit to carry flag	2	2
ANL C,bit	AND complement of direct bit to carry	2	2
ORL C,bit	OR direct bit to carry flag	2	2
ORL C,bit	OR complement of direct bit to carry	2	2
MOV C,bit	Move direct bit to carry flag	2	1
MOV bit,C	Move carry flag to direct bit	2	2

Table 57. Program Branches

Mnemonic	Description	Byte	Cycle
ACALL addr11	Absolute subroutine call	2	2
LCALL addr16	Long subroutine call	3	2
RET Return	From subroutine	1	2
RETI Return	From interrupt	1	2
AJMP addr11	Absolute jump	2	2
LJMP addr16	Long jump	3	2
SJMP rel	Short jump (relative address)	2	2
JMP @A + DPTR	Jump indirect relative to the DPTR	1	2
JZ rel	Jump if accumulator is zero	2	2
JNZ rel	Jump if accumulator is not zero	2	2
JC rel	Jump if carry flag is set	2	2
JNC rel	Jump if carry flag is not set	2	2
JB bit,rel	Jump if direct bit is set	3	2
JNB bit,rel	Jump if direct bit is not set	3	2
JBC bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE A,#data,rel	Compare immediate to A and jump if not equal	3	2
CJNE Rn,#data rel	Compare immediate to register and jump if not equal	3	2
CJNE @Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	2
DJNZ Rn,rel	Decrement register and jump if not zero	2	2
DJNZ direct,rel	Decrement direct byte and jump if not zero	3	2
NOP	No operation	1	1

8. Innovasic/Intel Part Number Cross-Reference Tables

Tables 58 and 59 cross-reference each Innovasic part number with the corresponding Intel part number for the PDIP and PLCC, respectively.

Table 58. Innovasic/Intel Part Number Cross-Reference for the PDIP

Innovasic Part Number	Intel Part Number	Package Type	Temperature Grades
IA8X44PDW40IR3 lead-free (RoHS)	P8344 P8344AH TP8344AH P8044 P8044AH P8044AH-R0117 TP8044AH TP8044AH-R0117	40-Pin Plastic Dual In-Line Package (PDIP) (600 mils)	Industrial
IA8X44PDW40I3 lead frame (SnPb)			

Table 59. Innovasic/Intel Part Number Cross-Reference for the PLCC

Innovasic Part Number	Intel Part Number	Package Type	Temperature Grades
IA8X44-PLC44I-R-P03 lead-free (RoHS)	N8344 N8344AH TN8344AH N8044 N8044AH N8044AH-R0117 TN8044AH TN8044AH-R0117 8044AHN 8044AN	44-Pin Plastic Leaded Chip Carrier (PLCC)	Industrial
IA8X44PLC44I3 lead frame (SnPb)			

9. Errata

9.1 Summary

Table 60 presents a summary of errata in the IA8044/IA8344 controller.

Table 60. Summary of Errata

Errata No.	Problem	Ver. 3
1	Cannot read internal ROM with EPROM verification method.	Exists
2	The device has a different pullup value than the Intel version.	Exists
3	The device responds to an idle flag one bit time too early.	Exists
4	Under certain conditions the SIU will overwrite the RCB register when starting a transmission.	Exists

9.2 Detail

Errata No. 1

Problem: Cannot read internal ROM with EPROM verification method.

Description: The IA8044/IA8344 does not contain internal EPROM and therefore does not support the EPROM read feature.

Workaround: Must use alternate method to read internal ROM.

Errata No. 2

Problem: The device has a different pullup value than the Intel version.

Description: The Intel version can source more current than the IA8044/IA8344.

Workaround: Adjust external circuits if necessary.

Errata No. 3

Problem: The device responds to an idle flag one bit time too early.

Description: This causes problems in a loop-mode network. It only occurs in loop mode when using an external SIU clock source and idle flags.

Workaround: None.

Errata No. 4

Problem: Under certain conditions the SIU will overwrite the RCB register when starting a transmission.

Description: The conditions are:

- The SIU is externally clocked.
- The SIU is in flexible mode.
- The CPU has not already read the RCB from a previous reception before the transmission takes place.

Workaround: Read the RCB before initiating a transmit.

10. Revision History

Table 61 presents the sequence of revisions to document IA211010112.

Table 61. Revision History

Date	Revision	Description	Page(s)
January 20, 2006	01	First edition released.	NA
August 28, 2007	02	Updated RoHS info, header, footer, cover page. Errata added.	All
January 2, 2009	03	Reformatted and reorganized to meet publication standards. Technical data updated. "Summary of Errata" table added.	All
March 30, 2010	04	Updated Innovasic part numbers on Cross Reference Table to reflect current part marking scheme. (Part is still Version 3 release.)	61

11. For Additional Information

The Innovasic Semiconductor IA8044 and IA8344 are "plug-and-play" drop-in replacements and are form, fit, and function compatible parts to the Intel® 8044 and 8344. The IA8044 and IA8344 replace the obsolete Intel 8044 and 8344, allowing users to retain existing board designs, software compilers/assemblers, and emulation tools—thus avoiding expensive redesign efforts.

The Innovasic Support Team is continually planning and creating tools for your use. Visit http://www.Innovasic.com for up-to-date documentation and software. Our goal is to provide timely, complete, accurate, useful, and easy-to-understand information. Please feel free to contact our experts at Innovasic at any time with suggestions, comments, or questions.

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