



# 5 mm x 7 mm Ceramic Package SMD VCXO, LVCMOS / LVPECL / LVDS I630 - Series

## Product Features

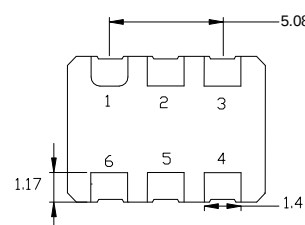
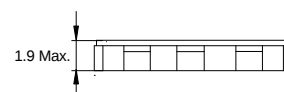
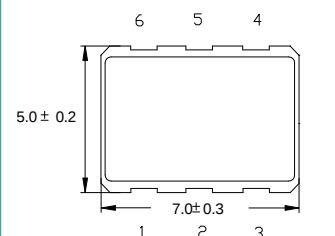
Small Surface Mount Package  
Fast Sample Delivery  
Frequencies to 1500 MHz  
Pb Free/ RoHS Compliant  
Leadfree Processing

## Applications

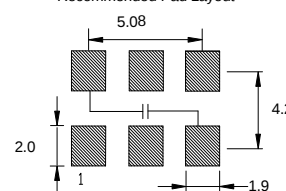
xDSL  
Broadcast video  
Wireless Base Stations  
Sonet /SDH  
WiMAX/WLAN  
Server and Storage

Ethernet/LAN/WAN  
Optical modules  
Clock and data recovery  
FPGA/ASIC  
Backplanes  
GPON

|                                                     |                                                                                                                                       |
|-----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|
| <b>Frequency</b><br>LVCMOS<br>LVPECL<br>LVDS        | 10 MHz to 225 MHz<br>10 MHz to 1500 MHz<br>10 MHz to 1500 MHz                                                                         |
| <b>Output Level</b><br>LVCMOS<br>LVPECL<br>LVDS     | VOH=90% VDD min., VOL=10 % VDD max.<br>VOH=VDD-1.03V max. (Nom. Load), VOL=VDD-1.6V max. (Nom. Load)<br>VOD=(Diff. Output) 350mV Typ. |
| <b>Duty Cycle</b><br>LVCMOS<br>LVPECL<br>LVDS       | 50% ±5% @ 50%VDD<br>50% ±5% @ 50%*<br>50% ±5% @ 50%*                                                                                  |
| <b>Rise / Fall Time</b><br>LVCMOS<br>LVPECL<br>LVDS | 3.0 ns max. (90%/10%)*<br>0.6 ns max. (80%/20%)*<br>0.6 ns max. (80%/20%)*                                                            |
| <b>Output Load</b><br>LVCMOS<br>LVPECL<br>LVDS      | 15pF<br>50 Ω to VDD - 2.0 VDC<br>RL=100 Ω/CL=10pF                                                                                     |
| <b>Frequency Stability</b>                          | See Table Below                                                                                                                       |
| <b>Supply Voltage</b>                               | 3.3 VDC ± 10%, 2.5 VDC ± 5%                                                                                                           |
| <b>Current</b>                                      | LVCMOS = 25 mA max., LVPECL = 60 mA max. LVDS = 35 mA max.                                                                            |
| <b>Linearity</b>                                    | 10% max.                                                                                                                              |
| <b>Pullability</b>                                  | See Table Below                                                                                                                       |
| <b>Control Voltage</b>                              | 1.65 VDC ± 1.65 VDC @ 3.3V<br>1.25 VDC ± 1.25 VDC @ 2.5V                                                                              |
| <b>Input Impedance</b>                              | 50K Ω min.                                                                                                                            |
| <b>Phase Jitter (RMS)<br/>At 12kHz to 20 MHz</b>    | 0.9 ps typical                                                                                                                        |
| <b>Operating Temp.<br/>Range</b>                    | See Table Below                                                                                                                       |
| <b>Storage</b>                                      | -40° C to +100° C                                                                                                                     |



Recommended Pad Layout



| Pin | Connection            |
|-----|-----------------------|
| 1   | Voltage Control       |
| 2   | Enable/Disable or N/C |
| 3   | GND                   |
| 4   | Output                |
| 5   | Output or N/C         |
| 6   | VDD                   |

Dimension Units: mm

| Part Number Guide |               | Sample Part Number: I630-31AB9H2-155.520 |                    |             |            |                          |                                 |              |
|-------------------|---------------|------------------------------------------|--------------------|-------------|------------|--------------------------|---------------------------------|--------------|
| Package           | Input Voltage | Operating Temperature                    | Stability (in ppm) | Pullability | Output     | Enable / Disable (Pin 2) | Complimentary Output (Pin 5) ** | Frequency    |
| I630              | 3 = 3.3V      | 1 = 0° C to +70° C                       | F = ±20            | B = ± 50    | 3 = LVCMOS | K = Enable               | 1 = N.C.                        | -155.520 MHz |
|                   | 6 = 2.5V      | 3 = -20° C to +70° C                     | A = ±25            | C = ±100    | 8 = LVDS   | O = N/C                  | 2 = Output                      |              |
|                   |               | 2 = -40° C to +85° C                     | B = ±50            |             | 9 = LVPECL |                          |                                 |              |

NOTE: A 0.01 µF bypass capacitor is recommended between VDD (pin 6) and GND (pin 3) to minimize power supply noise. \* Measured as percent of waveform. \*\* Available on LVDS and LVPECL output only.

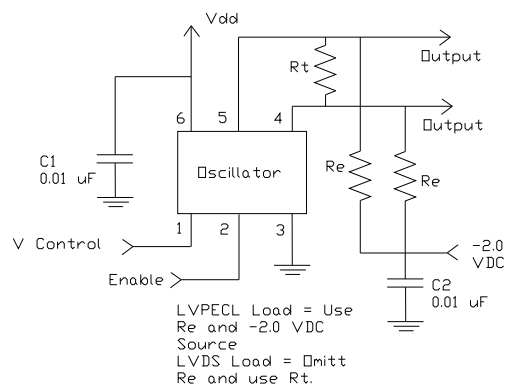
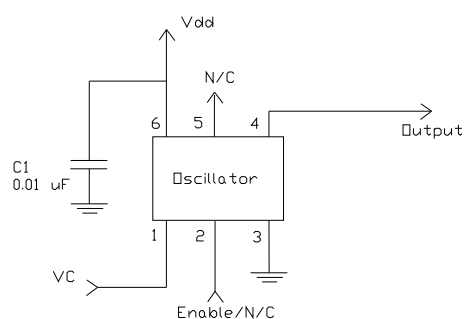


5 mm x 7 mm Ceramic Package SMD VCXO, LVCMOS / LVPECL / LVDS 1630 - Series

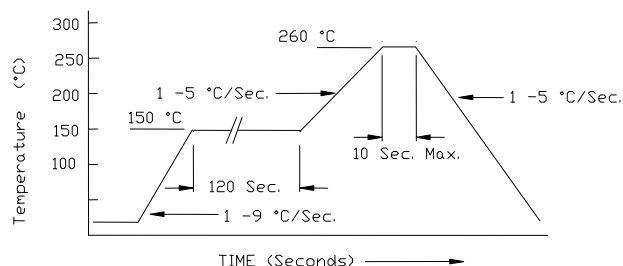
## SSB Phase Noise (typ.)

| Offset | 77.76 MHz   | 155.52 MHz  | 622.08 MHz  |
|--------|-------------|-------------|-------------|
| 10Hz   | -75 dBc/Hz  | -62 dBc/Hz  | -47 dBc/Hz  |
| 100Hz  | -105 dBc/Hz | -101 dBc/Hz | -79 dBc/Hz  |
| 1kHz   | -117 dBc/Hz | -112 dBc/Hz | -100 dBc/Hz |
| 10kHz  | -123 dBc/Hz | -115 dBc/Hz | -104 dBc/Hz |
| 100kHz | -125 dBc/Hz | -118 dBc/Hz | -106 dBc/Hz |

## Typical Application:



## Pb Free Solder Reflow Profile:



\*Units are backward compatible with 240C reflow processes

## Package Information:

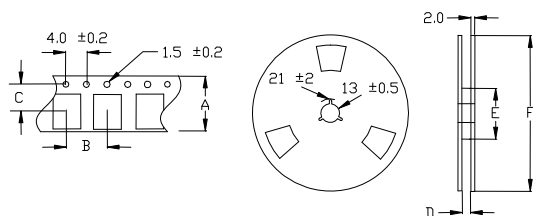
MSL = N.A. (package does not contain plastic, storage life is unlimited under normal room conditions).

Termination = e4 (Au over Ni over W base metalization).



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## Tape and Reel Information:



| Quantity per Reel | 1000         |
|-------------------|--------------|
| A                 | 16 +/- .3    |
| B                 | 8 +/- .2     |
| C                 | 7.5 +/- .2   |
| D                 | 17.5 +/- 1   |
| E                 | 50 / 60 / 80 |
| F                 | 180 / 250    |

## Environmental Specifications

|                              |                                                                        |
|------------------------------|------------------------------------------------------------------------|
| Thermal Shock                | MIL-STD-883, Method 1011, Condition A                                  |
| Moisture Resistance          | MIL-STD-883, Method 1004                                               |
| Mechanical Shock             | MIL-STD-883, Method 2002, Condition B                                  |
| Mechanical Vibration         | MIL-STD-883, Method 2007, Condition A                                  |
| Resistance to Soldering Heat | J-STD-020C, Table 5-2 Pb-free devices (except 2 cycles max)            |
| Hazardous Substance          | Pb-Free / RoHS / Green Compliant                                       |
| Solderability                | JESD22-B102-D Method 2 (Preconditioning E)                             |
| Terminal Strength            | MIL-STD-883, Method 2004, Test Condition D                             |
| Gross Leak                   | MIL-STD-883, Method 1014, Condition C                                  |
| Fine Leak                    | MIL-STD-883, Method 1014, Condition A2, R1=2x10 <sup>-8</sup> atm cc/s |
| Solvent Resistance           | MIL-STD-202, Method 215                                                |

## Marking

Line 1: ILSI and Date Code (YWW)

Line 2: Frequency