# Xilinx Parallel Cable IV

DS097 (v3.0) January 21, 2016 **Product Specification**

## Features

- Download speed of up to 5 Megabits per second (Mb/s)
- Over eight times faster than Xilinx Parallel Cable III using Xilinx ISE® iMPACT download software
- Embedded Development Kit (EDK) compatible
- ChipScope™ Pro Analyzer compatible
- In-system configures the following Xilinx devices:
  - Virtex® series FPGAs
  - Spartan® series FPGAs
  - XC9500/XC9500XL/XC9500XV CPLDs
  - CoolRunner™ (XPLA3)/CoolRunner-II CPLDs
  - XC18V00 ISP PROMs
  - XC4000 series FPGAs
  - Platform Flash XCF00S/XCF00P/XL PROMs
- LED status indicator
- Automatically senses and adapts to correct I/O voltage
- Interfaces to devices operating at 5V (TTL), 3.3V (LVTTL), 2.5V, 1.8V, and 1.5V
- In-system programs serial-access flash PROMs via the serial peripheral interface (SPI)
- Supports IEEE 1149.1 (JTAG), Xilinx slave-serial mode, and serial peripheral interface (SPI)
- J-Drive IEEE 1532 Programming Engine compatible
- Includes high-performance ribbon cable
- Compliant with IEEE 1284 Level 2 Electrical Specification
- Externally powered using keyboard/mouse splitter cable or AC power brick
- Compatible with ECP-compliant I/O controllers for high-speed, bidirectional communication
- Intended for development — not recommended for production programming

## Parallel Cable IV Description

The Xilinx Parallel Cable IV (PC4) (Figure 1) is a high-speed download cable that configures or programs all Xilinx FPGA, CPLD, and ISP PROM devices. The cable takes advantage of the IEEE 1284 ECP protocol and Xilinx iMPACT software to increase download speeds over eight times faster than existing solutions. The cable automatically senses and adapts to target I/O voltages and is able to accommodate a wide range of I/O standards from 1.5V to 5V. PC4 is designed for use in a desktop environment.

***Note:*** Xilinx also offers the Platform Cable USB II with a USB 2.0 interface to the host PC and similar capabilities as the Parallel Cable IV. See DS593, *Platform Cable USB II*, for details.

PC4 supports the widely used industry-standard IEEE 1149.1 boundary-scan (JTAG) specification, the Xilinx slave-serial mode for Xilinx FPGA devices, and serial peripheral interface for serial-access flash PROM programming. PC4 supports indirect programming of select flash memories including the Platform Flash XL configuration and storage device (via an FPGA JTAG port). The cable interfaces to target systems using a ribbon cable that features integral alternating ground leads to reduce crosstalk and improve signal integrity.

The cable is externally powered from either a power *brick* or by interfacing to a standard PC mouse or keyboard connection. A bi-color status LED indicates the presence of operating and target reference voltages.




*Figure 1:* **Xilinx Parallel Cable IV**

© 2001–2008, 2016 Xilinx, Inc. All rights reserved. XILINX, the Xilinx logo, Virtex, Spartan, ISE and other designated brands included herein are trademarks of Xilinx in the United States and other countries. All other trademarks are the property of their respective owners.

## Connecting to Host Computer

The PC4 connects to any PC using Microsoft® Windows® 2000, Windows XP, or Linux(1) operating systems through the built-in, standard IEEE 1284 DB25 parallel (printer) port connector.(2) To fully utilize the higher speeds of this cable, the host PC must have a parallel port that is enabled to support extended capability port (ECP) mode.(3)

If ECP mode is not enabled, the PC4 defaults to compatibility mode and does not run at the optimum speeds listed.

**Notes:**

1. See the System Requirements section in the ISE software manual for more specific operating system requirements.
2. Xilinx makes no representations about compatibility with third-party IEEE 1284 add-on adapters and does not support the add-on adapters.
3. Refer to host PC BIOS to see if ECP mode is enabled.

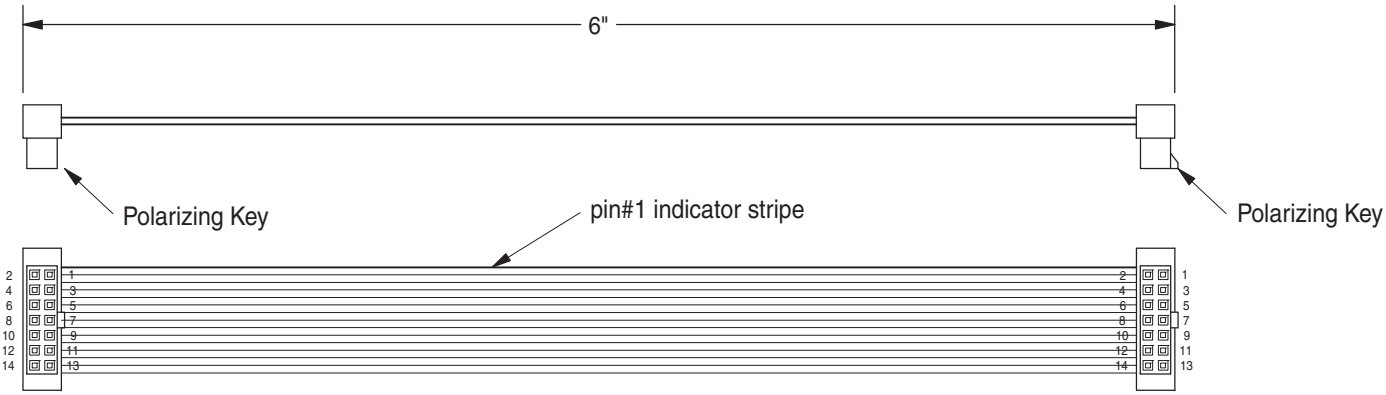
## High Performance Ribbon Cable

An insulation displacement connector (IDC) ribbon cable is supplied and recommended for connection to target systems. See Figure 2 and Figure 3. This cable incorporates multiple signal-ground pairs and facilitates error-free connection. A very small footprint, keyed mating connector is all that is required on the target system. Refer to Figure 4 for the appropriate connector pin assignments and sample vendor part numbers. Figure 5 shows the POD and its dimensions.

The Parallel Cable IV can also interface to target systems using *flying lead* wires. However, these are not included with PC4. The flying lead wires and additional ribbon cables can be purchased separately from the Xilinx Online Store.




*Figure 2:* **High Performance Ribbon Cable**

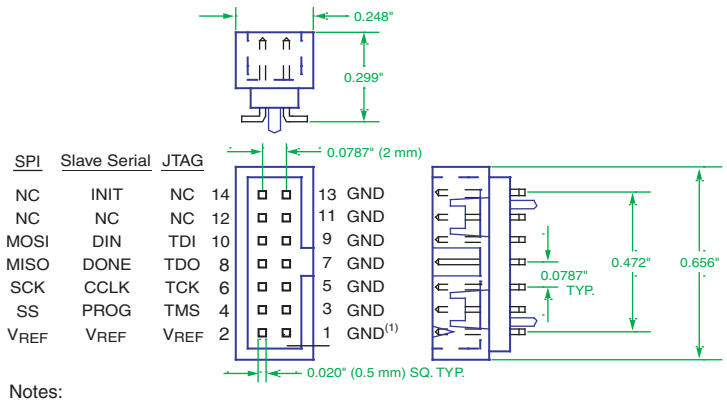



**Notes:**

1. Ribbon Cable - 14 conductor, 1.0 mm centers Round Conductor Flat Cable, 28AWG (7 x 36) stranded copper conductors; gray PVC with pin #1 edge marked.
2. 2 mm Ribbon, Female Polarized Connectors - IDC connection to ribbon, contacts are beryllium copper plated with 30 micro inches gold plating over 50 micro inches nickel, connectors mate to 0.5 mm square posts on 2 mm centers.

ds097_03_050508

*Figure 3:* **Ribbon Cable Diagram**




Notes:

1. Pin 1 is not a true digital ground. It must be connected to digital ground at the target system. See pin assignment descriptions (Table 2) for more information.
2. Connecter is a 2 x 7 (14 position) 2 mm surface-mount version for ribbon cable, Molex part no. 87832-1420, also available in through-hole mounting.

DS097_04_102106

*Figure 4:* **Target Interface Connector Signal Assignments**

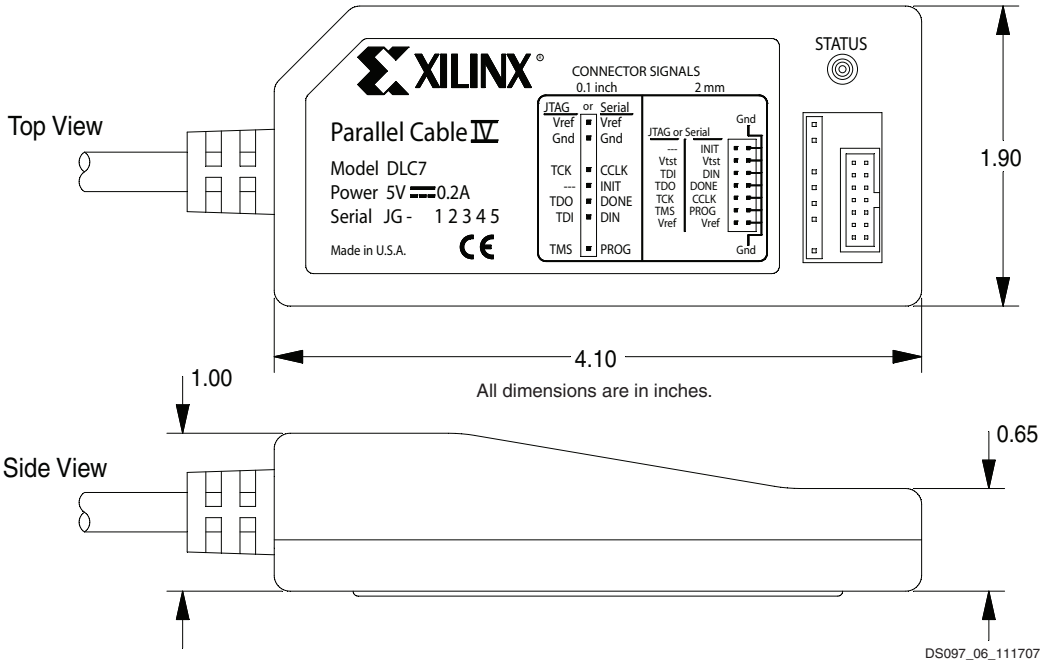



*Figure 5:* **Diagram of POD with Dimensions**

Table 1 provides some third-party sources for mating connectors that are compatible with the Parallel Cable IV ribbon cable.

*Table 1:* **Mating Connectors for 2-mm Pitch, 14-Conductor Ribbon Cable**

| Manufacturer(1) | SMT, Vertical | SMT, Right Angle | Through-Hole, Vertical | Through-Hole, Right Angle | Web Site |
|---|---|---|---|---|---|
| Molex | 87832-1420 | N/A | 87831-1420 | 87833-1420 | www.molex.com |
| FCI | 98424-G52-14 | N/A | 98414-G06-14 | 98464-G61-14 | www.fciconnect.com |
| Comm Con Connectors | 2475-14G2 | N/A | 2422-14G2 | N/A | www.commcon.com |

**Notes:**

1. Some manufacturer pin assignments may not conform to Xilinx pin assignments. Please refer to the manufacturer's data sheet for more information.
2. Additional ribbon cables can be purchased separately from the Xilinx Online Store.

## Pinout Assignments

*Table 2:* **PC4 Target Interface Connector Signal Assignments**

| Pin Name(1) | | | Type | Flying Lead Wires | Ribbon Cable | Description |
|---|---|---|---|---|---|---|
| JTAG | Slave Serial | SPI | | | | |
| TDI | – | – | Out | 2 | 10 | **Test Data In**. This is the target serial input data stream for JTAG operations and should be connected to the TDI pin on the first ISP device in the JTAG chain. |
| TDO | – | – | In | 3 | 8 | **Test Data Out**. This is the target serial output data stream for JTAG operations and should be connected to the TDO pin on the last ISP device in the JTAG chain. |
| TCK | – | – | Out | 5 | 6 | **Test Clock**. This is the clock signal for JTAG operations and should be connected to the TCK pin on all target ISP devices that share the same data stream. |
| TMS | – | – | Out | 1 | 4 | **Test Mode Select**. This is the JTAG mode signal that establishes appropriate TAP state transitions for target ISP devices. It should be connected to the TMS pin on all target ISP devices that share the same data stream. |
| – | INIT | – | In/Out | 4 | 14 | **Configuration Initialize**. This pin indicates that configuration memory is being cleared. It should be connected to the INIT_B pin of the target FPGA in a single device system or to the INIT_B pin on all FPGAs in daisy-chained configurations. |
| – | DIN | – | Out | 2 | 10 | **Configuration Data Input**. This is the serial input data stream for target FPGA(s). It should be connected to the DIN pin of the target FPGA in a single device system or to the DIN pin of the first FPGA in daisy-chained configurations. |
| – | DONE | – | In | 3 | 8 | **Configuration Done**. This pin indicates to PC4 that the target FPGA(s) have received the entire configuration bit stream. It should be connected to the DONE pin on all FPGAs for daisy-chained configurations. Additional CCLK cycles are issued following the positive transition of DONE to ensure that the configuration process is complete. |
| – | CCLK | – | Out | 5 | 6 | **Configuration Clock**. In slave-serial configuration mode, FPGAs are configured by loading one bit per CCLK cycle. CCLK should be connected to the CCLK pin on the target FPGA for a single device system or to the CCLK pin of all FPGAs in daisy-chained configurations. |
| – | PROG | – | Out | 1 | 4 | **Configuration Reset**. This pin is used to force a reconfiguration of the target FPGA(s). It should be connected to the PROG_B pin of the target FPGA in a single device system or to the PROG_B pin of all FPGAs in daisy-chained configurations. |
| – | – | MOSI | Out | 2 | 10 | **SPI Master-Output Slave-Input.** This pin is the target serial input data stream for SPI operations and should be connected to the D(2) pin on the SPI flash PROM. |
| – | – | MISO | In | 3 | 8 | **SPI Master-Input, Slave-Output.** This pin is the target serial output data stream for SPI operations and should be connected to the Q(2) pin on the SPI flash PROM. |
| – | – | SCK | Out | 5 | 6 | **SPI Clock.** This pin is the clock signal for SPI operations and should be connected to the C(2) pin on the SPI flash PROM. |
| – | – | SS | Out | 1 | 4 | **SPI Select.** This pin is the active-Low SPI chip select signal. This should be connected to the S(2) pin on the SPI flash PROM. |
| $V_{TST}$ | $V_{TST}$ | $V_{TST}$ | Out | | 12 | **Test Driver**. This pin is reserved for Xilinx diagnostics and should not be connected to any target circuitry. |

*Table 2:* **PC4 Target Interface Connector Signal Assignments *(Cont'd)***

| Pin Name(1) | | | Type | Flying Lead Wires | Ribbon Cable | Description |
|---|---|---|---|---|---|---|
| JTAG | Slave Serial | SPI | | | | |
| $V_{REF}$ | $V_{REF}$ | $V_{REF}$ | In | 7 | 2 | **Target Reference Voltage**. This pin should be connected to a voltage bus on the target system that supplies the SPI, JTAG or slave serial interface. For example, when communicating with CoolRunner II device using the JTAG interface, $V_{REF}$ should be connected to the target $V_{AUX}$ bus. $V_{REF}$ must be connected to a regulated voltage. There must not be any current limiting resistor. |
| GND | GND | GND | – | 6 | 1(3), 3, 5, 7, 9, 11, 13 | **Digital Ground**. Xilinx recommends that all odd-numbered pins on the ribbon cable connector (pins 1(1), 3, 5, 7, 9, 11, and 13) be connected to digital ground. Minimum crosstalk is achieved when using all grounds. |

**Notes:**

1. Pins not listed are no connects.
2. The listed SPI pin names match those of SPI flash memories from STMicroelectronics. Pin names of compatible SPI devices from other vendors can be different. Consult the vendor's SPI device data sheet for corresponding pin names.

   ***Caution!*** The PROG_B pin of the FPGA, which is connected to a target SPI device, must be asserted Low during SPI programming to ensure the FPGA does not contend with the SPI programming operation.
3. Pin 1 must not be isolated from the target system digital ground for use as a cable attachment identifier. Pin 1 is a virtual ground used for diagnostic purposes. This virtual ground is biased through a resistor network. For normal operation, Pin 1 must be connected to the target system digital ground.

   ***Caution!*** Pin 1 must not be the only digital ground pin attached to the target system digital ground plane.

## TDO/MISO Timing Specifications

When using JTAG or SPI configuration mode, target systems must guarantee that TDO/MISO signal assertion meets a minimum setup time relative to the positive edge of TCK/SCK. Buffers or multiplexers in the target hardware can add phase delays as long as the following setup specification is not violated. Figure 6 illustrates the relationship between TCK/SCK and TDO/MISO_internal for the 5 MHz default PC4 configuration speed.

TDO/MISO_internal is the propagation delayed version of the TDO/MISO signal generated by the target device (accounting for any target system buffers, multiplexers, and distributed capacitance).

All PC4 output signal transitions and input signal latching events are synchronized to an internal 40 MHz system clock. In JTAG mode, TDO is asserted by the last device in the target JTAG chain on the negative edge of TCK (1 in Figure 6). In SPI mode, MISO is asserted by the SPI device on the negative edge of SCK (1 in Figure 6). Setup and hold times for TDO/MISO_internal are referenced to the next positive edge of TCK/SCK (2 in Figure 6).

When the PC4 is operating at the maximum clock frequency of 5 MHz, the TDO/MISO_internal is sampled 12.5 ns (4 in Figure 6) prior to each negative edge of TCK/SCK. Setup time ($T_{DOS}$, 3 in Figure 6) is specified relative to the positive edge of TCK/SCK (2 in Figure 6).

When the PC4 configuration clock rate is changed to a lower frequency, there is additional margin for propagation delay through target buffers. Any design that complies with the margins specified for 5 MHz operation is guaranteed to operate at lower frequencies.

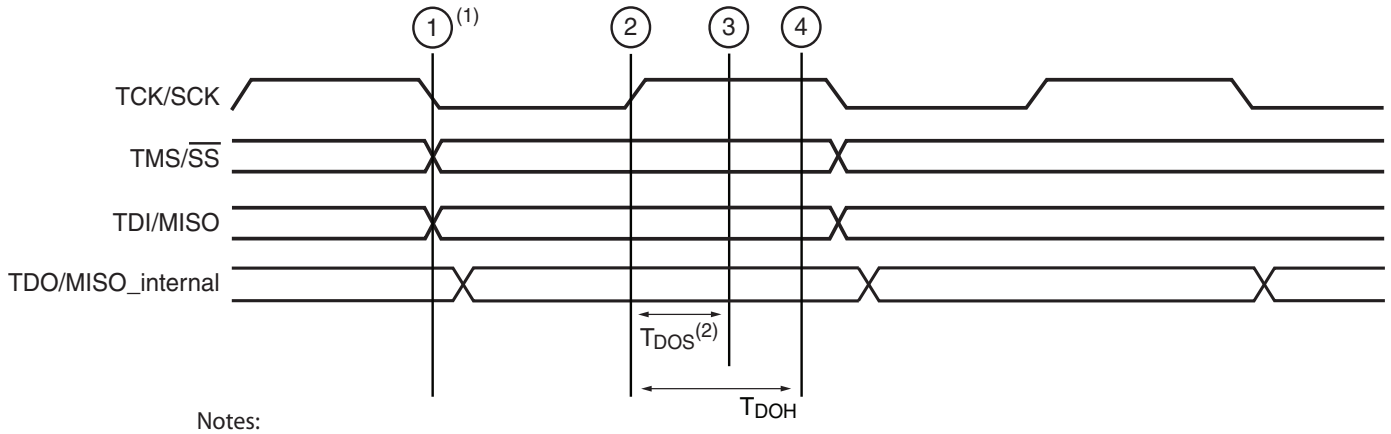



*Figure 6:* **TDO/MISO Timing Diagram**

*Table 3:* **TDO/MISO Timing Specifications**

| Selected Frequency | Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|---|
| 5 MHz | $T_{DOS}$ | TDO/MISO setup time | –42 | – | ns |
| | $T_{DOH}$ | TDO/MISO hold time | 88 | – | ns |
| 200 kHz | $T_{DOS}$ | TDO/MISO setup time | –2442 | – | ns |
| | $T_{DOH}$ | TDO/MISO hold time | 2488 | – | ns |

## Cable Power

The host interface cable (Figure 8) includes a short power jack for connection to one of two possible +5V DC power sources: (1) the keyboard or mouse part of the host PC or (2) an external AC adapter. The supplied power splitter cable is required when using the first option. The splitter cable is installed between the mouse cable and the standard 6-pin mini-DIN connector on the host PC.

PC4 operating current is less than 100 mA. It draws approximately 15 mA from the target reference voltage bus to power the SPI/JTAG/Slave Serial buffers.

Figure 7 shows a PC4 cable connection to a laptop.

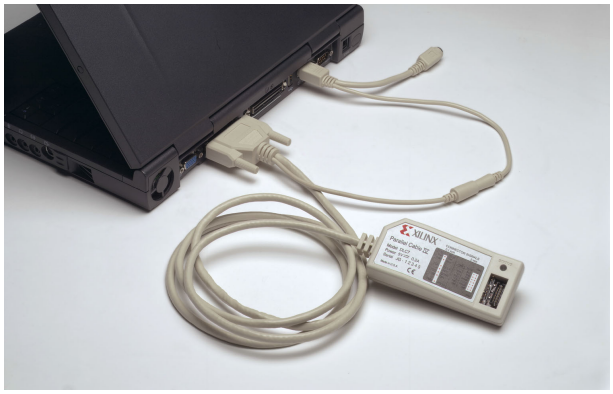


*Figure 7:* **Laptop PC4 Cable Connection**

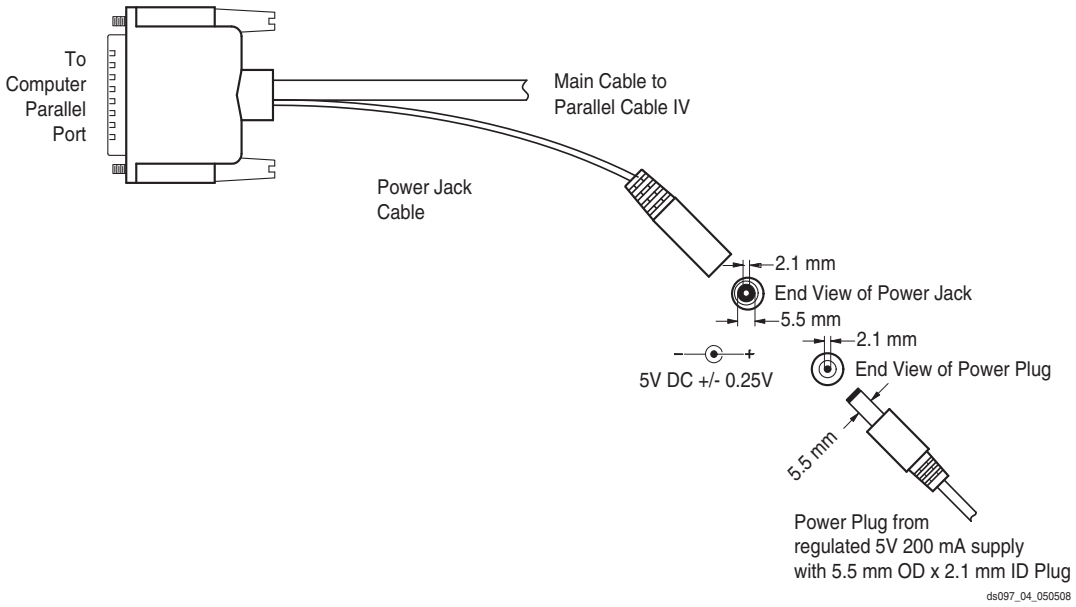



*Figure 8:* **Optional Power Brick Connection to Parallel Cable IV**

## Power Supply Sources

Table 4 provides some third-party sources for power supplies that are compatible with the Parallel Cable IV.

*Table 4:* **Power Supply Sources**(1, 2)

| Part Number | Description | Manufacturer | URL | Distributor | URL |
|---|---|---|---|---|---|
| DTS050400UC-P5P-KH(3) | 5V, 12W, 3 Prong Inlet | CUI Stack | www.cuistack.com | DigiKey | www.digikey.com |
| DTS050250SUDC-P5P | 5V, 12W, 2 Prong Inlet | CUI Stack | www.cuistack.com | DigiKey | www.digikey.com |
| FW1805-S760(3) | 5V, 15W, 3 Prong Inlet | Elpac | www.elpac.com | – | – |

**Notes:**

1. The external power supply must provide a regulated +5.0V DC @ 200 mA minimum.
2. The PC4 pigtail connector only mates with a power supply that uses a 2.1 mm plug on its DC output cable.
3. The three-prong Inlet power supplies are recommended for international use so that a variety of AC plug styles can be accommodated with a single power supply.

## Status LED

The Status LED indicates one of two possible conditions as shown in the following table.

| LED State | Operating Condition |
|---|---|
| Solid Green | Power available to POD and $V_{REF}$ detected. |
| Solid Amber | Power available to POD but no $V_{REF}$ detected. |

**Notes:**

1. If LED does not turn on, check to make sure that power has been connected to the PC4 either through the mouse/keyboard port or through the external power connector.

## Automatic I/O Voltage Sensing

Although JTAG configuration pins have typically operated at 3.3V or 5.0V, new devices support voltages as low as 1.5V. Voltage levels for Slave-Serial configuration pins follow the respective I/O bank voltage, which can be in the range from 1.5V to 5.0V. SPI pin voltage levels are the same as the SPI device power supply voltage which is typically 3.3V or 2.5V. Consequently, the PC4 output buffers must be capable of driving at the voltage level expected by the receiving devices. The $V_{REF}$ pin on the target device is used to bias the PC4 output buffers.

A sensing circuit continuously monitors the $V_{REF}$ pin. If $V_{REF}$ drops below 1.3V DC, all output buffers are 3-stated to avoid any possible damage when connected to a non-powered target system.

All pins are protected against continuous shorts to ground or voltages up to 5.5V DC.

## IEEE 1284 Cable Specifications

Level 1 compliant host ports are designed to operate over a maximum cable length of 10 ft. Level 2 compliant host ports operates over a maximum cable length of 33 ft. PC4 uses a Level 2 compliant cable interface buffer.

For more cable information, see the following web site:

www.xilinx.com/products/design_resources/config_sol/

## Signal Integrity Issues

The PC4 uses high slew rate buffers to drive TCK, TMS, and TDI. Users should pay close attention to proper PCB layout and signal termination to avoid transmission line effects. Users are encouraged to refer to the Xilinx "Signal Integrity" documentation and the application note XAPP361, *Planning for High Speed XC9500XV Designs*, on the Xilinx web site.

## PC4 Operating Characteristics

### Absolute Maximum Ratings

| Symbol | Description | Value | Units |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 5.5 | V |
| $T_A$ | Operating Temperature Range | 0° to +70° | C |
| $T_{STG}$ | Storage Temperature Range | –40° to +85° | C |
| $P_D$ | Power Dissipation | 750 | mW |
| $I_{OUT}$ | DC Output Current (TDI, TCK, TMS, INIT) | ±32 | mA |

### Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | External P/S | 4.75 | 5.25 | V |
| $V_{REF}$ | Target Reference Voltage | | 1.5 | 5.5 | V |
| $I_{CC}$ | Operating Current | | 60 | 100 | mA |
| $I_{REF}$ | Reference Current | | 6.0 | 15.0 | mA |
| $V_{OH}$ | High Level Output Voltage | $V_{REF}$ = 3.3V DC, $I_{OH}$ = –4 mA | 2.7 | – | V |
| $V_{OL}$ | Low Level Output Voltage | $V_{REF}$ = 3.3V DC, $I_{OL}$ = +4 mA | – | 0.36 | V |
| $V_{IH}$ | High Level Input Voltage | $V_{REF}$ > 1.5V | 1.2 | – | V |
| $V_{IL}$ | Low Level Input Voltage | $V_{REF}$ > 1.5V | – | 0.4 | V |

## Ordering Information

The device number is HW-PC4.

## Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 11/26/2001 | 1.0 | Initial Xilinx release. |
| 11/30/2001 | 1.1 | Changed to Advance Product Specification. |
| 01/21/2002 | 1.2 | Fixed the links in Table 4. |
| 02/06/2002 | 1.3 | Added "Signal Integrity Issues," page 8. |
| 03/08/2002 | 1.4 | Added Ordering Information. |
| 03/12/2002 | 1.5 | Updated "Features," page 1. |
| 03/03/2003 | 1.6 | Added TDO timing specification, pinout descriptions, desktop environment statement, Figure 7, fixed broken link. |
| 04/14/2003 | 1.7 | Added Spartan-3 to supported devices list, plus other edits. |
| 04/29/2003 | 1.8 | Added "Platform Flash family" to "Features," page 1. |
| 05/21/2003 | 1.9 | Fixed broken link on page 7. |
| 01/15/2004 | 2.0 | • Changed status of data sheet from Advance to Preliminary.<br>• Updated compatible PC operating systems (Win2000 and WinXP).<br>• Added Figure 5 (POD diagram).<br>• Updated FCI connector part numbers, Table 1.<br>• Changed textual references to cable from "PC IV" to "PC4". |
| 08/25/2004 | 2.1 | • Figure 4: Added note identifying Pin 1 as a "virtual ground" pin and clarifying how it should be used. Corrected part number of Molex connector. Deleted Digi-Key part number.<br>• Table 1: Added Footnote (1) regarding pin assignments. Corrected Molex connector part numbers.<br>• Table 2: Added explanation of Pin 1 "virtual ground" to definition of GND pins.<br>• Table 4: Corrected power supply part number in first line of table to DTS050400UC-P5P-KH. |
| 11/30/2005 | 2.2 | • Updated supported devices in "Features," page 1 to include all Spartan series and all Virtex series FPGAs, and removed obsolete System ACE MPM.<br>• Updated supported operating systems under "Connecting to Host Computer," page 2.<br>• Updated broken links. |
| 11/17/2006 | 2.3 | • Completed minor updates.<br>• Added support for serial-access flash PROM programming. |
| 11/28/2006 | 2.3.1 | Removed misplaced text from Figure 4, page 3. |
| 11/19/v07 | 2.4 | • Updated document template.<br>• Updated URLs.<br>• Added note to Page 1 regarding the availability of Platform Cable USB. |
| 05/14/2008 | 2.5 | • Updated "Parallel Cable IV Description," page 1 to clarify PC4 indirect programming support.<br>• Updated trademark notations. |
| 01/21/2016 | 3.0 | This product is obsolete. See XCN09016 for more information. |

## Notice of Disclaimer

THE XILINX HARDWARE FPGA AND CPLD DEVICES REFERRED TO HEREIN (“PRODUCTS”) ARE SUBJECT TO THE TERMS AND CONDITIONS OF THE XILINX LIMITED WARRANTY WHICH CAN BE VIEWED AT http://www.xilinx.com/warranty.htm. THIS LIMITED WARRANTY DOES NOT EXTEND TO ANY USE OF PRODUCTS IN AN APPLICATION OR ENVIRONMENT THAT IS NOT WITHIN THE SPECIFICATIONS STATED IN THE XILINX DATA SHEET. ALL SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE. PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS LIFE-SUPPORT OR SAFETY DEVICES OR SYSTEMS, OR ANY OTHER APPLICATION THAT INVOKES THE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR PROPERTY OR ENVIRONMENTAL DAMAGE (“CRITICAL APPLICATIONS”). USE OF PRODUCTS IN CRITICAL APPLICATIONS IS AT THE SOLE RISK OF CUSTOMER, SUBJECT TO APPLICABLE LAWS AND REGULATIONS.