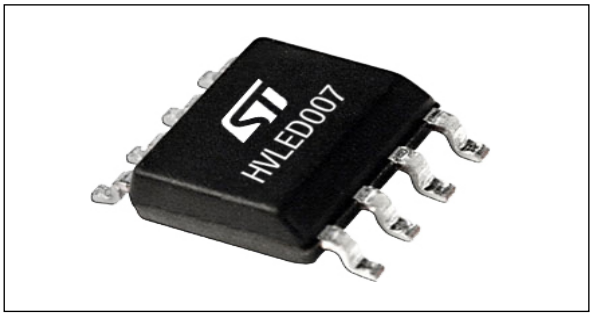
# HVLED007

# Transition mode PFC controller for flyback converters

**Datasheet - Production data**




## Features

- Transition-mode (quasi-resonant) control of flyback PFC pre-regulators
- Proprietary input current shaper for minimum THD of line current
- Control input for isolated feedback and optocoupler driving
- Output overvoltage protection
- Overload and short-circuit protection
- Low (≤ 60 µA) start-up current and low (≤ 4 ma) quiescent current
- Digital leading-edge blanking on current sense
- -600/+800 mA totem pole gate driver with UVLO pull-down and voltage clamp
- SO8 package

## Applications

Flyback PFC converters for:

- AC-DC LED drivers for domestic, commercial and industrial lighting
- Street lighting
- EN61000-3-2 compliant SMPS

## Description

The HVLED007 is a current-mode PFC controller specific for isolated high power factor, flyback converters operated in transition mode (aka quasi-resonant operation). Targeting both indoor and outdoor solid-state lighting applications, it provides extended temperature range operation down to -40 °C with guaranteed electrical specification.

The main feature of this IC is a special circuit (Input Current Shaper, ICS), that enables High-PF quasi-resonant flyback converters to draw a theoretically sinusoidal input current from the power line, unlike the traditional control.

In practice, with little effort it is possible to achieve a total distortion of the input current (THD) lower than 10% at full load and lower than 20% at 30% load over the entire input voltage range.

The IC is provided with a control input intended for being driven by the phototransistor of an optocoupler to close a secondary-regulated isolated control loop. However, with the addition of a simple external circuitry it can be used to close a primary-regulated voltage loop as well.

The HVLED007 includes protection features to handle overload, short-circuit and overvoltage conditions.

The totem-pole output stage, capable of 600 mA source and 800 mA sink current, is suitable for big MOSFET drives which, combined with the other features, makes the device an excellent low-cost solution for EN61000-3-2 compliant SMPS up to 100 W.

**Table 1. Device summary**

| Order code | Package | Packaging |
|---|---|---|
| HVLED007 | SO8 | Tube |
| HVLED007TR | | Tape and Reel |



This is information on a product in full production. www.st.com

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# 1 Block diagram

**Figure 1. Block diagram**

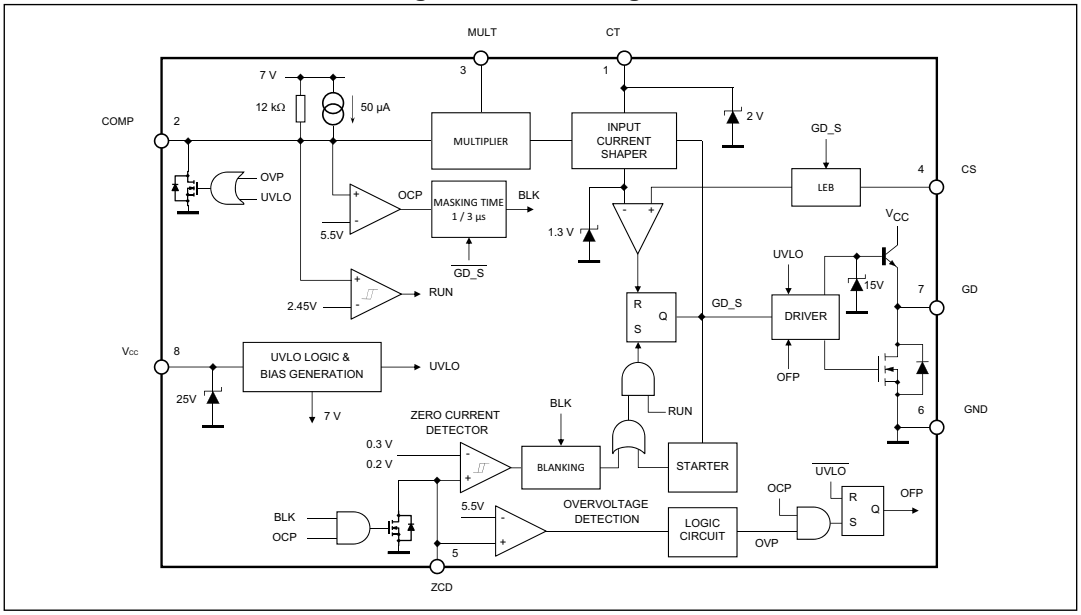



**Table 2. Absolute maximum ratings**

| Symbol | Pin | Parameter | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | 8 | IC supply voltage (Icc ≤ 20 mA) | -0.3 to VZ(1) | V |
| $I_{GD}$ | 7 | Output totem pole peak current | Self-limited | A |
| $V_{CT}$ | 1 | Voltage range | -0.3 to $V_{CTsat.hi}$(1) | V |
| $I_{CT}$ | 1 | Maximum sink current ($V_{CT} \geq V_{CTsat.hi}$(1)) | 2.5 | mA |
| $V_{COMP}$ | 2 | Voltage range | $V_{COMPsat.lo}$(1) to $V_{COMPsat.hi}$(1) | V |
| $I_{COMP.SOU}$ | 2 | Maximum source current ($V_{COMP} \leq V_{COMPsat.lo}$(1)) | 2 | mA |
| $I_{COMP.SNK}$ | 2 | Maximum sink current ($V_{COMP} \geq V_{COMPsat.hi}$(1)) | 0.8 | mA |
| $V_{MULT}$ | 3 | Voltage range | -0.3 to 8 | V |
| $V_{CS}$ | 4 | Voltage range | -0.3 to 8 | V |
| $V_{ZCD}$ | 5 | Voltage range | $V_{ZCDL}$(1) to 8 | V |
| $I_{ZCD}$ | 5 | Maximum source current ($V_{ZCD} \leq V_{ZCDL}$(1)) | -3 | mA |
| Ptot | | Power dissipation @Tamb = 50° | 0.65 | W |
| Tj | | Junction temperature operating range | -40 to 150 | °C |
| Tstg | | Storage temperature | -55 to 150 | °C |

1. See *Section 3: Electrical characteristics* for parameter definition and value.

# 2 Pin connections

**Figure 2. Pin connection (top view)**

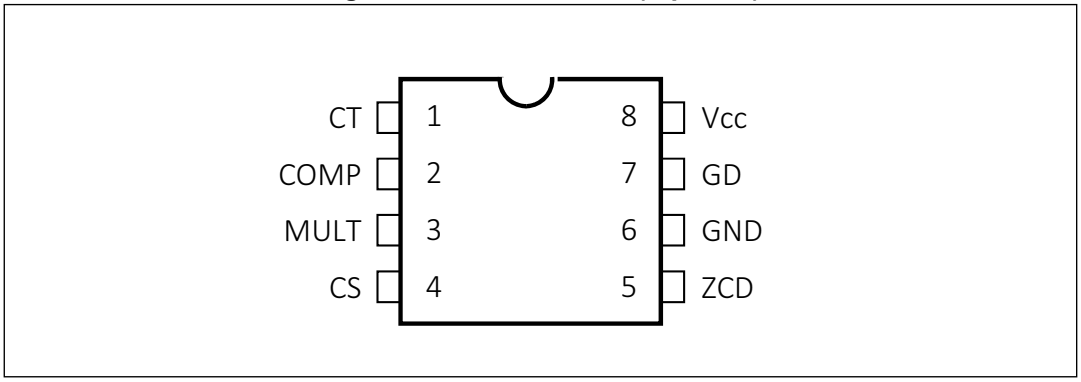



**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| Rth j-amb | Max. thermal resistance, junction-to-ambient | 150 | °C/W |

**Table 4. Pin functions**

| N. | Name | Function |
|---|---|---|
| 1 | CT | Input current shaper (ICS) circuit. A capacitor connected from this pin to ground (pin #6) is alternately charged and discharged internally, and the voltage developed across this capacitor is used as the reference for the current loop. |
| 2 | COMP | Control input for PWM regulation. The pin is driven by the phototransistor (emitter-grounded) of an optocoupler to modulate its voltage by modulating the current sunk. A capacitor placed between the pin and ground (pin #6), as close to the IC as possible to reduce noise pick-up, is useful to get a clean control voltage. The dynamics of the pin are in the 2.5 to 5.5 V range. A voltage lower than 2.5 V activates burst-mode operation. The voltage at the pin is bottom-clamped at about 2.2 V. |
| 3 | MULT | Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider. A capacitor placed between the pin and ground (pin #6), as close to the IC as possible is useful to reduce noise pick-up. |
| 4 | CS | Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with the internal reference generated by the ICS circuit, to determine MOSFET's turn-off. |
| 5 | ZCD | Transformer demagnetization sensing input for transition-mode (quasi-resonant) operation. A negative-going edge triggers MOSFET's turn-on. A voltage exceeding 5.5 V during MOSFET's OFF-time forces an internal discharge of the COMP pin (#2) below the burst-mode threshold. As a consequence, the IC is temporarily stopped (overvoltage protection). This function is strobed and digitally filtered to increase noise immunity. |
| 6 | GND | Ground. Current return for both the signal part of the IC and the gate driver. |

**Table 4. Pin functions (continued)**

| N. | Name | Function |
|---|---|---|
| 7 | GD | Gate driver output. The totem pole output stage is able to drive power MOSFETs and IGBTs with a peak current of 600 mA source and 800 mA sink. The high-level voltage of this pin is clamped at about 12 V to avoid excessive gate voltages in case the pin is supplied with a high Vcc. |
| 8 | $V_{CC}$ | Supply voltage of both the signal part of the IC and the gate driver. The supply voltage upper limit is extended to 22.5 V min. to provide more headroom for supply voltage changes. Sometimes a small bypass capacitor (0.1 µF typ.) to ground (pin #6) might be useful to get a clean bias voltage for the signal part of the IC. |

# 3 Electrical characteristics

(Tj = -40 to 125°C, Vcc=12, Co = 1 nF; unless otherwise specified.)

**Table 5. Electrical characteristics**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Supply voltage** | | | | | | |
| $V_{CC}$ | Operating range | After turn-on | 10.5 | - | 22.5 | V |
| $V_{CCon}$ | Turn-on threshold | Positive-going | 11.7 | 12.5 | 13.3 | V |
| $V_{CCoff}$ | Turn-off threshold | Negative-going | 9.5 | 10 | 10.5 | V |
| Hys | Hysteresis | - | 2.2 | - | 2.8 | V |
| $V_Z$ | Zener voltage | Icc = 20 mA | 22.5 | 25 | 28 | V |
| **Supply current** | | | | | | |
| $I_{start-up}$ | Start-up current | Before turn-on, Vcc = 11 V | - | 30 | 60 | µA |
| Iq | Quiescent current | After turn-on, $V_{MULT}$ = 1 V, $V_{COMP} = V_{COMPsat.hi}$, $V_O = V_{OL}$ | - | 2.5 | 3.9 | mA |
| | | During burst mode | - | 1.7 | 2.5 | mA |
| $I_{CC}$ | Operating supply current | @ 70 kHz, D = 50%, $V_{MULT}$ = 1V, $V_{COMP} = V_{COMPsat.hi}$ | - | 3.5 | 5.5 | mA |
| **Input current shaper** | | | | | | |
| $V_{CT}$ | Operating range | - | 0 | - | 1.5 | V |
| $V_{CTsat.hi}$ | Upper clamp voltage | (1) | 1.5 | 2 | 2.5 | V |
| $R_T$ | Internal discharge resistor | - | - | 8.3 | - | kΩ |
| $V_{CT_OL}$ | Overload detection threshold | Positive-going(1) | 1.25 | 1.4 | 1.6 | V |
| **PWM control input** | | | | | | |
| $V_{COMPsat.hi}$ | Upper saturation voltage | - | 5.8 | 6.2 | 6.7 | V |
| $V_{COMP_OL}$ | Overload detection threshold | Positive-going | 5.25 | 5.5 | 5.7 | V |
| $\Delta V_{COMP_OL}$ | Comparator hysteresis | Negative-going | - | 100 | - | mV |
| $V_{COMPlo}$ | Lower end of regulation range | (2) | 2.35 | 2.5 | 2.65 | V |
| $V_{COMP_BM}$ | Burst-mode threshold | Negative-going(2) | 2.3 | 2.45 | 2.6 | V |
| $\Delta V_{COMP_BM}$ | Comparator hysteresis | Positive-going | - | 50 | - | mV |
| $V_{COMPsat.lo}$ | Lower clamp voltage | ICOMP = -700 µA | 2.05 | 2.2 | 2.35 | V |
| $I_{COMPsat}$ | Source current | $V_{COMP} = V_{COMPsat.hi}$ | - | 50 | - | µA |
| $I_{COMPmax}$ | Maximum source current | $V_{COMP} = V_{COMP_BM}$ | - | 350 | 600 | µA |

**Table 5. Electrical characteristics (continued)**

| Symbol | Parameter | Test condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $R_{COMP}$ | Equivalent dynamic resistance | $V_{COMPlo} < V_{COMP} < V_{COMP_OL}$ | | 8 | 12 | 19 | kΩ |
| **Multiplier input** | | | | | | | |
| $I_{MULT}$ | Input bias current | $V_{MULT}$ = 0 to 4 V | | - | - | -1 | µA |
| $V_{MULT}$ | Linear operation range | - | | 0 to 3 | - | - | V |
| ΔVcs | Output max. slope | $V_{MULT}$ = 0 to $V_{csmax}$<br>$V_{COMP} = V_{COMPsat.hi}$ | | 1 | 1.1 | - | V/V |
| $\Delta V_{MULT}$ | | | | | | - | - |
| $K_M$ | Gain | $V_{MULT}$ = 1 V, $V_{COMP}$ = 5.25 V | | 0.375 | 0.4 | 0.45 | 1/V |
| **Current sense comparator** | | | | | | | |
| $I_{CS}$ | Input bias current | $V_{CS}$ = 0 to $V_{CSmax}$ | | - | - | -1 | µA |
| $t_{d(H-L)}$ | Delay to output | - | | - | 240 | - | ns |
| $t_{LEB}$ | Leading edge blanking | After turn-on of GD<br>$V_{MULT}$ = 1 V | | 100 | 200 | 300 | ns |
| $V_{CSmax}$ | Current sense reference clamp | $V_{COMP} = V_{COMPsat.hi}$ | Tj = 25°C | 1.25 | 1.3 | 1.35 | V |
| | | | - | 1.2 | - | 1.4 | |
| **Zero current detector** | | | | | | | |
| $V_{ZCDA}$ | Arming voltage | Positive-going edge(3) | | 0.2 | 0.3 | 0.4 | V |
| $V_{ZCDT}$ | Triggering voltage | Negative-going edge(3) | | 0.15 | 0.2 | 0.25 | V |
| $V_{ZCDL}$ | Lower clamp voltage | $I_{ZCD}$ = -50 µA to -2.5 mA | | -0.15 | 0 | 0.1 | V |
| $V_{ZCDmax}$ | Maximum operating voltage | - | | 7 | - | - | V |
| $I_{ZCDb}$ | Input bias current | $V_{ZCD}$ = 1 V to $V_{ZCDmax}$<br>$V_{COMP}<V_{COMPsat.hi}$, $V_{CT}<V_{CT_OL}$ | | - | - | 1 | µA |
| $I_{ZCDsrc}$ | Source current capability | $V_{ZCD} = V_{ZCDL}$ | | - | - | 2.5 | mA |
| $T_{MASK}$ | Masking time (after turn-off of GD) | $V_{COMP} < V_{COMP_OL}$ | | 0.6 | 1 | 1.5 | µs |
| | | $V_{COMP}$ $V_{COMP_OL}$ | | 1.8 | 3 | 4.5 | |
| $R_{DS(on)}$ | Grounding switch ON-state resistance | - | | - | 300 | - | Ω |
| **Output overvoltage** | | | | | | | |
| $V_{ZCD_OVP}$ | OVP comparator threshold | Positive-going | | 5.3 | 5.5 | 5.7 | V |
| **Starter** | | | | | | | |
| $t_{START}$ | Start Timer period | - | | 170 | 280 | 440 | µs |
| **Gate driver** | | | | | | | |
| $V_{OL}$ | Output low voltage | $I_{sink}$ = 100 mA | | - | 0.6 | 1.2 | V |
| $V_{OH}$ | Output high voltage | $I_{source}$ = 5 mA | | 9.5 | 10.3 | - | V |
| $I_{srcpk}$ | Peak source current | - | | -0.6 | - | - | A |

**Table 5. Electrical characteristics (continued)**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{snkpk}$ | Peak sink current | - | 0.8 | - | - | A |
| $t_f$ | Voltage fall time | - | - | 30 | 70 | ns |
| $t_r$ | Voltage rise time | - | - | 60 | 130 | ns |
| $V_{Oclamp}$ | Output clamp voltage | $I_{source}$ = 5mA; Vcc = 20 V | 10 | 12 | 15 | V |
| - | UVLO saturation | Vcc= 0 to $V_{CCon}$, $I_{sink}$= 2 mA | - | - | 1.1 | V |

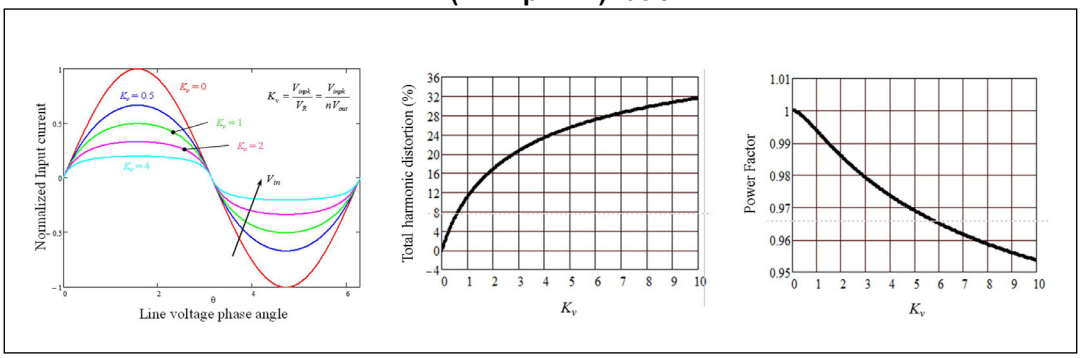
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# 4 Application information

## 4.1 Introduction

The HVLED007 is intended to drive Hi-PF QR flyback converters, an extremely popular topology in SSL applications because it is very cost-effective and addressable with the same transition-mode (TM) PFC controllers used for boost PFC stages. However, the TM control technique that in boost PFC stages theoretically provides a sinusoidal input current and unity power factor, in Hi-PF QR flyback converters features inherent distortion of the input current, as depicted in the diagrams of *Figure 3*.

**Figure 3. Input current distortion in Hi-PF QR flyback converters with traditional TM control: current shape and resulting total harmonic distortion and power factor vs. Kv (= Vinpk/VR) ratio**




Traditionally, to keep current distortion within acceptable limits, the converter is designed to operate with low $K_V$ (= $V_{inpk}$ /$V_R$) values, achieved using a large reflected voltage $V_R$ = ($N_{pri}$ / $N_{sec}$) $V_{out}$. This, however, requires the use of a power switch (MOSFET) with higher breakdown voltage.

Additionally PFC controllers intended for boost topology, this being a non-isolated topology, do not normally have on-board protection functions suitable for a flyback converter and that therefore need to be implemented with additional external circuits. On the other hand, they have provisions on board that are little useful in an isolated topology like a flyback (e.g. the error amplifier).

The HVLED007 addresses these aspects specifically, providing a novel TM control technique able to provide a sinusoidal input current and unity power factor in flyback converters as well and protection functions typical of offline flyback controller ICs.

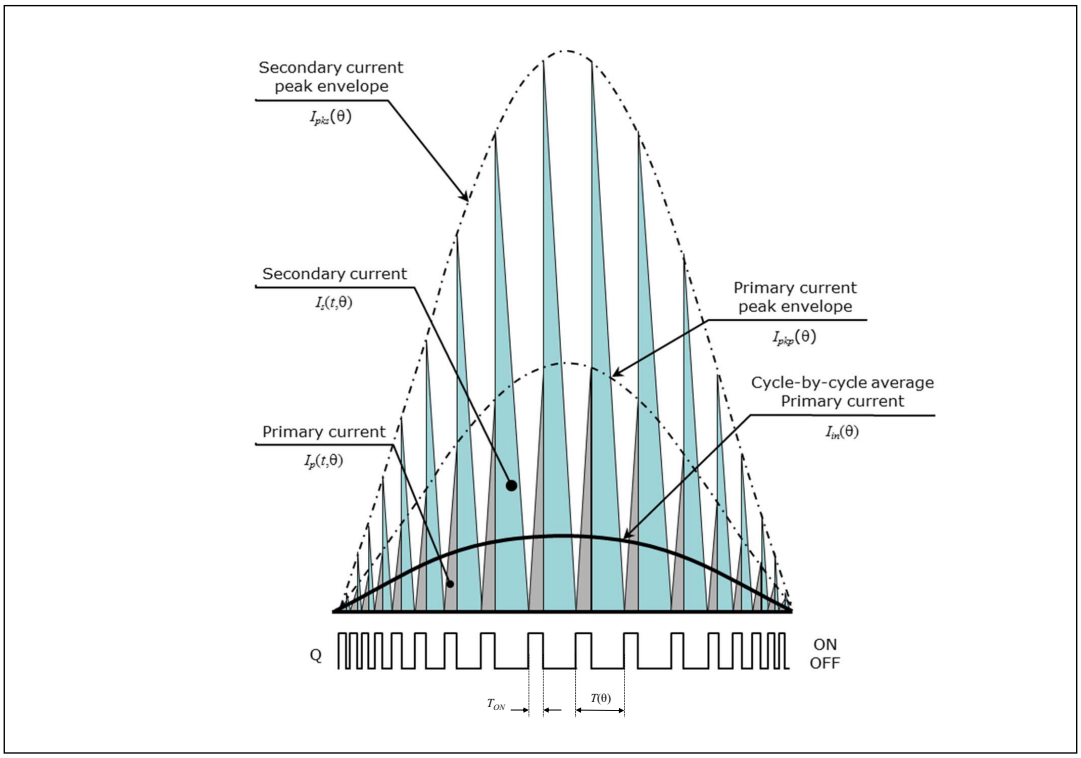
## 4.2 Input current shaping function - operating principle

In a Hi-PF QR flyback converter powered from an AC line with a sinusoidal voltage $V_{in}(\theta) = V_{inpk} \sin\theta$, (with $\theta = 2\pi f_{line} t$) the input current is the average of the primary current, which flows only during the ON-time of the power switch and is a series of triangles separated by voids corresponding to the OFF-time of the power switch (see current waveforms in *Figure 4*). This can be expressed quantitatively as follows:

**Equation 1**

$$I_{in}(\theta) = \frac{1}{2} Ip_{pk}(\theta) \frac{T_{ON}}{T(\theta)}$$

**Figure 4. Hi-PF QR flyback converter with the traditional TM control: current waveforms**




With the traditional TM control method, the term $Ip_{pk}(\theta)$, the peak envelope of the primary current, is sinusoidal ($Ip_{pk}(\theta) = Ip_{pk} \sin \theta$). The distortion stems from the term $T_{ON} / T(\theta)$, due to the primary current being chopped, which is not constant ($T_{ON}$ is constant, $T(\theta)$ is not).

This distortion is prevented if the flyback converter is operated with a fixed switching frequency in the Discontinuous Conduction Mode (DCM). However, there are a few benefits in using TM operation that are lost when operating with a fixed frequency (FF): lower conducted EMI emissions, safer operation under short-circuit conditions, valley-switching or even true soft-switching (zero-voltage switching, ZVS).

The idea behind the novel TM method is to distort the current reference $Vcs_{ref}(\theta)$ that determines $Ip_{pk}(\theta)$ ($Ip_{pk}(\theta) = Vcs_{ref}(\theta) / Rs$) by a term $T(\theta) / T_{ON}$ : this cancels out the term $T_{ON} / T(\theta)$ introduced by averaging and results in a sinusoidal average primary current, i.e. in a sinusoidal input current. Then, the control objective can be expressed in the following terms:

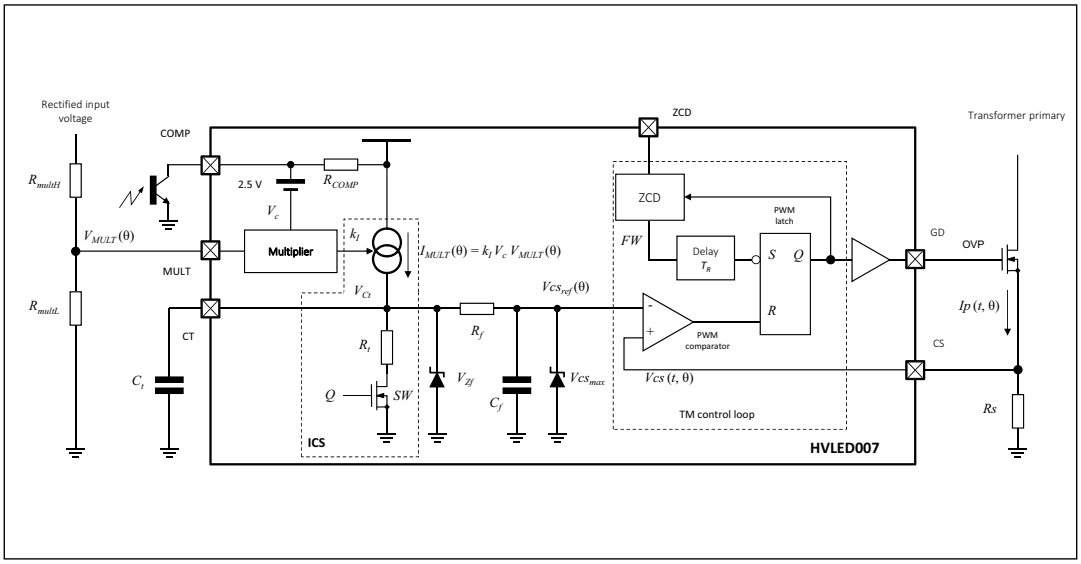
**Equation 2**

$$Vcs_{ref}(\theta) = Vcs_x \sin \theta \frac{T(\theta)}{T_{ON}(\theta)}$$

Note that in *Equation 2* also $T_{ON}$ is denoted as a function of the instantaneous line phase θ; in fact, with the novel method it is no longer constant as in the traditional method.

The "Input Current Shaper" (ICS) that implements this basic idea is shown in *Figure 5* along with the overall control loop inside the IC.

**Figure 5. Input current shaper (ICS) block and its interconnection with HVLED007 control**




The ON/OFF mechanism of the external power switch is exactly the same as in the traditional TM method: the power switch is turned on as the secondary current zeroes (with a delay $T_R$ to achieve valley switching, see "*Section 4.8: Zero current detection and triggering block (pin ZCD); starter*") and turned off when the voltage *Vcs* (*t*, θ) on the current sensing input CS (proportional to the primary current *Ip* (*t*, θ)) reaches the reference value $Vcs_{ref}$ (θ). Note that the explicit dependence on time (*t*) denotes cycle-by-cycle quantities.

The difference between the traditional TM method and that implemented in the HVLED007 is in the way the reference $Vcs_{ref}$ (θ) is generated. In the traditional TM method, $Vcs_{ref}$ (θ) is generated by taking the input voltage as the template and adjusting its amplitude with feedback loop control voltage via the multiplier; in the HVLED007 the output of the multiplier is processed by the ICS circuit highlighted in the dotted box before being provided to the PWM comparator. The ICS circuit is composed of the current generator $I_{MULT}$ (θ), the external capacitor $C_t$ connected between pin CT and ground and a switched resistor $R_t$ that is connected in parallel to $C_t$ during the ON-time $T_{ON}$ (θ) of the power switch through the switch *SW*. The current generator provides the charging current for $C_t$, given by:

**Equation 3**

$$I_{MULT}(\theta) = k_I \left[K_p \left(V_{inpk} \sin\theta\right) V_c\right]$$

where $K_p = R_{multL} / (R_{multH} + R_{multL})$ is the voltage gain of the resistor divider that senses the rectified input voltage. The key waveforms are shown in *Figure 6*.

Assuming $T(\theta) << R_t C_t << 1/(2 f_{line})$, to a first approximation the voltage ripple across the capacitor $C_t$ can be neglected and the current $I_{MULT}$ (θ) can be considered constant in a switching cycle. The average voltage $V_{Ct}$ (θ) developed across $C_t$, which shapes the peak primary current $Ip_{pk}$(θ), is found by charge balance in a switching cycle:

**Equation 4**

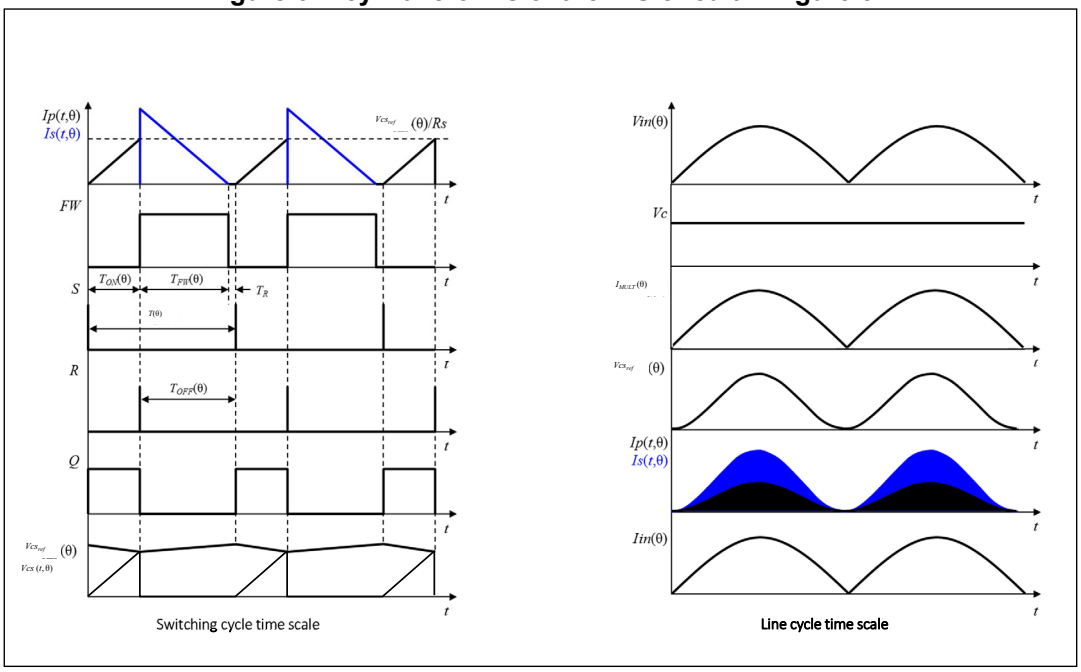
$$I_{MULT}(\theta)\ T(\theta) = \frac{V_{Ct}(\theta)}{R_t} T_{ON}(\theta)$$

Solving (*Equation 4*) for $V_{Ct}(\theta)$:

**Equation 5**

$$V_{Ct}(\theta) = I_{MULT}(\theta)\ R_t \frac{T(\theta)}{T_{ON}(\theta)}$$

**Figure 6. Key waveforms of the ICS circuit in figure 5**




$V_{Ct}(\theta)$ is connected to the (-) input of the PWM comparator through the low-pass filter $R_f C_f$, whose purpose is to remove unwanted high frequency noise. The associated time constant ($\approx$ 100 ns) is such that the voltage across $C_f$ is not significantly different from that across $C_t$, so that $V_{Ct}(\theta)$ is actually the reference $Vcs_{ref}(\theta)$ for the current loop. If we substitute the expression (*Equation 3*) of $I_{MULT}$ into (*Equation 5*) we find:

**Equation 6**

$$Vcs_{ref}(\theta) = V_{Ct}(\theta) = [K_p(V_{inpk} \sin\theta)\ V_c]\ \ k_I\ R_t \frac{T(\theta)}{T_{ON}(\theta)}$$

that has exactly the desired form (*Equation 2*) with:

**Equation 7**

$$Vcs_x = [K_p\ (\ V_{inpk})\ V_c]\ k_I\ R_t$$

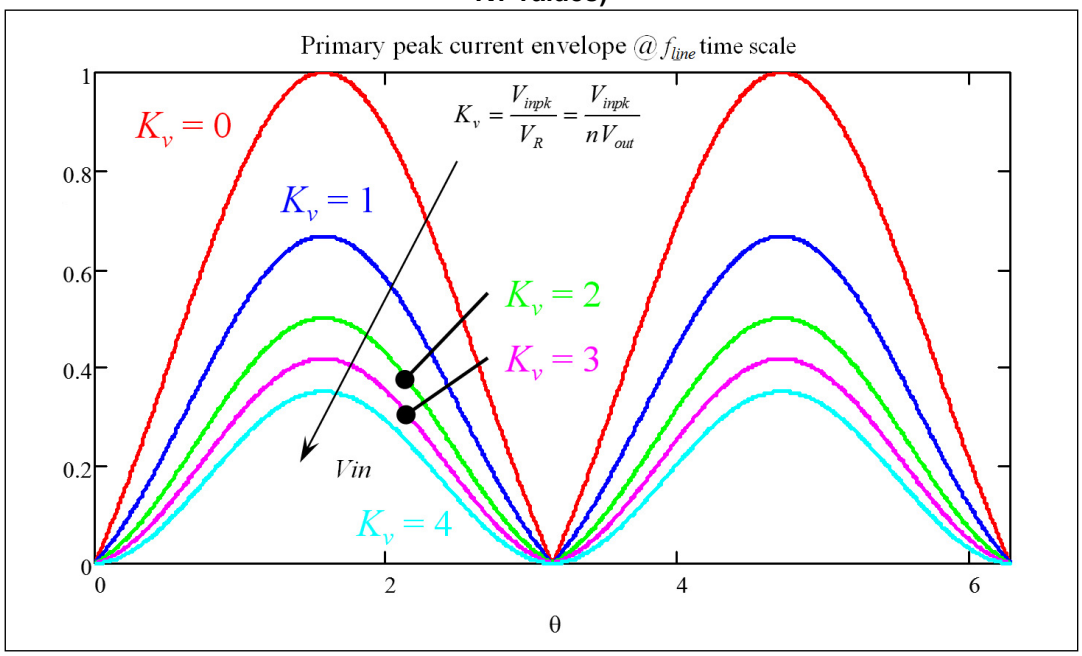
In order for (*Equation 6*) to meet the control objective (*Equation 2*) it is necessary that $V_c$ is constant along a line half-cycle. This is a normal design target in any Hi-PF converter, thus the ICS circuit actually meets the control objective. The resulting shape of $Vcs_{ref}(\theta)$ is shown in *Equation 7* for different values of $K_v$.

It is worth noting that in (*Equation 7*) the parameter $K_p$ is selected by the user (see "*Section 4.12: Suggested step-by-step design procedure of a Hi-PF QR flyback converter based on the HVLED007*"), $V_c$ corresponds to $V_{COMP}$ - 2.5 V and the quantity $k_l R_t$ to the multiplier gain $K_M$ listed among the parameters in "*Section 3: Electrical characteristics*".

The voltage $Vcs_{ref}(\theta)$ is clamped at a value $Vcs_{max}$ that determines the maximum amplitude of the signal on the current sense input CS. This value, listed among the parameters in "*Section 3: Electrical characteristics*", is accurate because it determines the maximum power deliverable by the converter and is used to design the saturation current of the flyback transformer (see "*Section 4.7: Current sensing input (pin CS). Sense resistor (Rs) selection*").

Also the voltage across $C_t$ is internally clamped (at $V_{Zf} > Vcs_{max}$) to prevent a too large dead zone between the external voltage generated across $C_t$ by the shaping circuit and $Vcs_{ref}(\theta)$ internally clamped at $Vcs_{max}$. For further details about the operating principle and the effect of non-idealities please refer to Reference 1.

**Figure 7. Shape of the current reference Vcsref(θ) (5) at different input voltages (i.e. Kv values)**




## 4.3 Operation of a Hi-PF QR flyback converter based on the HVLED007

The ICS circuit changes the profile of the peak current envelope along a line half-cycle (as shown in *Figure 7*) and this slightly changes the timing and the electrical quantities in the converter in steady-state operation as compared to those of a traditionally controlled Hi-PF QR flyback converter [Reference 2]. There are differences in the peak and rms currents but

no difference in the voltage stresses apart from those caused by parasitics and resulting from the different peak currents.

The timing, the control and electrical quantities of a Hi-PF QR flyback converter based on the HVLED007, needed for a proper design, are summarized in *Table 6*, *7* and *8* respectively. The symbolism used has been defined already or is obvious.

Their derivation is based on some simplifying assumptions (in addition to $T(\theta) << R_t C_t << 1/(2 f_{line})$):

- the voltage drop across the EMI filter, the input bridge and the power switch in the ON-state are negligible as compared to the instantaneous line voltage;
- transformer's efficiency is 100% and its windings are perfectly coupled;
- ZCD circuit's delay $T_R$ is negligible, so the converter is assumed to work exactly at the boundary between the continuous and the discontinuous current conduction mode.

Please refer to [Reference 1] for more information on their derivation. It is worth noting that:

- Switching frequency along a line half-cycle is at a minimum on the peak of the sinusoid ($\theta = \pi/2$) and rises along the edges to reach the maximum value at the zero-crossings of the line voltage ($\theta = 0$ and $\theta = \pi/2$).
- The absolute minimum of the switching frequency occurs on the peak of the sinusoid at the maximum input power ($P_{in} = P_{in_max}$) and at the minimum input voltage ($K_v = K_{v_min} = V_{inpk_min} / V_R$).
- The ON-time of the power switch behaves exactly the other way round: it is at a maximum on the peak of the sinusoid, goes to a minimum at the zero-crossings and increases with $P_{in}$.
- All peak and rms currents have a maximum at the maximum input power ($P_{in} = P_{in_max}$) and the minimum input voltage ($K_v = K_{v_min}$).

**Table 6. Timing quantities in a HVLED007-based Hi-PF QR flyback converter**

| Eq. # | Parameter | Expression |
|---|---|---|
| 1 | Power switch ON-time | $T_{ON}(\theta) = 4 \frac{Lp}{V_R^2} P_{in} \frac{1 + K_v \sin\theta}{K_v^2}$ |
| 2 | Switching period | $T(\theta) = 4 \frac{Lp}{V_R^2} P_{in} \left(\frac{1 + K_v \sin\theta}{K_v}\right)^2$ |
| 3 | Switching frequency | $f_{sw}(\theta) = \frac{1}{T(\theta)} = \frac{1}{4} \frac{V_R^2}{Lp\, P_{in}} \left(\frac{K_v}{1 + K_v \sin\theta}\right)^2$ |
| 4 | Duty cycle | $D(\theta) = \frac{T_{ON}(\theta)}{T(\theta)} = \frac{1}{1 + K_v \sin\theta}$ |

**Table 7. Control quantities in a HVLED007-based Hi-PF QR flyback converter**

| Eq. # | Parameter | Expression |
|---|---|---|
| 1 | Control voltage | $V_c = \frac{4}{K_v^2}\frac{P_{in}}{V_R^2}\frac{Rs}{K_m K_p}$ |
| 2 | ICS charge current | $I_{MULT}(\theta) = \frac{4}{K_v}\frac{P_{in}}{V_R}\frac{Rs}{R_t}\sin\theta$ |
| 3 | Current reference | $Vcs_{ref}(\theta) = 4\,Rs\,\frac{P_{in}}{V_R}\sin\theta\frac{1 + K_v \sin\theta}{K_v}$ |
| 4 | Peak-to-peak current reference ripple at switching frequency | $\Delta Vcs_{ref}(\theta) = \frac{1}{R_t C_t}\left(\frac{4P_{in}}{K_v V_R}\sin\theta\right)^2 \frac{Rs\,Lp}{V_R}(1 + K_v \sin\theta)$ |

**Table 8. Electrical quantities in a HVLED007-based Hi-PF QR flyback converter**

| Eq. # | Parameter | Expression |
|---|---|---|
| 1 | Peak envelope of primary current | $Ip_{pk}(\theta) = 4\,\frac{P_{in}}{V_R}\sin\theta\frac{1 + K_v \sin\theta}{K_v}$ |
| 2 | Primary peak current | $Ip_{pk} = 4\,\frac{P_{in}}{V_R}\frac{1 + K_v}{K_v}$ |
| 3 | Primary rms current | $Ip_{rms} = 4\,\frac{P_{in}}{V_R}\frac{1}{K_v}\sqrt{\frac{1}{6} + \frac{4}{9\pi}K_v}$ |
| 4 | Primary DC current | $Ip_{dc} = \frac{4}{\pi K_v}\frac{P_{in}}{V_R}$ |
| 5 | Primary AC current | $Ip_{ac} = 4\,\frac{P_{in}}{V_R}\frac{1}{K_v}\sqrt{\frac{1}{6} - \frac{1}{\pi^2} + \frac{4}{9\pi}K_v}$ |
| 6 | Secondary peak current | $Is_{pk} = 4\,\frac{1 + K_v}{K_v}I_{out}$ |

| Eq. # | Parameter | Expression |
|---|---|---|
| 7 | Secondary rms current | $Is_{rms} = I_{out}\sqrt{2+\frac{64}{9\pi K_v}}$ |
| 8 | Secondary DC current | $Isdc = Iout$ |
| 9 | Secondary AC current | $Is_{ac} = I_{out}\sqrt{1+\frac{64}{9\pi K_v}}$ |
| 10 | Low-frequency secondary current | $I_o(\theta) = 2\,I_{out}\,sin^2\,\theta = I_{out}\,(1 - cos\,2\theta)$ |
| 11 | Low-frequency output voltage ripple | $\Delta V_{o-pk} = I_{out}\frac{1}{2(2\pi f_{line})\,C_{out}} = \frac{I_{out}}{4\pi f_{line}\,C_{out}}$ |

As to the dynamic properties of a HVLED007-based Hi-PF QR flyback converter, the ICS circuit is essentially transparent: it only affects the DC gain of the feedback loop. This is intuitive if one recalls that one of the basic assumptions was that the time constant associated to the ICS circuit were << 1/(2 $f_{line}$) and that in Hi-PF converters the crossover frequency of the loop is typically much lower than $f_{line}$.

Assuming 100% efficiency and that the Hi-PF QR flyback converter powers one or more downstream switching regulators that drive the LED strings, the control-to-output transfer function is:

**Equation 8**

$$G(s) = \frac{I_{out}}{V_c}\frac{1}{sC_{out}} = \left(\frac{1}{2}\frac{N_{pri}}{N_{sec}}K_v\right)^2 K_M\,K_P\frac{V_{out}}{Rs}\frac{1}{sC_{out}}$$

## 4.4 Shaping capacitor ($C_t$) selection (pin CT)

As previously mentioned, one fundamental assumption for proper operation of the novel control method implemented in the HVLED007 is that the time constant $R_t\,C_t$ associated to the ICS meets the constraints:

**Equation 9**

$$T(\theta) << R_t\,C_t << 1/(2f_{line})$$

The left-hand side inequality ensures that the voltage across the shaping capacitor $C_t$ is essentially a DC level in any given switching cycle; the right-hand inequality ensures that this DC level is able to change quickly enough to closely follow the ideal reference given by (*Equation 6*) and depicted in *Figure 7*.

With the HVLED007, since $R_t$ is fixed inside the control IC ($R_t$ = 8.3 kΩ) the design objective is to properly select the value of $C_t$. This is done looking basically at two interrelated factors: the amplitude of the ripple voltage $\Delta V_{Ct}(t, \theta)$ across $C_t$ at the switching frequency and the Total Harmonic Distortion (THD) of the input current. The amplitude of $\Delta V_{Ct}(t, \theta)$ affects also the maximum available signal on the current sense input and, then, the selection of the sense resistor *Rs*. Please refer to "*Section 4.7: Current sensing input (pin CS). Sense resistor (Rs) selection*" for more information concerning this point.

The ripple voltage, generated by the charge and discharge of $C_t$ through $I_{MULT}(\theta)$ and $R_t$, can be considered essentially triangular and symmetrically superimposed on the slowly varying (at 2 $f_{line}$) DC value $V_{Ct}(\theta)$. Its peak-to-peak amplitude is given in equation #4 contained in *Table 7*. As discussed in [Reference 1], this ripple causes distortion of the current reference and a reduction of the programmed peak current. Both can be significant if the ripple amplitude is not adequately low.

As a rule of thumb, the maximum peak-to-peak value of $\Delta V_{Ct}(t, \theta)$ should not exceed 10% of the maximum amplitude of $V_{Ct}(\theta)$. Both amplitudes are at a maximum at the maximum input power ($P_{in} = P_{in_max}$) and minimum input voltage ($K_v = K_{v_min}$).

Combining equations #3 and #4 of *Table 7*, this condition can be expressed as:

**Equation 10**

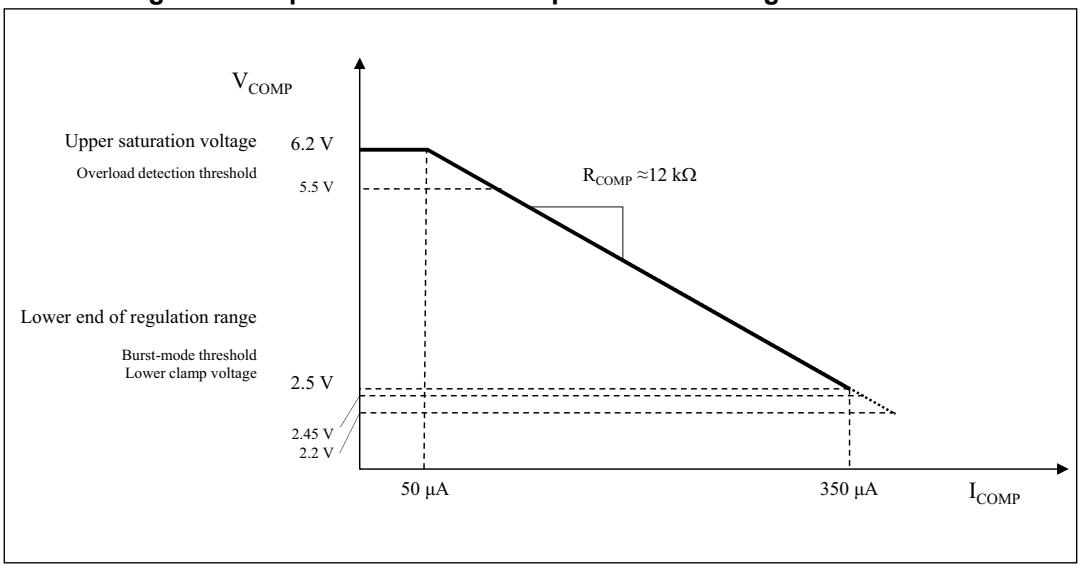
$$\frac{\Delta Vcs_{ref}}{Vcs_{ref}} = \frac{4}{R_t C_t} \frac{Lp\ P_{in_max}}{K_{v_min}\ V_R^2}\ sin\theta \le 0.1$$

With this choice the programmed peak current $Vcs_{ref}(\theta)$ - $\Delta Vcs_{ref}(\theta)$ /2 is less than 5% lower than the value calculated with equations #1 and #2 in *Table 8*, which neglect the contribution of the ripple (see "*Section 4.7: Current sensing input (pin CS). Sense resistor (Rs) selection*" for more details). The distortion caused by the ripple does not exceed 2.5% and the resulting time constant $R_t C_t$ is typically in the range of 4 to 5 times the maximum switching period $T(\theta)_{max}$. Experience shows that this value is close to the value that minimizes the THD of the input current for line frequencies in the range of 47 to 63 Hz, which is the range typically specified for applications running from most of the power lines worldwide.

## 4.5 Control input for isolated feedback and optocoupler driving (pin COMP)

Pin COMP is to be driven by the phototransistor (emitter-grounded) of an optocoupler to modulate its voltage by modulating the current sourced by the pin. *Figure 8* shows the output characteristic of the pin.

**Figure 8. Output characteristic of pin COMP and significant levels**




As long as the current $I_{COMP}$ sourced by pin COMP does not exceed 50 µA, the voltage $V_{COMP}$ on pin COMP stays at its upper saturation voltage (6.2 V). For higher $I_{COMP}$ values $V_{COMP}$ falls linearly with a slope corresponding to a resistance $R_{COMP}$ of about 12 kΩ until it reaches the lower end of the regulation range (2.5 V). Values of $V_{COMP}$ higher than 5.5 V are interpreted as an "out of regulation condition" (see "*Section 4.9: Overload and short-circuit protection (OCP function)*"). $V_{COMP}$ is bottom-clamped at 2.2 V to prevent a too large dead-zone under the lower end of the regulation range.

A capacitor placed between the pin and ground, as close to the IC as possible, may be used to either set a pole in the output-to-control transfer function or, in case frequency compensation is done entirely on the secondary side, just reduce noise pick-up. In the latter case it is recommended that the additional pole set in the transfer function by the filter capacitor along with the dynamic resistance of pin COMP ($R_{COMP}$) is placed at least at a decade above the crossover frequency of the overall open-loop transfer function.

It is worth noting that pin COMP can be driven also by a TS431 to close a control loop in non-isolated applications or in isolated applications with primary sensing regulation. Additionally, forcing pin COMP below 2.45 V by an external switch results in disabling the converter.

- Burst-mode operation. When $V_{COMP}$ falls below $V_{COMP_BM}$ (= 2.45 V) a comparator triggers the so-called "static OVP" function, thus forcing the system to stop and initiating burst-mode operation. While operating in this mode, the HVLED007 provides a series of a few switching cycles spaced out by idle periods where the external power switch is in OFF-state. This ensures system's ability to regulate the output voltage under no load conditions.
  More in detail, the HVLED007 stops switching as $V_{COMP}$ falls below $V_{COMP_BM}$; the Start Timer (see "*Section 4.8: Zero current detection and triggering block (pin ZCD); starter*") is disabled too. While in the idle state, the converter being stopped, no energy is delivered to the output, so the output voltage starts decaying. The feedback circuit reacts to this droop and, as a consequence, $V_{COMP}$ increases; as it exceeds $V_{COMP_BM}$ by 50 mV, the Start Timer is re-enabled and the IC restarts switching either by a negative-going edge on the ZCD pin (if the idle time is short enough and the drain voltage is still ringing, see "*Section 4.8: Zero current detection and triggering block (pin ZCD); starter*") or by the Start Timer if no edge is detected on the ZCD pin. If the load level has not changed, after

a short while $V_{COMP}$ falls again below $V_{COMP_BM}$ in response to the energy burst and stops again the IC, repeating the same sequence.
With this operating mode the duration of each burst and the idle time are automatically adjusted according to the load conditions: as the load is progressively decreased, the number of switching cycles in each burst becomes smaller and smaller and the duration of the idle time becomes longer and longer. If the load increases, the number of switching cycles in each burst becomes larger and the duration of the idle time becomes shorter, until the operation becomes again continuous.

## 4.6 Multiplier input for input voltage sensing (pin MULT)

The multiplier input (MULT) is intended to sense the rectified input voltage through a resistor divider to provide a sinusoidal template to the multiplier and the ICS circuit.

The user needs to properly select the voltage gain of the resistor divider $K_p$. The selection criterion is that $K_p$ needs to be large enough so that the peak of the programming signal $Vcs_{ref}(\theta)$ generated by the ICS circuit at the minimum input voltage can reach the range of the clamp value $Vcs_{max}$ with a level of $V_{COMP}$ voltage lower than the overload detection threshold $V_{COMP_OL}$ (see "*Section 4.5: Control input for isolated feedback and optocoupler driving (pin COMP)*"). The condition to fulfill is:

**Equation 11**

$$K_p V_{inpk-min} = V_{MULTpk_min} \geq \frac{Vcs_{max_min}}{K_{M_min}(V_{COMP_OL_min} - V_{COMPIo})(1+K_{v_min})} = \frac{1.231}{1+K_{v_min}}$$

with $K_{v_min} = V_{inpk_min}/V_R$. It is recommended that $K_p$ be as close to the value given by (*Equation 11*) as possible (compatibly with expected tolerance of $K_p$), so as to maximize the usage of the regulation range of $V_{COMP}$.

It is also recommended to check that with the selected $K_p$ the amplitude of $V_{MULTpk}$ calculated at the peak of the maximum specified input voltage does not exceed 3 V (linearity limit of the multiplier), in which case the value of $K_{v_min}$ should be increased (i.e. $V_R$ reduced). Normally, this should not happen: the parameters of the ICS circuit have been designed so as to allow a reflected voltage as high as 250 V even in an ultra-wide range application ($V_{in}$ = 85 to 305 Vac).

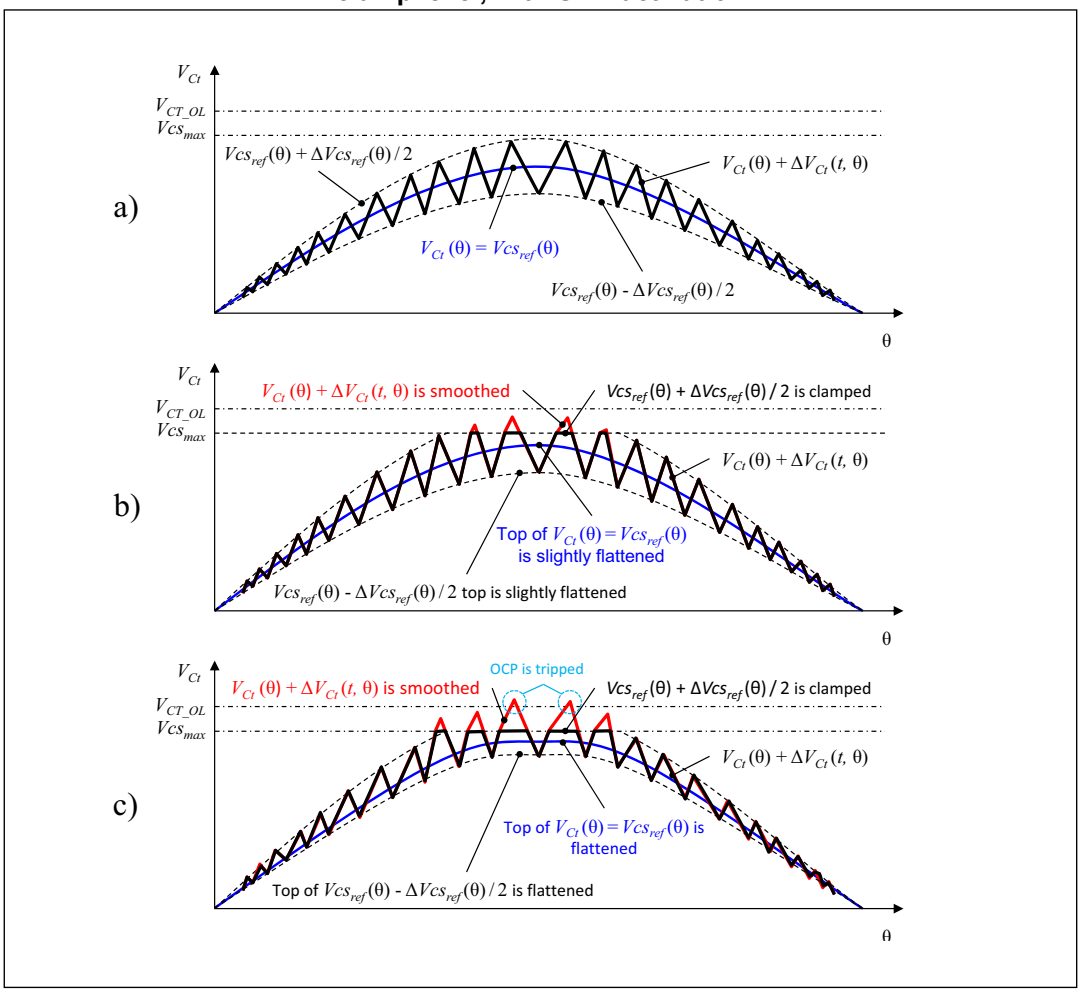
## 4.7 Current sensing input (pin CS). Sense resistor (Rs) selection

The PWM comparator (see *Figure 4*) senses the voltage $Vcs(t, \theta)$ across the current sense resistor $Rs$ and, by comparing it to the programming signal $Vcs_{ref}(\theta)$ generated by the ICS circuit, determines the exact time when the external power switch is to be switched off, i.e. $Vcs(T_{ON}(\theta), \theta) = Vcs_{ref}(\theta)$. Its output resets the PWM latch, previously set by the ZCD triggering block (see *Section 4.8: Zero current detection and triggering block (pin ZCD); starter*), which asserts the gate driver output low. The use of PWM latch avoids spurious switching of the external power switch that might result from the noise generated ("double-pulse suppression").

Cycle-by-cycle current limitation is realized by clamping the programming signal $Vcs_{ref}(\theta)$ at a value $Vcs_{max}$ (= 1.3 V typ.). The value of $Vcs_{max}$, along with that of the sense resistor $Rs$, determines the overcurrent setpoint, i.e. the maximum peak current $Ip_{pk\ max}$ allowed to flow

on the primary side. If the power demanded by the load requires a larger primary current this results in a no longer regulated output voltage and in a gradual reduction of the power throughput of the converter as the output voltage gets lower.

**Figure 9. Effect of ripple on Ct on current sense signal: a) within linear dynamics, close to clamp level; b) signal slightly exceeding clamp level; c) signal exceeding clamp level, with OCP activation**




The value of $Ip_{pk\ max}$ is selected so as to ensure with adequate margin that the full load power can be delivered to the output at the minimum specified input voltage, i.e. it is larger than the value provided by equation #2 in *Table 8* with $P_{in} = P_{in_max}$ and $K_v = K_{v_min}$.

However, when determining the value of *Rs*, the effects of the ripple voltage across the shaping capacitor $C_t$ might need taking into account. In fact, as shown in the key waveforms at switching frequency time scale in *Figure 6*, the turn-off of the power switch occurs on the valleys of the ripple. So, the exact turn-off condition is:

**Equation 12**

$$Vcs\ (T_{ON}(\theta), \theta) = Vcs_{ref}(\theta) - \Delta Vcs_{ref}(\theta)/2$$

and the programmed peak current is actually:

**Equation 13**

$$Ip_{pk}(\theta) = 4\frac{P_{in}}{V_R}\sin\theta\frac{1+K_v\sin\theta}{K_v}\left(1-\frac{1}{2R_t C_t}\frac{4Lp\,P_{in}}{K_v V_R^2}\sin\theta\right)$$

which can be derived from equations #3 and #4 in *Table 7*. As previously mentioned, if $C_t$ is selected with the criterion proposed in "*Section 4.4: Shaping capacitor ($C_t$) selection (pin CT)*", this peak is no more than 5% lower than the value provided by equation #1 in *Table 8*. The control loop easily compensates for that generating a $Vcs_{ref}(\theta)$ only slightly larger than that predicted by equation # 3 in *Table 7* by positioning the control voltage $V_{COMP}$ at a level slightly higher than that predicted by equation #1 in *Table 7*. However there is one more point to be considered and that can be clarified with the aid of *Figure 9*:

- Case a) is that of normal operation just mentioned, i.e. with $Vcs_{ref}(\theta)$ more than $\Delta Vcs_{ref}(\theta)/2$ away from $Vcs_{max}$ so that the current sense signal is entirely in its linear operation range.
- Case b) occurs when $Vcs_{ref}(\theta)$ is less than $\Delta Vcs_{ref}(\theta)/2$ away from $Vcs_{max}$; the peaks of the ripple ($Vcs_{ref}(\theta) + \Delta Vcs_{ref}(\theta)/2$) is clamped at $Vcs_{max}$. This impacts indirectly on the envelope of the valleys $Vcs_{ref}(\theta) - \Delta Vcs_{ref}(\theta)/2$ and, then, on $Ip_{pk}(\theta)$. In fact, as the peaks of the ripple start being clamped, the smoothing resistor $R_f$ has a loading effect on the ICS circuit: the current flowing through $R_f$ to the clamp is stolen from that charging $C_t$ so that the slope of the ascending ramps gets lower, whereas the descending ramps get steeper. This alters the operation of the ICS circuit and results in a $Vcs_{ref}(\theta)$ and an envelope of the valleys that are slightly flattened around the top of the sinusoid. In turn, this flattens the peak of the input current sinusoid, increasing the THD.
- Case c) occurs when the peaks of the ripple ($Vcs_{ref}(\theta) + \Delta Vcs_{ref}(\theta)/2$) not only exceed $Vcs_{max}$ with all the consequences discussed in the previous case but also the level $V_{CT_OL}$, which trips the overload protection (see "*Section 4.9: Overload and short-circuit protection (OCP function)*"). This should be the case of a real overload but note that this may occur - normally at low input voltage - even before $Vcs_{ref}(\theta)$ is clamped at $Vcs_{max}$ when $\Delta Vcs_{ref}(\theta)$ is too large (too small $C_t$ and/or too large $Rs$). This is not the case if $C_t$ is selected with the criterion proposed in "*Section 4.4: Shaping capacitor ($C_t$) selection (pin CT)*": $\Delta Vcs_{ref}(\theta)/2$ does not exceed $0.05 \cdot 1.4 = 70$ mV, while the difference $V_{CT_OL} - Vcs_{max}$ is always greater than 100 mV.

Therefore, as a conclusion, for a given $C_t$ (again, selected as per proposed criterion), if the additional distortion caused at low line by the peaks of the ripple being clamped is acceptable one can consider using the full dynamics of the current sense or nearly so, so that the value of Rs is found from:

**Equation 14**

$$Rs \le \frac{Vcs_{max_min}}{Ip_{pk_max}} = \frac{1.2}{Ip_{pk_max}}$$

If the additional distortion is to be prevented, the full dynamics needs to be reduced accordingly; then:

**Equation 15**

$$Rs \leq \frac{Vcs_{max_min}}{Ip_{pk_max}} \left(1 - \frac{2}{R_t C_t} \frac{Lp\ P_{in_max}}{K_{v_min} V_R^2}\right) \approx \frac{1.14}{Ip_{pk_max}}$$

where the last equality holds when $C_t$ is selected as per proposed criterion.

Whatever the design choice is, when designing the flyback transformer make sure that its saturation current $I_{sat}$ meets the condition:

**Equation 16**

$$I_{sat} \geq \frac{Vcs_{max_max}}{Rs} = \frac{1.4}{Rs}$$

## 4.8 Zero current detection and triggering block (pin ZCD); starter

The Zero Current Detection (ZCD) and Triggering blocks switch on the external MOSFET if a negative-going edge falling below 200 mV is applied to the ZCD pin. To do so, the triggering block must be previously armed by a positive-going edge exceeding 300 mV. The voltage at the pin is bottom limited by a clamp that holds the voltage on the pin close to zero during the ON-time of the external power switch.

This arm/trigger operation is typically used to detect transformer demagnetization for TM operation, i.e. close to the boundary between the discontinuous and the continuous conduction mode. An intentional delay $T_R$ is added to the demagnetization detection instant to make the turn-on instant as close as possible to the point where the drain ringing is at a minimum (valley switching).

The signal for the ZCD input is obtained from the transformer's auxiliary winding, typically used also to power the HVLED007. The triggering block is blanked for at least 1 µs after MOSFET's turn-off to prevent any negative-going edge that follows leakage inductance demagnetization from triggering the ZCD circuit erroneously (see "*Section 4.9: Overload and short-circuit protection (OCP function)*").

The interface between the pin and the auxiliary winding is a resistor divider. Its resistance ratio is properly chosen (see "*Section 4.10: Overvoltage protection (OVP function)*") and the upper resistance value $R_{zcd}$ is such that the current sourced by the pin during the ON-time of the power switch is within the rated capability of the internal clamp (2.5 mA):

**Equation 17**

$$R_{zcd} > 400 \frac{N_{aux}}{N_{pri}} V_{inpk_max}$$

where $N_{pri}$ and $N_{aux}$ are the primary and auxiliary turns number respectively.

At converter power-up, as the IC exits from UVLO, no signal is coming from the ZCD pin, thus an internal oscillator ("Start Timer"), which is active as long as the gate driver (pin GD) is low, sets GD high as its timeout elapses and enables the converter to start up. Switching cycles is initiated by the internal starter until the output voltage and, then, the voltage

developed by the auxiliary winding, becomes high enough to arm the ZCD triggering block and start self-triggered TM operation.

The Start Timer is invoked also whenever the IC stops during burst-mode operation (i.e. as $V_{COMP} < V_{COMP_BM}$, see "*Section 4.5: Control input for isolated feedback and optocoupler driving (pin COMP)*") or after an overvoltage detection (see "*Section 4.10: Overvoltage protection (OVP function)*") to restart switching activity.

## 4.9 Overload and short-circuit protection (OCP function)

The purpose of this function is to enable the HVLED007 to effectively control the converter when the load exceeds its maximum specified value or in case of short-circuit at the output so that no component in the power circuit is exposed to risk of failure.

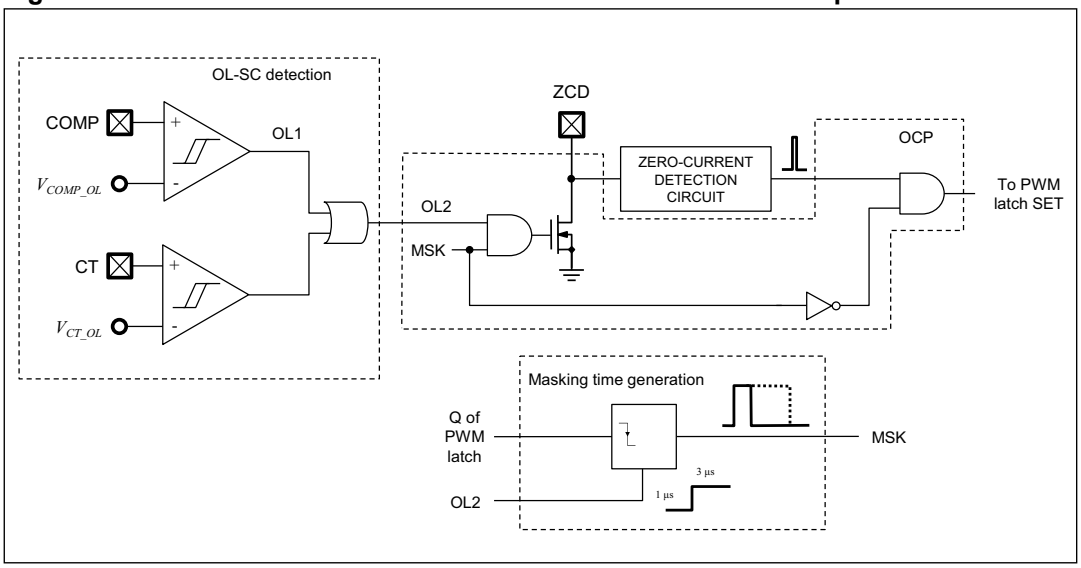
This high-level goal is met by making the converter operate intermittently under these conditions. To allow this, the low-level goal of the OCP function is to make the converter operate at the frequency of the Start Timer, so that the supply voltage of the HVLED007 cannot be kept above the UVLO threshold at all times and the IC continuously shuts down and restarts.

- Detection. Overload and short-circuit conditions (OL-SC) have a twofold detection:
  a) on pin COMP, when its voltage is over the upper end of the regulation range ($V_{COMP} > V_{COMP_OL}$);
  b) on pin CT, when its voltage $V_{Ct}$ exceeds an internal threshold $V_{CT_OL}$ (= 1.4 V).

OL-SC conditions are then detected by the logic OR of the two detection circuits.

- Corrective actions. The corrective actions aim to prevent the ringing after leakage inductance demagnetization from erroneously triggering a new switching cycle, which would result in high frequency operation under OL-SC conditions.
  Once this has been ensured, one can rely on the natural behavior of TM-operated systems, where the higher the overload, the lower the operating frequency and, therefore the power capability of the converter.
  Eventually, under short-circuit, the output voltage being too low, the ZCD circuit can no longer be armed and the converter works at the frequency of the internal Start Timer (≈3.6 kHz), with an extremely low power capability. Since under these conditions the supply voltage of the IC cannot be kept above its UVLO threshold, the IC continuously shuts down and restarts, as targeted.
  To meet this goal, a time window is generated whenever the external power MOSFET is switched off (signal MSK in the block diagram of *Figure 10*). The synch pulses coming from the ZCD circuit are blanked out during this time window.
  Normally, the duration of this time window is 1 µs but when an OL-SC is detected, it is increased to 3 µs. In addition to blanking the synch pulses coming from the ZCD circuit, during this 3 µs time window the pin ZCD is internally grounded to kill the initial spike that occurs at MOSFET turn-off and prevent the ZCD circuit from being improperly armed.

**Figure 10. Functional schematic of the overload and short-circuit protection function**




## 4.10 Overvoltage protection (OVP function)

The purpose of this function is to temporarily stop the operation of the converter in case the output voltage overshoots at start-up or as a result of a sudden load drop, exceeding a preset value.

- Detection. An overvoltage (OV) in the output voltage is sensed through the pin ZCD, which is connected via a resistor divider to the auxiliary winding in the transformer that serves both as zero current detection (to trigger a new switching cycle) and self-supply voltage generator (to power the IC). In fact, during the OFF-time of the external power MOSFET the voltage across the auxiliary winding tracks the output voltage. Tracking is acceptably good for a protection except for a short period after turn-off because strongly affected by the spike caused by the leakage inductance of the transformer and the ringing that follows its demagnetization. To prevent this noise from falsely triggering the OVP function, the detection is done by a comparator referred to a voltage reference $V_{ZCD_OVP}$ (= 5.5 V) on a filtered ZCD signal and the output of this comparator is blanked by the same signal MSK (see *Figure 10*) used in the OCP function.
  If this voltage exceeds $V_{ZCD_OVP}$, a comparator is triggered and a potential overvoltage condition is assumed. In fact, to reduce sensitivity to noise and distinguish a real failure from a disturbance (e.g. induced during ESD tests), the OVP comparator must be triggered in two consecutive switching cycles in order for the corrective actions to take place.
  More in detail: the first time the OV comparator is triggered a warning flag is set; if in the following switching cycle the OV comparator is triggered again, then the OV condition is confirmed, the corrective action takes place and the warning flag is reset; otherwise no action follows and the warning flag is reset.
- Corrective actions. When an OV condition is detected as specified above, an internal MOSFET switch is turned on, thus connecting a resistor from the pin COMP to GND. The resistor value $R_{dis}$, which matches $R_{COMP}$ (see *Table 5: Electrical characteristics*), is such that the COMP voltage is definitely taken below the burst-mode threshold. The MOSFET switch is turned off as the COMP voltage falls below the burst-mode threshold.
  The discharge switch is kept in the ON-state also when the IC is in UVLO (provided its

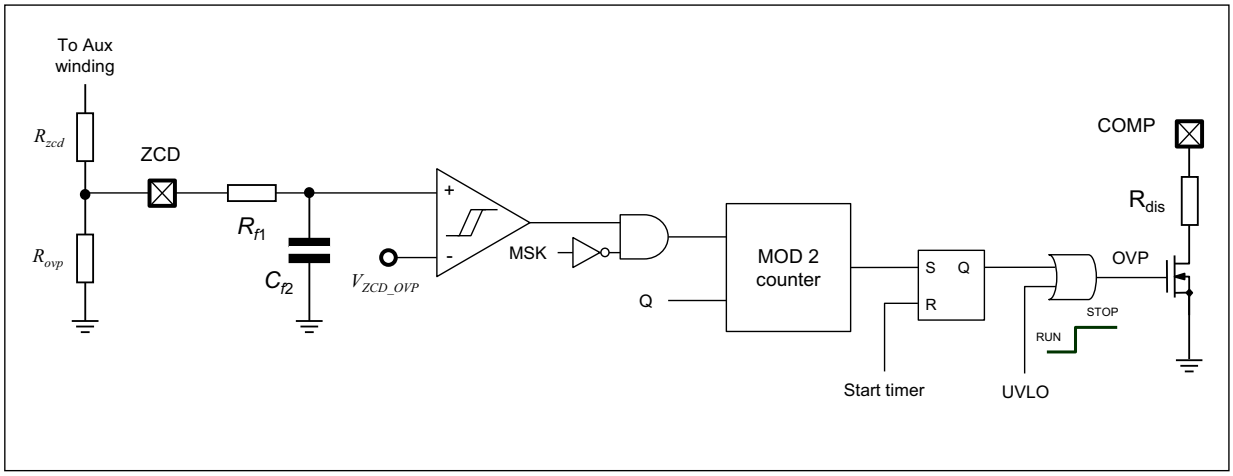
Vcc supply voltage is high enough to define its state) to reset the COMP voltage. *Figure 11* shows the functional schematic of the OVP circuit.
The OVP detection level $V_{outOVP}$ can be defined by properly selecting the lower resistor $R_{ovp}$ of the divider that connects the pin ZCD to the auxiliary winding according the formula:

**Equation 18**

$$R_{ovp} = \frac{V_{ZCD_OVP}}{\frac{N_{aux}}{N_{sec}} V_{outOVP} - V_{ZCD_OVP}} R_{zcd}$$

where $N_{sec}$ and $N_{aux}$ are the secondary and auxiliary turns number respectively. The $R_{zcd}$ value is defined by other application parameters (see "*Section 4.8: Zero current detection and triggering block (pin ZCD); starter*").

**Figure 11. Functional schematic of the OVP function**



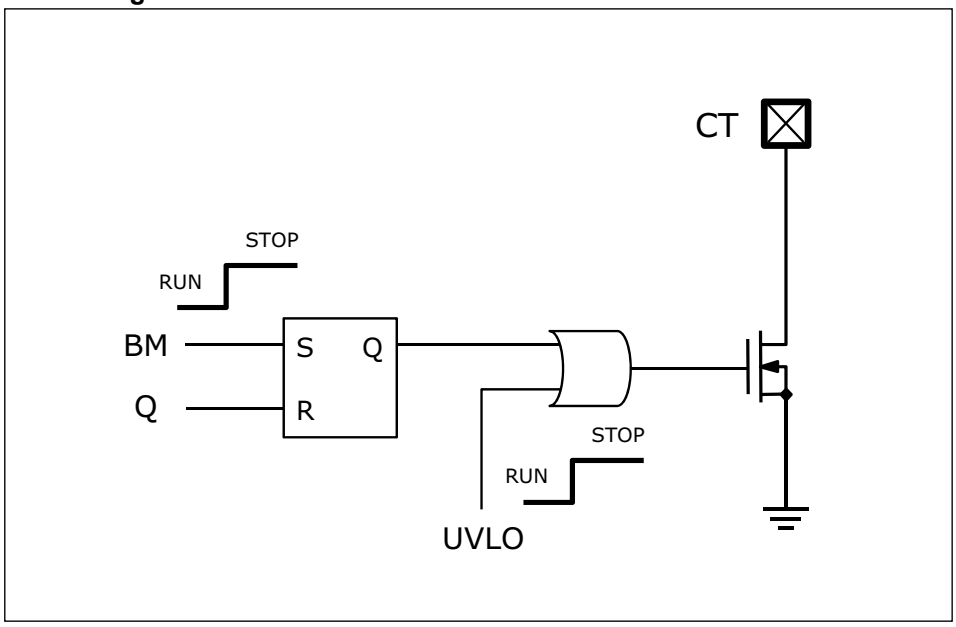

## 4.11 *Soft-restart function*

This function provides a smooth converter restart limiting the initial primary peak current whenever the IC is temporarily stopped during burst-mode operation (i.e. as $V_{COMP} < V_{COMP_BM}$, see "*Section 4.5: Control input for isolated feedback and optocoupler driving (pin COMP)*") or after an overvoltage detection (see "*Section 4.10: Overvoltage protection (OVP function)*").

This goal is met by turning on a MOSFET switch connected between pin CT and ground that discharges the external shaping capacitor $C_t$.

Firstly, the discharge switch is kept in the ON-state as long as the IC is in UVLO (provided its Vcc supply voltage is high enough to define its state) to reset the CT voltage at start-up. Secondly, the discharge switch is turned on as long as the IC is stopped and is turned off when the idle period ends and the gate-drive is turned on. The schematic of *Figure 12* shows the block diagram of the circuit implementing the above-mentioned functionality.

Figure 12. Functional schematic of the soft restart function



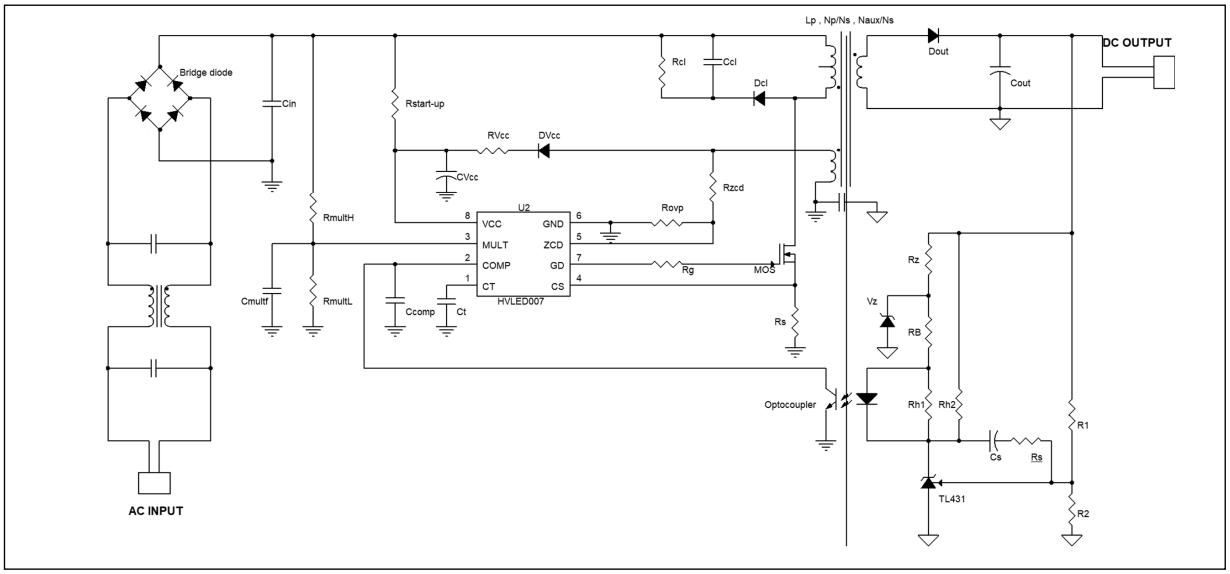

## 4.12 Suggested step-by-step design procedure of a Hi-PF QR flyback converter based on the HVLED0007

Table 9. Basic electrical specification and key parameters of a Hi-PF QR flyback

| Parameter | Symbol |
|---|---|
| Line voltage range | $V_{in_min}$ - $V_{in_max}$ |
| Line frequency range | $f_{L_min}$ - $f_{L_max}$ |
| Regulated output voltage | $V_{out}$ |
| Output overvoltage level | $V_{out_OVP}$ |
| Output current range | $I_{out_min}$ - $I_{out_max}$ |
| Maximum Vout ripple @ 2 fL_min | $\Delta V_{out_pk\text{-}pk}$ |
| Expected efficiency at full load (estimated value) | $\eta$ |
| Voltage drop on secondary rectifier (estimated value) | $V_F$ |
| Reflected voltage | $V_R$ |
| Minimum switching frequency | $f_{sw_min}$ |

The proposed design procedure can be outlined in fourteen steps, starting from the design specification detailed in *Table 9* and with reference to the typical application schematic shown in *Figure 13*.

**Figure 13. Typical application schematic (reference for suggested design procedure)**



1. Calculate peak voltages corresponding to ($V_{in_min}$ - $V_{in_max}$) and relevant $K_v$ values ($K_{v_min}$ - $K_{v_max}$). Calculate estimated maximum input power $P_{in_max}$ from max. load and estimated efficiency:

$$P_{in_max} = \frac{V_{out} I_{out_max}}{\eta}$$

2. Calculate operating conditions at $V_{in} = V_{in_min}$ and $P_{in} = P_{in_max}$ with the aid of the equations in *Table 8*, using previously calculated values of $K_{v_min}$ and $P_{in_max}$.
3. Calculate transformer's primary-to-secondary turns ratio, based on the desired $V_R$:

$$n = \frac{N_{pri}}{N_{sec}} = \frac{V_R}{V_{out} + V_F}$$

4. Calculate required primary inductance from equation #3 in *Table 6* solved for $L_p$ and with sin θ = 1, $K_v = K_{v_min}$ and $P_{in} = P_{in_max}$:

$$Lp = \frac{1}{4} \frac{V_R^2}{f_{sw_min} P_{in_max}} \left( \frac{K_{v_min}}{1 + K_{v_min}} \right)^2$$

5. Calculate first-cut value of shaping capacitor from (*Equation 10*) with *sin* θ = 1. This value might be subject to post-design changes to optimize THD of input current or adjust maximum deliverable power.
6. Pick maximum primary peak current $I_{ppk_max}$; select sense resistor *Rs* using either (*Equation 14*) or (*Equation 15*) and calculate required transformer saturation current $I_{sat}$ from (*Equation 16*).
7. Design transformer with any commonly used procedure using data calculated in steps 2 to 6.
8. Calculate worst-case voltage stress on power switch and secondary rectifier from spec data and actual primary-to-secondary turns ratio.
9. Select primary MOSFET and secondary rectifier using information on their current and voltage stress derived in steps 3 and 7.
10. Use either output voltage ripple or AC current rating, whichever gives the higher capacitance value, to select output capacitor $C_{out}$.
11. Calculate resistor divider connected to ZCD pin of HVLED007: determine $R_{zcd}$ from (*Equation 17*), then calculate $R_{ovp}$ with (*Equation 18*).
12. Determine multiplier bias gain Kp; pick a value larger than the minimum provided by (*Equation 11*).:

$$Kp \geq \frac{1.231}{V_{inpk_min} (1 + K_{v_min})}$$

check that the resulting amplitude of $V_{MULTpk}$ at $V_{in} = V_{in_max}$ does not exceed 3 V; if it does, $K_{v_min}$ needs increasing (i.e. $V_R$ needs lowering) and design should restart from step 1.

Individual values of $R_{multH}$ and $R_{multL}$ may be selected based on power consumption considerations.

13. Design clamp circuit that limits leakage inductance spikes with any commonly used procedure with data calculated in step 2.
14. Design feedback circuit and its frequency compensation according to relevant specifications (not included in *Table 9* for simplicity).

# 5 Referenced documents

1. C. Adragna, G. Gritti, "High-power-factor quasi-resonant flyback converters draw sinusoidal input current", Applied Power Electronics Conference and Exposition, 2015. APEC '15, Conference Proceedings 2015, pp. 498-505, March 2015
2. Design Equations of High-Power-Factor Flyback Converters based on the L6561. Application note AN1059

# 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com.

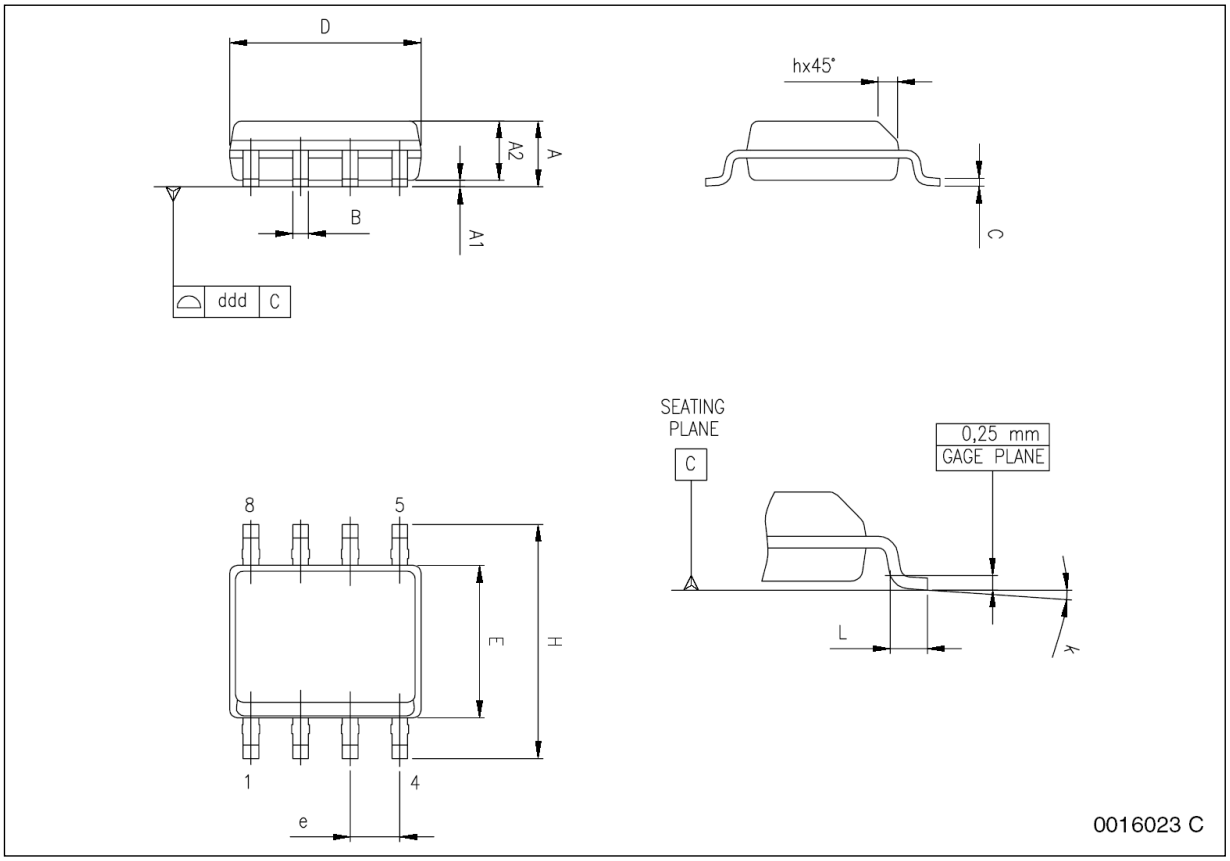
ECOPACK is an ST trademark.

**Table 10. SO-8 mechanical data**

| Dim. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 1.35 | | 1.75 | 0.053 | | 0.069 |
| | | | | | | |
| A1 | 0.10 | | 0.25 | 0.004 | | 0.010 |
| A2 | 1.10 | | 1.65 | 0.043 | | 0.065 |
| B | 0.33 | | 0.51 | 0.013 | | 0.020 |
| C | 0.19 | | 0.25 | 0.007 | | 0.010 |
| D (1) | 4.80 | | 5.00 | 0.189 | | 0.197 |
| E | 3.80 | | 4.00 | 0.15 | | 0.157 |
| e | | 1.27 | | | 0.050 | |
| H | 5.80 | | 6.20 | 0.228 | | 0.244 |
| h | 0.25 | | 0.50 | 0.010 | | 0.020 |
| L | 0.40 | | 1.27 | 0.016 | | 0.050 |
| k | 0° (min.), 8° (max.) | | | | | |
| ddd | | | 0.10 | | | 0.004 |

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

**Figure 14. Package dimensions**



# 7 Revision history

Table 11. Document history

| Date | Revision | Changes |
|---|---|---|
| 18-Jan-2019 | 1 | Initial version. |

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