Three-Channel, Closed-Loop, Switch Mode LED Driver IC with External Reset

Features

- Switch mode controller for single-switch converters
- Gate drivers optimized for driving Logic Level FETs
  - 0.25A sourcing
  - 0.5A sinking
- Typical ±2% absolute and string-to-string current accuracy (with ±1% sense resistors)
- High PWM dimming ratio
- 10-40V input range
- Constant frequency operation up to 1MHz
- On-chip clock or external clock option
- Programmable slope compensation
- Linear and PWM dimming
- Independent output short circuit protection
- Independent output over voltage protection
- Hiccup mode protection

Applications

- RGB backlight applications
- Multiple string white LED driver applications

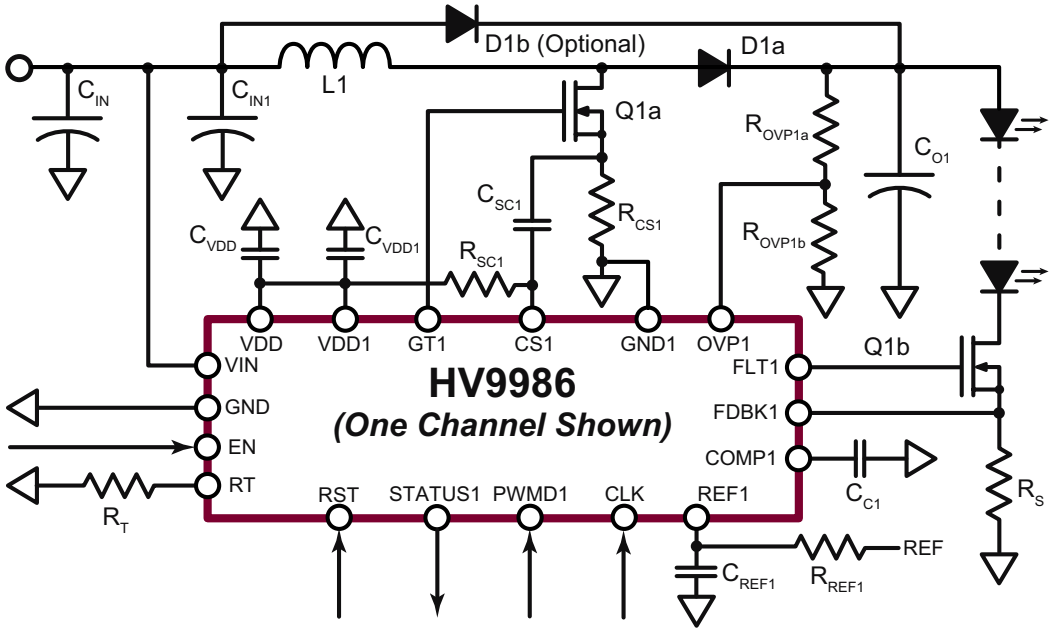
General Description

The HV9986 is a three-channel peak current mode PWM controller for driving single switch converters in a constant output current mode. It can be used for driving either RGB LEDs or multiple channels of white LEDs.

The HV9986 features a 40V linear regulator, which provides a 5V supply to power the IC. The switching frequencies of the three converters in the IC are controlled either with an external clock signal (the channels operate at a switching frequency of 1/12th of the external clock frequency) or using the internal oscillator. The three channels are positioned 120° out-of-phase to reduce the input current ripple. Each converter is driven by a peak current mode controller with output current feedback.

The three output currents can be individually dimmed using either linear or PWM dimming. The IC includes three disconnect FET drivers which enable high PWM dimming ratios, as well as to help disconnect the output in case of an output short circuit condition. HV9986 includes independent fault control for each of the channels so that a fault condition in one channel will not affect the performance of the other two. It also includes three open drain fault indicator outputs which can be used by the controlling microprocessor to reset the channel.

Typical Application Circuit



Ordering Information

Device	40-Lead QFN *6.00x6.00mm body* *1.00mm height (max)* *0.50mm pitch*
HV9986	HV9986K6-G

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

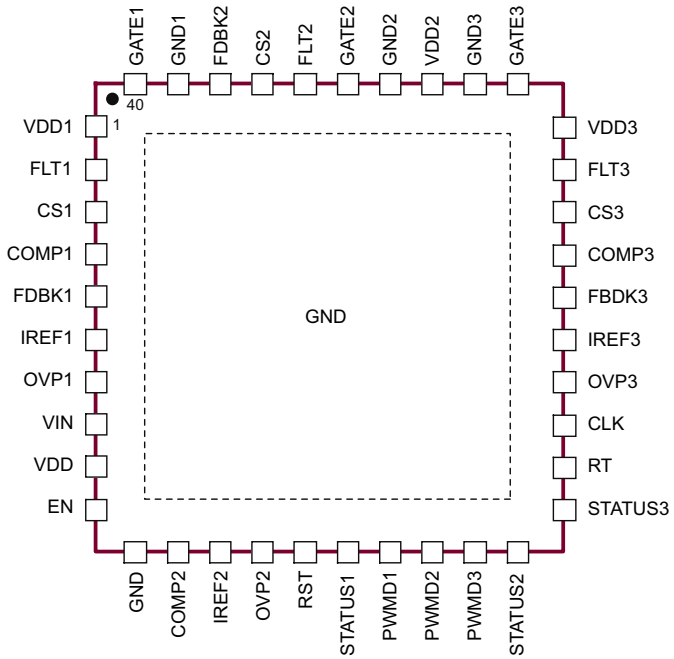
Parameter	Value
VIN to GND	-0.3V to +45V
VDD to GND, VDD 1-3 to GND	-0.3V to +6.0V
All other pins to GND	-0.3V to (V_{DD} + 0.3V)
Junction temperature	-40°C to +125°C
Storage ambient temperature range	-65°C to +150°C
Continuous power dissipation *(T_A = +25°C)*	4000mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Resistance

Package	θ_{ja}
40-Lead QFN	18°C/W

Pin Configuration



40-Lead QFN (K6)
(top view)

Product Marking



L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
= "Green" Packaging

Package may or may not include the following marks: Si or

40-Lead QFN (K6)

Electrical Characteristics *(The * denotes the specifications which apply over the full operating ambient temperature range 0°C<T_A<+85°C, otherwise the specifications are at T_A = 25°C. V_{IN} = 24V, V_{DD1} = V_{DD2} = V_{DD3} = V_{DD} unless otherwise noted.)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
Input							
V_{INDC}	Input DC supply voltage	*	10	-	40	V	DC input voltage
I_{INSD}	Shut-down mode supply current	*	-	-	200	µA	EN ≤ 0.8V
I_{IN}	Supply current	-	-	-	1.5	mA	EN ≥ 2.0V; PWMD1 = PWMD2 = PWMD3 = GND
Internal Regulator							
V_{DD}	Internally regulated voltage	*	4.75	5.00	5.25	V	V_{IN} = 10 - 40V; EN = HIGH; PWMD1-3 = V_{DD}; GATE1-3 = 1.0nF; CLK = 6.0MHz
$UVLO_{RISE}$	V_{DD} under voltage lockout threshold	-	4.25	-	4.75	V	V_{DD} rising
$UVLO_{HYST}$	V_{DD} under voltage hysteresis	-	-	250	-	mV	V_{DD} falling

\# *Denotes specifications guaranteed by design.*
* *The specifications which apply over the full operating temperature range at 0°C < T_A < +85°C are guaranteed by design and characterization.*

Electrical Characteristics *(cont.)*

*(The * denotes the specifications which apply over the full operating ambient temperature range $0^oC<T_A<+85^oC$, otherwise the specifications are at $T_A = 25^oC$. $V_{IN} = 24V$, $V_{DD1} = V_{DD2} = V_{DD3} = V_{DD}$ unless otherwise noted.)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
Enable Input							
$V_{EN(LO)}$	EN input low voltage	*	-	-	0.8	V	---
$V_{EN(HI)}$	EN input high voltage	*	2.0	-	-	V	---
R_{EN}	EN pull down resistor	-	50	100	150	kΩ	V_{EN} = 5.0V
PWM Dimming (PWMD1, PWMD2 and PWMD3)							
$V_{PWMD(lo)}$	PWMD input low voltage	*	-	-	0.8	V	---
$V_{PWMD(hi)}$	PWMD input high voltage	*	2.0	-	-	V	---
R_{PWMD}	PWMD pull down resistor	-	50	100	150	kΩ	V_{PWMD} = 5.0V
Gate (GATE1, GATE2 and GATE3)							
I_{SOURCE}	GATE short circuit current, sourcing	#	0.25	-	-	A	V_{GATE} = 0V
I_{SINK}	GATE sinking current	#	0.5	-	-	A	$V_{GATE} = V_{DD}$
T_{RISE}	GATE output rise time	*	-	-	85	ns	C_{GATE} = 2.0nF
T_{FALL}	GATE output fall time	*	-	-	45	ns	C_{GATE} = 2.0nF
D_{MAX}	Maximum duty cycle	#	-	91.7	-	%	---
Over Voltage Protection (OVP1, OVP2 and OVP3)							
$V_{OVP,rising}$	Over voltage rising trip point	*	1.13	1.25	1.37	V	OVP rising
$V_{OVP,HYST}$	Over voltage hysteresis	-	-	125	-	mV	OVP falling
Current Sense (CS1, CS2 and CS3)							
T_{BLANK}	Leading edge blanking	*	100	-	250	ns	---
T_{DELAY}	Delay to output of GATE	-	-	-	200	ns	100mV overdrive to the current sense comparator
R_{DIS}	Discharge resistance for slope compensation	*	-	-	300	Ω	GATE = Low
Internal Transconductance Opamp (Gm1, Gm2 and Gm3)							
GB	Gain bandwidth product	#	-	1.0	-	MHz	75pF capacitance at COMP pin
A_V	Open loop DC gain	-	65	-	-	dB	Output open
V_{CM}	Input common-mode range	#	-0.3	-	3.0	V	---
V_O	Output voltage range	#	-	-	V_{DD}	-	---
G_M	Transconductance	-	500	-	750	µA/V	---
V_{OFFSET}	Input offset voltage	-	-5.0	-	5.0	mV	---
I_{BIAS}	Input bias current	#	-	0.5	1.0	nA	---
R_{RATIO}	Resistor divider ratio ($\Delta V_{CS}/\Delta V_{COMP}$)	#	-	0.11	-	-	---

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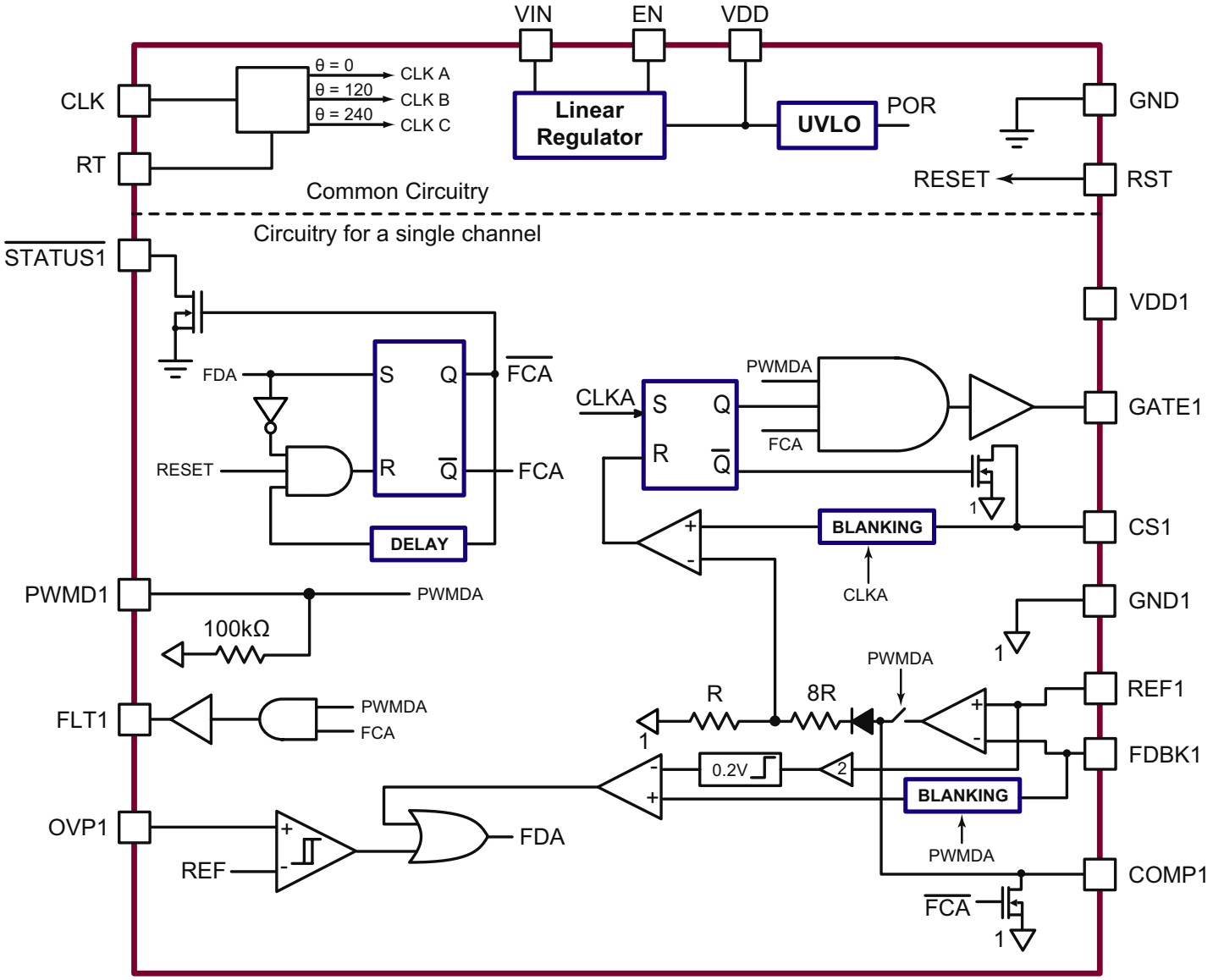
Electrical Characteristics *(cont.)* *(The * denotes the specifications which apply over the full operating ambient temperature range $0^oC<T_A<+85^oC$, otherwise the specifications are at $T_A = 25^oC$. $V_{IN} = 24V$, $V_{DD1} = V_{DD2} = V_{DD3} = V_{DD}$ unless otherwise noted.)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
External Clock Input							
f_{OSC1}	Oscillator frequency	-	-	500	-	kHz	F_{CLOCK} = 6.0MHz
K_{SW}	Oscillator divider ratio	#	-	12.0	-	-	---
$P_{HI}1$	GATE1-GATE2 phase delay	#	-	120	-	o	---
	GATE1-GATE3 phase dDelay	#	-	240	-	o	---
$T_{OFF,MIN}$	Minimum CLOCK low time	#	50	-	-	ns	---
$T_{ON,MIN}$	Minimum CLOCK high time	#	50	-	-	ns	---
$V_{CLOCK,HI}$	CLOCK input high	*	2.0	-	-	V	---
$V_{CLOCK,LO}$	CLOCK input low	*	-	-	0.8	V	---
Oscillator							
F_{osc1}	Switching frequency (common for all channels)	-	110	125	140	kHz	RT = 400kΩ
F_{osc2}	Switching frequency of the three converters (common for all channels)	-	440	500	560	kHz	RT = 100kΩ
F_{osc}	Switching frequency range	#	-	-	1000	kHz	---
Disconnect Driver (FLT1, FLT2 and FLT3)							
$T_{RISE,FAULT}$	Fault output rise time	*	-	-	300	ns	500pF capacitor at FLT pin
$T_{FALL,FAULT}$	Fault output fall time	*	-	-	200	ns	500pF capacitor at FLT pin
Short Circuit Protection (all three channels)							
$T_{BLANK,SC}$	Blanking time	*	400	-	700	ns	---
G_{SC}	Gain for short circuit comparator	-	1.85	2.0	2.15	-	---
V_{omin}	Minimum current limit threshold	-	0.15	-	0.25	V	REF = GND
T_{OFF}	Propagation time for short circuit detection	*	-	-	250	ns	FDBK = 2 • REF + 0.1V
Open Drain STATUS and RESET Pins (STATUS1,STATUS2 STATUS3, RST)							
V_{OL}	Output low voltage	-	0	-	0.3	V	I_{SINK} = 1.0mA
$V_{RESET(LO)}$	Reset input low voltage	*	-	-	0.8	V	---
$V_{RESET(HI)}$	Reset input high voltage	*	2.0	-	-	V	---
R_{RST}	Reset pull down resistor	-	50	100	150	kΩ	V_{RST} = 5.0V

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Internal Block Diagram



Functional Description

Power Topology

The HV9986 is a three-channel, switch-mode converter LED driver designed to control a boost, a buck or a SEPIC converter in a constant frequency, peak current controlled mode. The IC includes an internal linear regulator, which operates from input voltages 10 to 40V. The IC can also be powered directly using the VDD pins and bypassing the internal linear regulator. The IC includes features typically required in LED drivers like open LED protection, output short circuit protection, linear and PWM dimming, and accurate control of the LED current.

Each channel of the IC is independent of the other channels and a fault on one channel will not affect the performance of the other two channels. There is no built-in hiccup timer, but the fault channel can be reset with an external reset signal. This allows the user full control over the behavior of the fault condition enabling intelligent control of the three channels using an external microcontroller.

The IC is ideally suited for backlight application using either RGB or multi-channel white LED configurations.

Power Supply to the IC (VIN, VDD, VDD1-3)

The HV9986 can be powered directly from its VIN pin that takes a voltage up to 40V. When a voltage is applied at the VIN pin, the HV9986 tries to maintain a constant 5.0V (typ.) at the VDD pin. The regulator also has a built in under-voltage lockout which shuts the IC off if the voltage at the VDD pin falls below the UVLO threshold. By connecting this VDD pin to the individual VDD pins of the three channels, the internal regulator can be used to power all three channels in the IC.

In case the internal regulator is not utilized, an external power supply (5.0V +/ 10%) can be used to power the IC. In this case, the power supply is directly connected to the VDD pins and the VIN pin.

All four VDD pins must by bypassed by a low ESR capacitor (≥0.1µF) to provide a low impedance path for the high frequency current of the output gate driver. These capacitors must be referenced to the individual grounds for proper noise rejection (see Layout Guidelines section for more information). Also, in all cases, the four VDD pins must be connected together externally.

The input current drawn from the external power supply (or VIN pin) is a sum of the 1.0mA (max) current drawn by the all the internal circuitry (for all three channels) and the current drawn by the gate drivers (which in turn depends on the switching frequency and the gate charge of the external FET).

$$I_{IN} = 1mA + (Q_{G1} + Q_{G2} + Q_{G3}) \bullet f_S$$

In the above equation, f_S is the switching frequency of the converters and Q_{G1-3} are the gate charges of the external FETs (which can be obtained from the FET datasheets).

The EN pin is a TTL compatible input used to disable the IC. Pulling the EN pin to GND will shut down the IC and reduce the quiescent current drawn by the IC to be less than 200µA. If the enable function is not required, the EN pin can be connected to VDD.

Clock Input (CLK)

The switching frequency of the converters can be set in one of two ways. One way to set the switching frequency is to use the on-chip oscillator using a resistor at the RT pin. In this case, the CLK pin should be connected to GND. If the on-chip clock is used, two or more HV9986s cannot be synchronized to each other.

The other way to is set the switching frequency by using a TTL compatible square wave input at the CLK pin. The switching frequencies of the three converters will be 1/12th the frequency of the external clock. By using the same clock for multiple ICs, all the ICs can be synchronized together. In this case, the RT pin can be either left open or connected to VDD.

Current Sense (CS1-3)

The current sense input is used to sense the source current of the switching FET. Each CS input of the HV9986 includes a built-in 100ns (minimum) blanking time to prevent spurious turn off due to the initial current spike when the FET turns on.

The IC includes an internal resistor divider network, which steps down the voltage at the COMP pins by a factor of 9. This voltage is used as the reference for the current sense comparators. Since the maximum voltage of the COMP pin is approximately V_{DD}, this voltage determines the maximum reference current for the current sense comparator and thus the maximum inductor current.

The current sense resistor R_{CS} should be chosen so that the input inductor current is limited to below the saturation current level of the input inductor. For discontinuous conduction mode of operation, no slope compensation is necessary. In this case, the current sense resistor is chosen as:

$$R_{CS} = \frac{V_{DD} - 1V}{9 \bullet I_{L,PK}}$$

where $I_{L,PK}$ is the peak inductor current.

For continuous conduction mode converters operating in the constant frequency mode, slope compensation becomes necessary to ensure stability of the peak current mode controller, if the operating duty cycle is greater than 50%. This factor must also be accounted for when determining R_{CS} (see Slope Compensation section).

Slope Compensation

Choosing a slope compensation which is one half of the down slope of the inductor current ensures that the converter will be stable for all duty cycles.

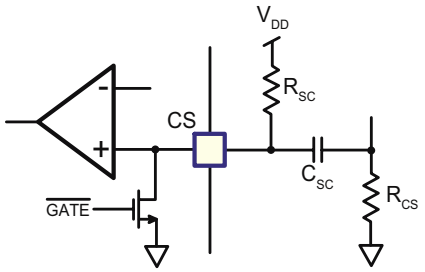


Fig. 1. Slope Compensation

Slope compensation in the HV9986 can be programmed by two external components (see Fig. 1). A resistor for VDD sets a current (which is almost constant since the VDD voltage is much larger than the voltage at the CS pin). This current flows into the capacitor and produces a ramp voltage across the capacitor. The voltage at the CS pin is then the sum of the voltage across the capacitor and the voltage across the current sense resistor, with the voltage across the capacitor providing the required slope compensation. When the GATE turns off, an internal pull down FET discharges the capacitor. The 300Ω resistance of the internal FET will prevent the voltage at the CS pin from going all the way to zero. The minimum value of the voltage will instead be:

$$V_{CS,MIN} = \frac{V_{DD}}{R_{SC}} \bullet 300\Omega$$

The slope compensation capacitor is chosen so that it can be completely discharged by the internal 300Ω FET at the CS pin during the time the FET is off. Assuming the worst case switch duty cycle of 92%,

$$C_{SC} = \frac{0.08}{3 \bullet 300\Omega \bullet f_S}$$

Assuming a down slope of DS (A/µs) for the inductor current, the current sense resistor and the slope compensation resistor can be computed as:

$$R_{CS} = \frac{V_{DD} - 1}{9} \bullet \frac{1}{\left[\frac{DS \bullet 10^6 \bullet 0.92}{2 \bullet f_S}\right]} + I_{L,PK}$$

$$R_{SC} = \frac{2 \bullet V_{DD}}{DS \bullet 10^6 \bullet C_{SC} \bullet R_{CS}}$$

where $I_{L,PK}$ is the peak inductor current.

Control of the LED Current

The LED currents in the HV9986 are controlled using three independent current feedbacks. The reference voltages which set the three LED currents are provided at each REF pin (REF1-3). These reference voltages are compared to the voltage from the LED current sense resistors at the corresponding FDBK pins (FDBK1-3). HV9986 includes three 1MHz transconductance amplifiers with tri-state output, which are used to close the feedback loops and provide accurate current control. The compensation networks are connected at the COMP pins (COMP1-3).

The output of each op-amp is buffered and connected to the current sense comparators using an 8R:1R divider.

The outputs of the op-amps are controlled by the signal applied to the PWMD pins (PWMD1-3). When PWMD is high, the output of the opamp is connected to the COMP pin. When PWMD is low, the output is left open. This enables the integrating capacitor to hold the charge when the PWMD signal is low, and the gate driver output (GATE1-3) is off. When the IC is enabled, the voltage on the integrating capacitor will force the converter into steady state almost instantly.

Linear Dimming

Linear Dimming can be accomplished in the HV9986 by varying the voltages at the REF pins. Since the HV9986 is a peak current mode controller, it has a minimum on-time for the GATE outputs. This minimum on-time will prevent the converters from completely turning off even when the REF pins are pulled to GND. Thus, linear dimming cannot accomplish true zero LED current. To get zero LED current PWM dimming has to be used. Different signals can be connected to the three REF pins if desired, and these inputs need not be connected together.

Due to the offset voltage of the short circuit comparator as well as the non-linearity of the X2 gain stage, pulling the REF pin very close to GND would cause the internal short circuit comparator to trigger and shut down the IC. To overcome this, the output of the gain stage is limited to 125mV

(minimum), allowing the REF pin to be pulled all the way to 0V without triggering the short circuit comparator.

PWM Dimming

PWM dimming in the HV9986 can be accomplished by using TTL compatible square wave sources at the PWMD pins (PWMD1-3). All three channels can be individually PWM dimmed as desired.

When the PWM signal is high, the GATE and FLT pins are enabled and the output of the transconductance opamp is connected to the external compensation network. Thus, the internal amplifier controls the output current. When the PWMD signal goes low, the output of the transconductance amplifier is disconnected from the compensation network. Thus, the integrating capacitor maintains the voltage across it. The GATE is disabled, so the converter stops switching, and the FLT pin goes low, turning off the disconnect switch.

The output capacitor of the converter determines its PWM dimming response, since it has to get charged and discharged whenever the PWMD signal goes high or low. In the case of a buck converter, since the inductor current is continuous, a very small capacitor is used across the LEDs. This minimizes the effect of the capacitor on the PWM dimming response of the converter. However, in the case of a boost converter, the output current is discontinuous and a large output capacitor is required to reduce the ripple in the LED current. Thus, this capacitor will have a significant impact on the PWM dimming response. By turning the disconnect switch off when PWMD goes low, the output capacitor is prevented from being discharged, and thus the PWM dimming response of the boost converter Improves dramatically.

Note that disconnecting the LED load during PWM dimming causes the energy stored in the inductor to be dumped into the output capacitor. The filter capacitor should be chosen large enough so that it can absorb the inductor energy without significant change of the voltage across it.

Fault Conditions

The HV9986 is a robust controller which can protect the LEDs and the LED driver in case of fault conditions. The outputs of the HV9986 LED driver are protected from both an open and a short LED condition. In both cases, the HV9986 shuts down the channel with the fault and reports a fault condition to the controlling microprocessor. The microprocessor then attempts to restart the channel by providing a reset signal to the HV9986. This process does not interfere with the normal behavior of the other channels.

When a fault condition is detected, both GATE and FLT outputs are disabled, the COMP pin is pulled to GND. The corresponding STATUS pin of the channel with the fault is pulled low to indicate a fault condition. The external microprocessor can then attempt to restart the channel by applying a pulse at the RST pin. It is necessary to ensure that the time between the STATUS pin going low and the pulse being applied at the RST pin is long enough to ensure that the compensation networks are all completely discharged and that the converters start at minimum duty cycle.

Output Short Circuit Protection

When a short circuit condition is detected (output current becomes higher than twice the steady state current), the GATE and FLT outputs are disabled, the COMP pin is pulled to GND and the STATUS pin is pulled low. As soon as the disconnect FET is turned off, the output current goes to zero and short circuit condition disappears. The channel is now ready to be reset. Note that at this point, the output capacitor is charged to almost the full output voltage.

When a reset pulse is applied to the RST pin, the converter turns on almost immediately. If there is a persistent short circuit, the IC detects a short circuit and shuts off. The time between the rising edge of the rest pulse and the next shutdown of the channel (due to a persistent short circuit) is typically about 50ns – 500ns and depends on the gate capacitance of the disconnect FET. A long reset pulse would immediately cause the HV9986 to reset causing the channel to toggle between ON and OFF states at very high frequencies as long as the RST pin is held high. This might damage the disconnect FET as well as the LED sense resistor due to the large power dissipation.

To avoid this condition, it is recommended that upon the detection of a fault condition, the respective channel's PWM dimming signal be set to 0% and once the IC is reset (and the reset pulse is complete), the PWM dimming signal be slowly ramped up from 0%.

Hiccup Time Computation

During short circuit conditions, there are two factors that determine the hiccup time.

The first is the time required to discharge the compensation capacitors. Assuming a pole-zero R-C network at the COMP pin (series combination of R_Z and C_Z in parallel with C_C),

$$t_{COMP,n} = 3 \cdot R_{Zn} \cdot C_{Zn}$$

where n refers to the channel number.

In case the compensation networks are only of Type 1 (single capacitor), then:

$$t_{COMP,n} = 3 \cdot 300\Omega \cdot C_{Zn}$$

Thus, the maximum COMP discharge time required can be computed as:

$$t_{COMP,MAX} = max\ (t_{COMP1},\ t_{COMP2},\ t_{COMP3})$$

The second factor is the time required for the inductors to discharge completely after the short circuit condition has been cleared. This time can be computed as:

$$t_{IND,n} = \frac{\pi}{4}\sqrt{L_n \bullet C_{On}}$$

where L and C_O are the input inductor and output capacitor of each power stage.

Thus, the maximum time required for the inductors to discharge can be computed as:

$$t_{IND,MAX} = max\ (t_{IND1},\ t_{IND2},\ t_{IND3})$$

During an over voltage condition, the hiccup time required can be computed as:

$$t_{OVP} = -(R_{OVPA,n} + R_{OVPB,n}) \bullet Cn \bullet ln(V_{LED}/V_{OVP})$$

Where V_{OVP} is the output voltage where the OVP condition is triggered and V_{LED} is the minimum LED string voltage.

The hiccup time is then chosen as:

$$t_{HICCUP} > max\ (t_{COMP,MAX},\ t_{IND,MAX},\ t_{OVP})$$

Note that the STATUS pin just indicates a fault condition and does not distinguish between an open LED or a short circuit fault. Thus, the hiccup time needs to be the larger of short circuit hiccup time and the open LED hiccup time.

False Triggering of the Short Circuit Comparator During PWM Dimming

During PWM dimming, the parasitic capacitance of the LED string causes a spike in the output current when the disconnect FET is turned on. If this spike is detected by the short circuit comparator, it will cause the IC to falsely detect an over current condition and shut down.

In the HV9986, to prevent these false trigger events, a built-in 500ns blanking network for the short circuit comparator is included. This blanking network is activated when the PWMD input goes high. Thus, the short circuit comparator will not see the spike in the LED current during the turn-on transition of the PWM Dimming. Once the blanking time is over, the short circuit comparator will start monitoring the output current. Thus, the total delay time for detecting a short circuit will depend on the condition of the PWMD input.

If the output short circuit exists before the PWM dimming signal goes high, the total detection time will be:

$$t_{DETECT1} = t_{BLANK} + t_{DELAY} \approx 900ns(max)$$

If the short circuit occurs when the PWM dimming signal is already high, the time to detect will be:

$$t_{DETECT1} = t_{DELAY} \approx 200ns(max)$$

Layout Considerations

For multi-channel peak current mode controller IC to work properly with minimum interference between the channels, it is important to have a good PCB layout which minimizes noise. Following the layout rules stated below will help to ensure proper performance of all three channels.

1. **GND Connection**
   The IC has four separate ground connections - one for each of the three channels and one analog ground for the common circuitry. It is recommended that four separate ground planes be used in the PCB, and all the GND planes be connected together at the return terminal of the input power lines.

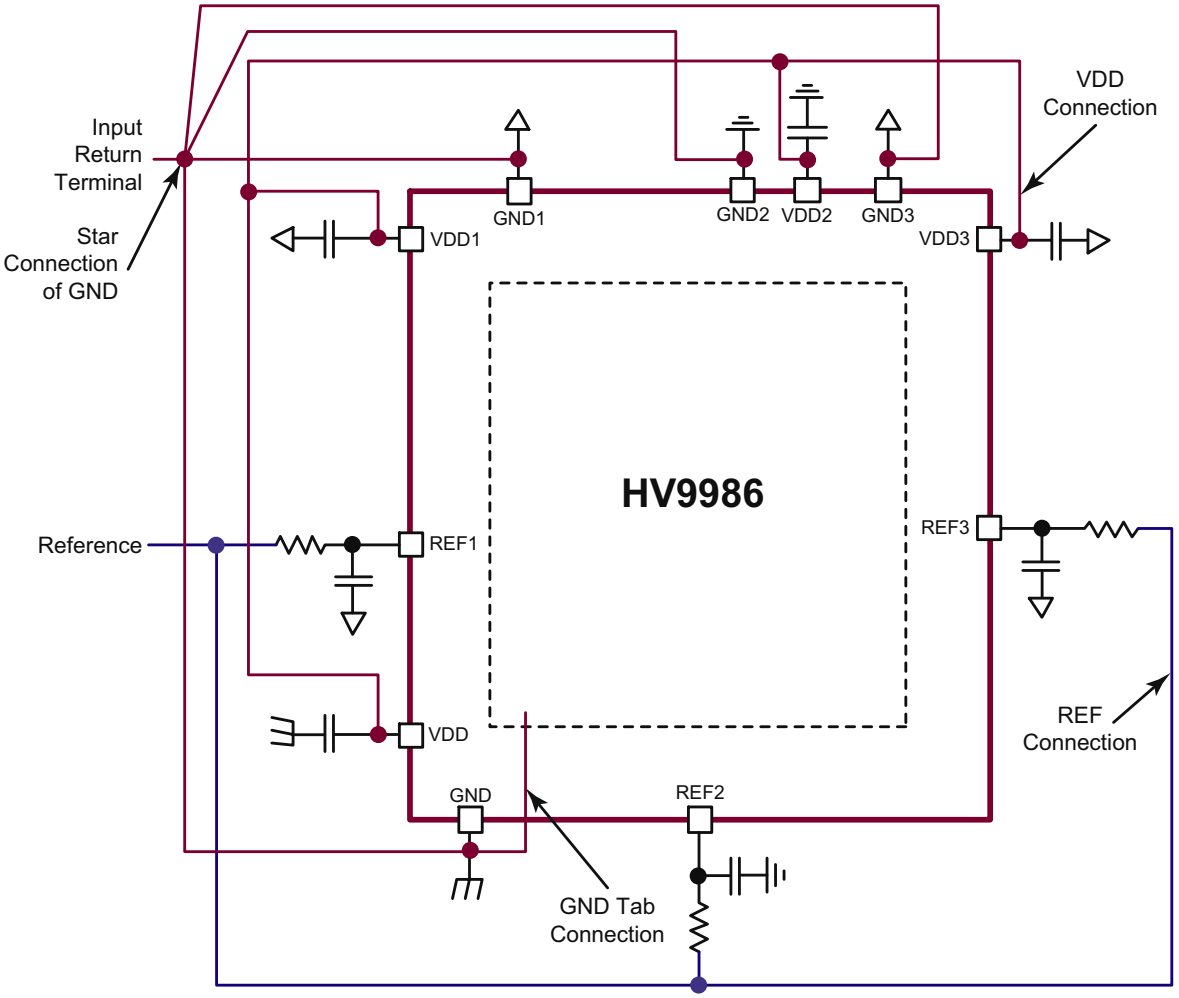
2. **VDD Connection**
   Each VDD pin should be bypassed with a low ESR capacitor to its OWN ground (i.e. VDD1 is bypassed to GND1 and so on). The common VDD pin can be bypassed to the common GND.

3. **REF Connection**
   In case all the references are going to be driven from a single voltage source, it is recommended to have a small R-C low pass filter (1.0k, 1.0nF) at each REF pin with the filter being referenced to the appropriate channel's ground (as in the case of the VDD pins). If the REF pins are driven with three individual voltage sources, then just a small capacitor (1.0nF) at each pin would suffice.

4. **GATE and CS connection**
   The connection from GATE output to the gate of the external FET as well as the connection from the CS pin to the external sense resistor made as short as possible to avoid false trigerrings.

5. **OVP protection**
   Typically, the OVP resistor dividers would be located away from the IC. To prevent false trigerring of the IC due to noise at the OVP pin, a small bypass capacitor (1.0nF) right at the OVP pin is recommended.

Layout Guidelines



Pin Description

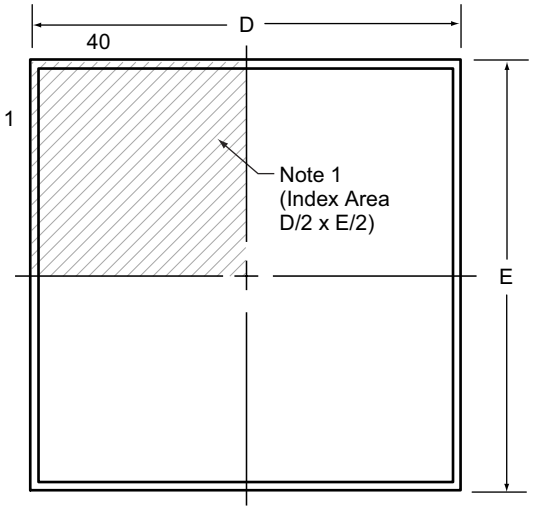
Pin #	Name	Description
1	VDD1	These pins are the power supply pins of the three channels. They can either be connected to the VDD pin or supplied with an external power supply. They must be bypassed with a low ESR capacitor to their respective GNDs (at least 0.1µF). All VDD pins (VDD, VDD1-3) must be connected together externally. An external 5V supply can be connected to these pins to power the IC if the internal regulator is not used.
33	VDD2	
30	VDD3	
2	FLT1	These pins are used to drive external logic-level disconnect switches. The disconnect switches are used to protect the LEDs in case of fault conditions and also serve to provide excellent PWM dimming response by disconnecting and reconnecting the LEDs from the output capacitor during PWM dimming.
36	FLT2	
29	FLT3	
3	CS1	These pins are used to sense the source current of the external power FETs. They include a built-in 100ns (min) blanking timer. Connecting an RC-network at these pins programs the slope compensation. Refer to the Slope Compensation section for additional information.
37	CS2	
28	CS3	
4	COMP1	Stable closed loop control can be accomplished by connecting a compensation network between each COMP pin and its respective GND.
12	COMP2	
27	COMP3	
5	FDBK1	These pins are the output current feedback inputs for each channel. They receive voltage signal from external sense resistors.
26	FDBK2	
38	FDBK3	
6	REF1	The voltages at these pins set the output current level for each channel. Recommended voltage range for these pins is 0V – 1.25V.
13	REF2	
25	REF3	
7	OVP1	These pins provide the over voltage protection for the three channels. When the voltage at any of these pins exceeds 1.25V, the HV9986 is turned off. The fault channel cannot be reset until the voltage drops below 1.125V.
14	OVP2	
24	OVP3	
8	VIN	Input of the internal 40V linear regulator.
9	VDD	This pin is the output of the linear regulator. It maintains a regulated 5.0V as long as the voltage of the VIN pin is between 10V and 40V. It must be bypassed with a low ESR capacitor to GND (at least 0.1µF). This pin can be used as a power supply for the three channels.
10	EN	When the pin is pulled below 0.8V, then IC goes into a standby mode and draws minimal current.
11	GND	Ground connection for the common circuitry in the HV9986.
15	RST	This pin is used to reset the fault channel using an external TTL compatible signal.
16	STATUS1	These open drain pins are used to indicate a fault on a particular channel.
20	STATUS2	
21	STATUS3	
17	PWMD1	PWM dimming of the three channels is accomplished by using the PWMD pins. The three pins directly control the PWM dimming of the three channels and a square wave input should be applied at these pins
18	PWMD2	
19	PWMD3	

Pin Description *(cont.)*

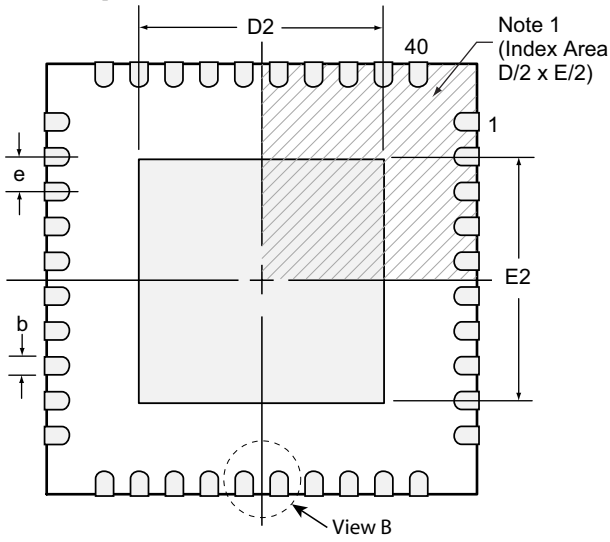
Pin #	Name	Description
22	RT	A resistor at this pin programs the on-board oscillator. If an external clock is being used, this pin should be connected to VDD.
23	CLK	This pin is the clock input for the HV9986. The input to the CLK pin should be a TTL compatible square wave signal. The three channels will switch at 1/12th the switching frequency of the signal applied at the CLK pin. This pin is used if more than one HV9986's are being used in a system. If the on-chip oscillator is being used, this pin should be connected to GND.
31	GATE3	These pins are the gate drivers which drive the external logic-level, N-channel boost converter MOSFETs.
35	GATE2	
40	GATE1	
32	GND3	Ground return for each of the channels. It is recommended that all the GNDs of the IC be connected together in a STAR connection at the input GND terminal to ensure best performance.
34	GND2	
39	GND1	

40-Lead QFN Package Outline (K6)

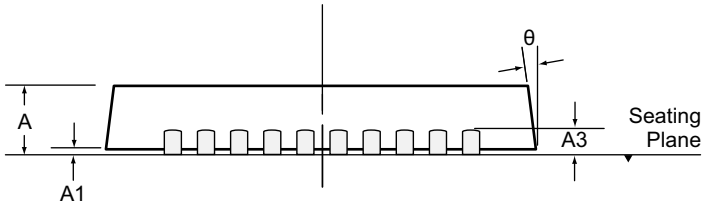
6.00x6.00mm body, 1.00mm height (max), 0.50mm pitch



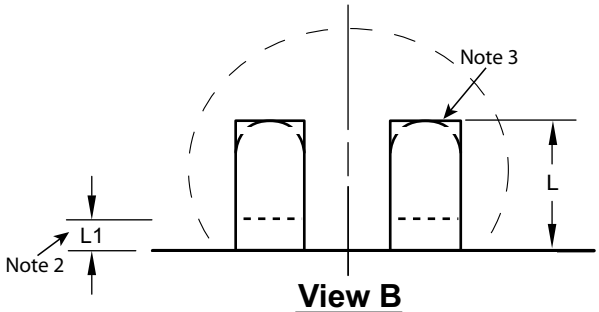
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ°
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	5.85*	1.05	5.85*	1.05	0.50 BSC	0.30†	0.00	0
	NOM	0.90	0.02		0.25	6.00	-	6.00	-		0.40†	-	-
	MAX	1.00	0.05		0.30	6.15*	4.45	6.15*	4.45		0.50†	0.15	14

JEDEC Registration MO-220, Variation VJJD-6, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc. #: *DSPD-40QFNK66X6P050, Version C041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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