HT9030

Calling Line Identification Receiver

Features

- BELL 202 FSK demodulation
- Ring detection input and output
- Carrier detection output
- Low battery detection input and output
- Power down mode
- High input sensitivity
- 3.58MHz crystal or ceramic resonator

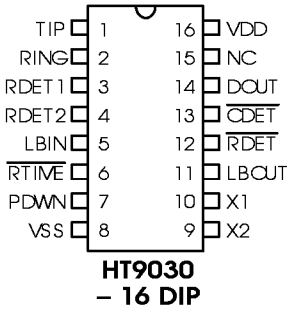
Applications

- Feature phones
- Adjunct boxes
- Fax and answering machines
- Computer interface products

General Description

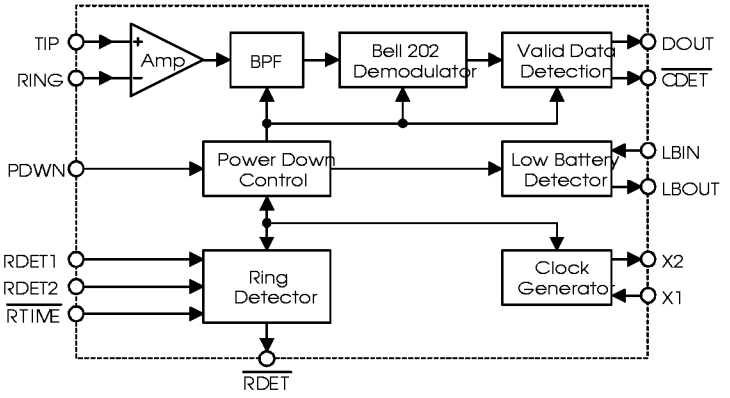
The HT9030 calling line identification receiver is a low power CMOS integrated circuit designed for receiving physical layer signals transmitted according to Bellcore TR-NWT-000030 specifications. The primary application for this device is in products that are to be used to receive and display the calling number, or message waiting indicator sent to subscribers from central office facilities. The device also provides a low battery detection circuit, a power down circuit, a carrier detection circuit and a ring detection circuit for easier system applications.

Package Information



HT9030
– 16 DIP

Block Diagram



Pin Description

Pin No.	Pin Name	I/O	Description
1	TIP	I	This input pin is connected to the tip side of the twisted pair wires. It is internally biased to 1/2 VDD when the device is in power up mode. This pin must be DC isolated from the line.
2	RING	I	This input pin is connected to the ring side of the twisted pair wires. It is internally biased to 1/2 VDD when the device is in power up mode.This pin must be DC isolated from the line.
3	RDET1	I	It detects ring energy on the line through an attenuating network and enables the oscillator and ring detection.
4	RDET2	I	It couples ring signal to the precision ring detector through an attenuating network. $\overline{\text{RDET}}$="0" if a valid ring signal is detected.
5	LBIN	I	Input for low battery detector
6	$\overline{\text{RTIME}}$	O	An RC network may be connected to this pin in order to hold this pin voltage below 2.2V between the peaks of the ringing signal. This pin controls internal power up and activates partial circuitry needed to determine whether the incoming ring is valid or not.
7	PDWN	I	A logic "1" on this pin puts the chip in power down mode. When a logic "0" is on this pin, the chip is activated.
8	VSS	—	Power supply ground
9	X2	O	A 3.58MHz crystal or ceramic resonator should be connected to this pin and X1.
10	X1	I	A 3.58MHz crystal or ceramic resonator should be connected to this pin and X2.
11	LBOUT	O	This pin will be set to "1" when the voltage on LBIN pin is lower than the internal reference voltage. Otherwise this pin stays at "0".
12	$\overline{\text{RDET}}$	O	This open drain output goes low when valid ringing signal is detected. When connected to PDWN pin, this pin can be used for auto power up.
13	$\overline{\text{CDET}}$	O	This open drain output goes low indicating that a valid carrier is present on the line. An hysteresis is built-in to allow for a momentary drop out of the carrier. When connected to PDWN pin, this pin can be used for auto power up.
14	DOUT	O	This pin presents the output of the demodulator whenever $\overline{\text{CDET}}$ pin is low. This data stream includes the alternate "1" and "0" pattern, and the 150ms of marking,which precedes the data. At all other times, this pin is held high.
15	NC	—	No connect
16	VDD	—	Positive power supply

Absolute Maximum Ratings

Voltages referenced to VSS, except where noted.

DC Supply Voltage.....-0.5V to 6.0V
Power Dissipation.....25mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range .....–40°C to 150°C

Electrical Characteristics

(Crystal=3.58MHz, Ta=0~70°C unless otherwise noted)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	DC Supply Voltage	5V	—	3.5	5	5.5	V
I_{STBY}	Stand-by Current	5V	PDWN=1, $\overline{RTIME}$=1 All outputs unloaded	—	—	1	μA
I_{DD1}	Operating Current	5V	PDWN=1, $\overline{RTIME}$=0 All outputs unloaded	—	1	—	mA
I_{DD2}	Operating Current	5V	PDWN=0, $\overline{RTIME}$=0 or 1, All outputs unloaded	—	2.5	—	mA
V_{IL}	Input Low Voltage	5V	—	—	—	$0.2V_{DD}$	V
V_{IH}	Input High Voltage	5V	—	$0.8V_{DD}$	—	—	V
I_{OL}	Output High Sourcing Current	5V	$V_{OH}=0.9V_{DD}$	0.8	—	—	mA
I_{OH}	Output Low Sinking Current	5V	$V_{OL}=0.1V_{DD}$	2	—	—	mA
I_{IN}	Input Leakage Current	5V	—	—	—	±1	μA
V_{T-}	Input Low Threshold Voltage	5V	—	—	2.2	—	V
V_{T+}	Input High Threshold Voltage	5V	—	—	2.9	—	V
V_{RD2}	RDET2 Threshold Voltage	5V	—	—	1.2	—	V
R_{IN}	Tip/Ring Input DC Resistance	5V	—	—	500	—	KΩ
R_{LBIN}	Pull Low Resistance on pin LBIN	5V	(see fig-1)	—	91	—	KΩ
Vref	Internal Reference Voltage	5V	(see fig-1)	—	1.2	—	V
fosc	Operating Frequency	5V	—	—	3.58	—	MHz

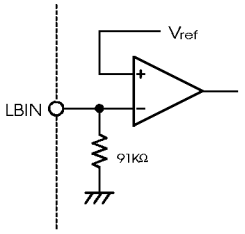


fig-1

Analog Characteristics

V_{DD}=5V, V_{SS}=0V, Crystal=3.58MHz, Ta=0 to 70°C, 0dBm=0.7746Vrms@600Ω

Characteristics		Min.	Typ.	Max.	Unit
Input Sensitivity: Tip and Ring		—	–40	—	dBm
Band Pass Filter Frequency Response (Relative to 1700Hz @ 0dBm)	60Hz 1200Hz 2200Hz 5000Hz ≥10000Hz	—	–54 0 +1 –19 –35	—	dB
Carrier Detect ON Sensitivity		—	–52	–48	dBm
Carrier Detect OFF Sensitivity		—	–55	—	dBm

Switching Characteristics

V_{DD}=5V, V_{SS}=0V, Crystal=3.58MHz, Ta=25°C, C_L=50pF

Symbol	Description	Min.	Typ.	Max.	Unit
T_{DOSC}	Oscillator Startup	—	2	—	ms
T_{SUPD}	Power Up to Decode FSK (Set Up Time)	—	8	—	ms
T_{DAQ}	Carrier Detect Acquisition Time	—	7	—	ms
T_{DCH}	End of Data to Carrier Detect High	—	9	—	ms

Timing Diagram

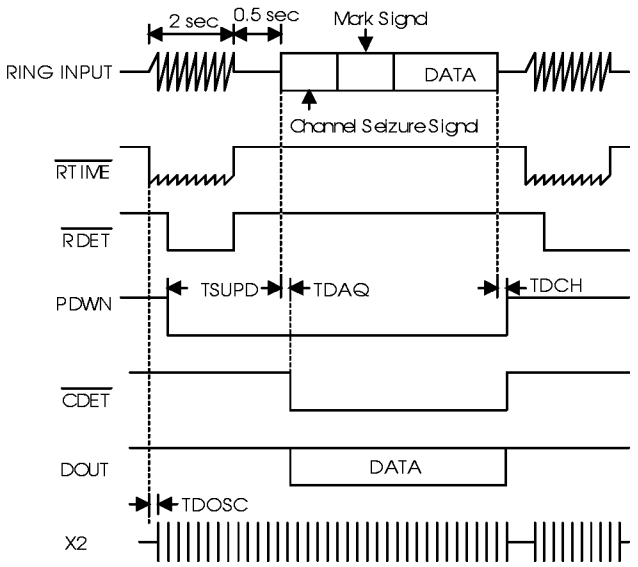


fig-2

Note:

The HT9030 is only a CLID receiver for receiving the physical layer FSK signals. The higher layers of data transmission, data link layer and message assembly layer, are well defined in TR-NMT-000030 and TR-NMT-00031. Please refer to these two documents for more details about the higher layer protocols.

Application Circuit

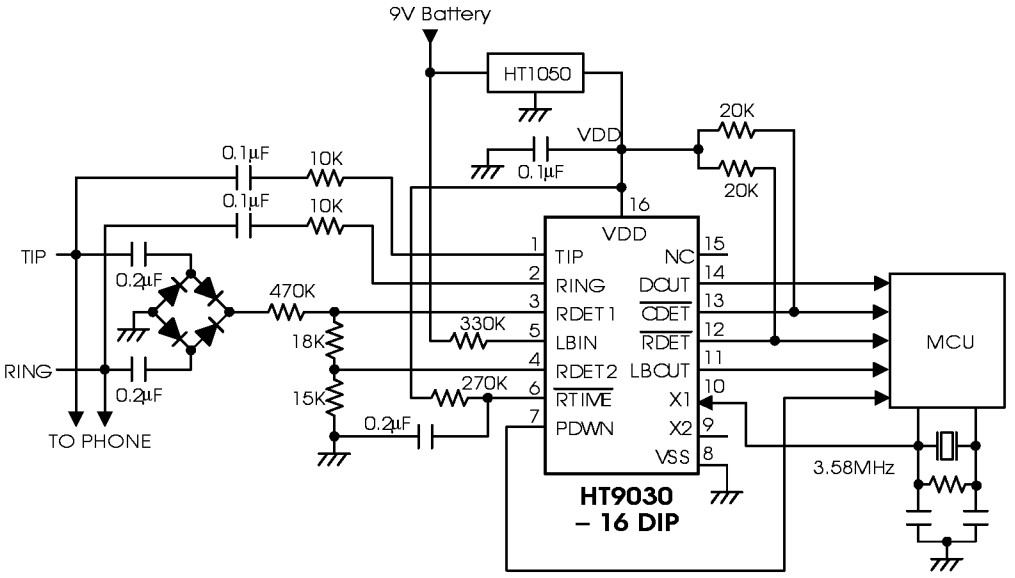


fig-3