Features

- Integrated Transition Mode (TM) PFC controller and Quasi-Resonant (QR) flyback controller
- Wide AC input range from $85V_{AC}$ to $265V_{AC}$
- Integrated 650V JFET quick high voltage start-up
- Integrated THD PFC stage optimiser
- Brown-out and brown-in protection
- Internal accurate feedback reference voltage: ±2%
- Internal 9.6ms PWM soft-start
- High/Low line over-power compensation
- FB pin protection (Auto Recovery)
  - Over-power and overload protection
  - Short-circuit protection
  - Open-loop protection
- External triggering and adjustabe over-temperature protection – RT Pin
- VCC pin OVP – latched
- Internal over-temperature shutdown – 140°C
- 16-pin NSOP package

Applications

- AC/DC NB adapters
- Open-frame SMPS
- Battery chargers
- General LED lighting applications
- Industrial, commercial, and residential fixtures

General Description

The HT7L5820/HT7L5821 is highly integrated device which includes a Power Factor Correction controller and quasi-resonant flyback controller. The high level of functional integration provides the means for very cost-effective designs with a minimum of external components.

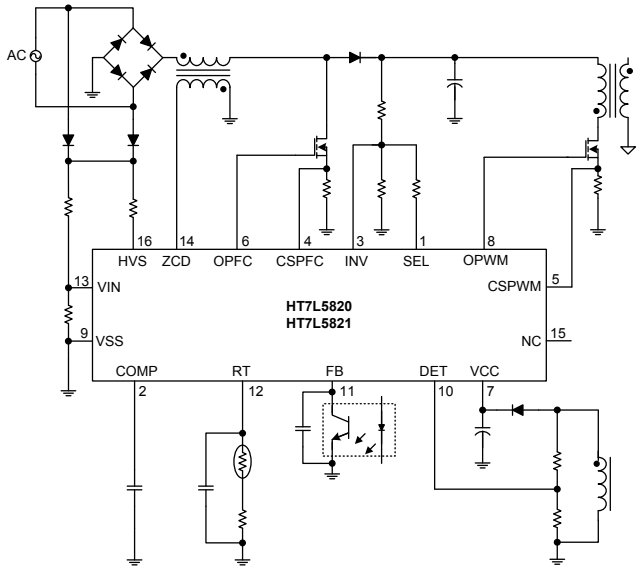
In the PFC stage the device uses a transition mode to provide a regulated output voltage with low system costs, low harmonic distortion and high power factor. For QR flyback the device provides higher efficiencies and lower EMI when compared with conventional PWM systems.

The device also includes a range of features to protect the controller from fault conditions. These include secondary side open-loop and over-current protection, VCC pin over-voltage protection, DET pin over-voltage for output over-voltage protection, brown-in/out AC input voltage, internal over-temperature shutdown and adjustable over-temperature protection using the RT pin with an external NTC resistor.

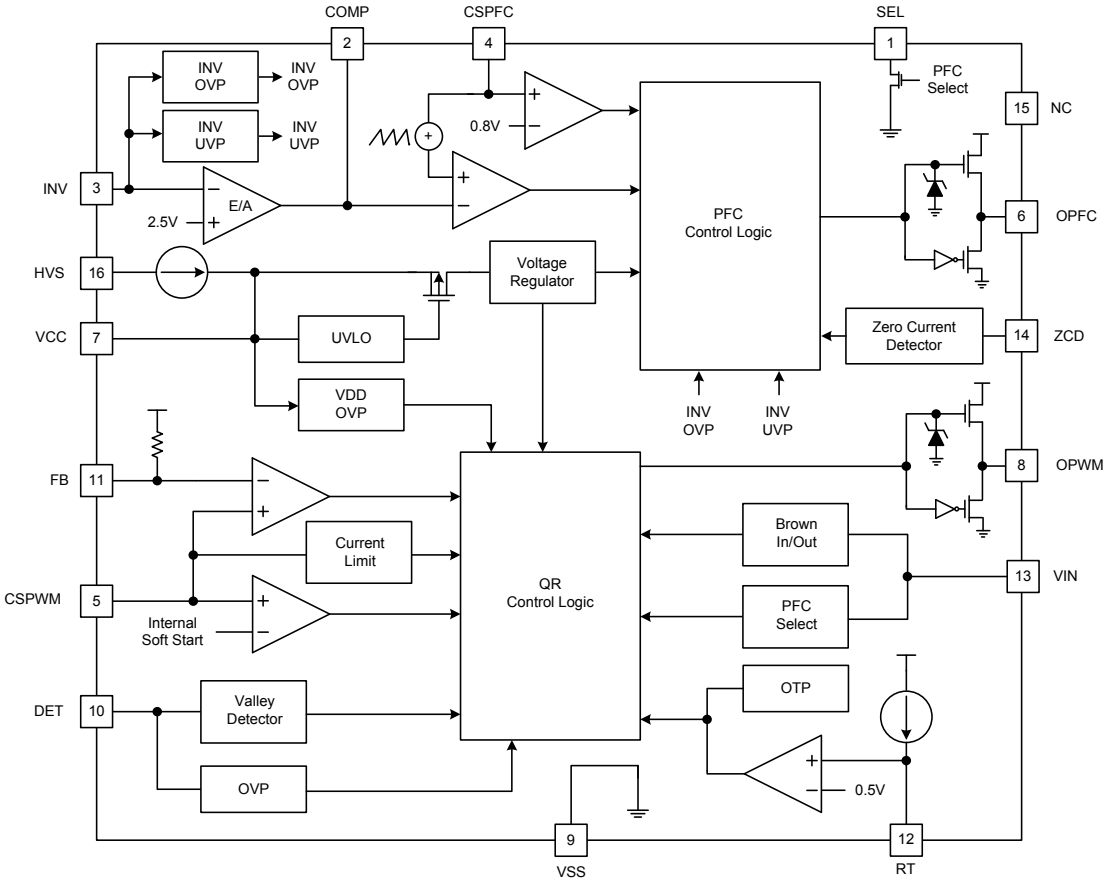
Selection Table

Part No.		HT7L5820	HT7L5821
Protection Mode	Internal OTP	Auto-Recovery	Latched
	RT Pin OTP		
	RT Pin Triggering		
	Output Voltage OVP		

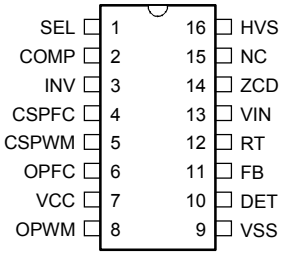
Application Circuits



Block Diagram



Pin Assignment



HT7L5820/HT7L5821
16 NSOP-A

Pin Description

Pin No.	Symbol	Description
1	SEL	PFC output selected pin
2	COMP	PFC compensation pin, a capacitor should be placed between COMP and VSS
3	INV	Voltage sense for PFC output, regulation voltage is 2.5V
4	CSPFC	Current sense pin. A resistor is connected to sense the PFC MOSFET current
5	CSPWM	Current sense pin. A resistor is connected to sense the Flyback MOSFET current
6	OPFC	Gate drive output to drive the external MOSFET for PFC
7	VCC	Power supply pin
8	OPWM	Gate drive output to drive the external MOSFET for Flyback
9	VSS	Ground pin
10	DET	Zero-current detect pin for Flyback
11	FB	Voltage feedback pin for Flyback. Connect a photo-coupler for system regulation
12	RT	External protection triggering
13	VIN	Sense input for mains voltage
14	ZCD	Zero-current detect pin for PFC
15	NC	No connection
16	HVS	HVS pin is connected to the AC line voltage through a resistor

Absolute Maximum Ratings

Parameter	Value	Unit
VCC Supply Voltage	-0.3 to 30	V
HVS Voltage	-0.3 to 650	V
SEL, COMP, INV, CSPFC, CSPWM, FB, RT, VIN	-0.3 to 6	V
Maximum Current at ZCD, DET	3 (source), 3 (sink)	mA
Operating Junction Temperature	-40 to 150	°C
Storage Temperature Range	-55 to 150	°C
Maximum Junction Temperature	150	°C

Recommended Operating

Parameter	Value	Unit
Operating Ambient temperature	-40 to 105	°C

Electrical Characteristics

V_{CC}=15V, Ta=-40~105°C (Ta=T_j), unless otherwise specified

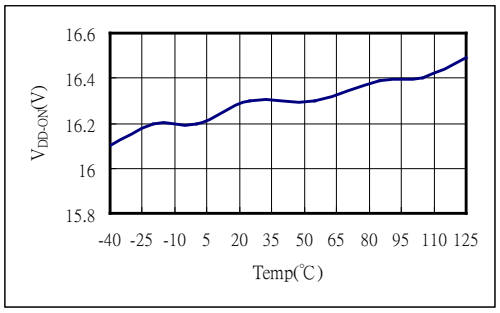
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC} Section						
V_{OP}	Continuous Operation Voltage	—	—	—	25	V
V_{CC-ON}	Turn-On Threshold Voltage	—	15	16.5	18	V
$V_{CC-PWM-OFF}$	PWM Off Threshold Voltage	—	9	10	11	V
V_{CC-OFF}	Turn-Off Threshold Voltage	—	7	8	9	V
I_{DD-ST}	Startup Current	V_{CC}=V_{CC-ON}-0.16V, gate open	—	20	—	μA
I_{DD-OP}	Operating Current	V_{CC}=15V, OPFC, OPWM=100kHz, C_{L-PFC}, C_{L-PWM}=2nF	—	—	10	mA
$I_{DD-GREEN}$	Green Mode Operating Supply Current (Average)	V_{CC}=15V, C_{L-PWM}=2nF OPWM=450Hz	—	5.5	—	mA
$I_{DD-PWM-OFF}$	Operating Current at PWM-Off Phase	V_{CC}=$V_{CC-PWM-OFF}$ - 0.5V	70	120	170	μA
V_{CC-OVP}	V_{CC} Over-Voltage Protection (Latch-Off)	—	26	28	30	V
$t_{VCC-OVP}$	V_{CC} OVP Debounce Time	—	100	150	200	μs
$I_{DD-LATCH}$	V_{CC} Over-Voltage Protection Latch-Up Holding Current	V_{CC}=7.5V	—	120	—	μA
HVS Startup Current Source Section						
$V_{HVS-MIN}$	Minimum Startup Voltage on HVS Pin	—	—	—	50	V
I_{HVS}	Supply Current Drawn from HVS Pin	V_{AC}=90V (V_{DC}=120V), V_{CC}=0V	1.3	—	—	mA
		HVS=500V, V_{CC}=V_{CC-OFF}+1V	—	8	—	μA
VIN and SEL Section						
$V_{VIN-UVP}$	Threshold Voltage for AC Input Under-Voltage Protection	—	0.85	0.9	0.95	V
$V_{VIN-RE-UVP}$	Under-Voltage Protection Reset Voltage (for Startup)	—	1.2	1.25	1.3	V
$t_{VIN-UVP}$	Under-Voltage Protection Debounce Time (No Need at Startup and Hiccup Mode)	—	70	120	170	ms
$V_{VIN-SEL-H}$	High V_{VIN} Threshold for SEL Comparator	SEL ground	2.45	2.5	2.55	V
$V_{VIN-SEL-L}$	Low V_{VIN} Threshold for SEL Comparator	SEL open	2.25	2.3	2.35	V
t_{SEL}	SEL-Enable Debounce Time	—	70	120	170	ms
V_{SEL-OL}	Output Low Voltage of SEL Pin	Io=0.1mA	—	1	—	V
$t_{on-max-PFC}$	PFC Maximum On Time	CSPFC=0v,COMP=5.5V	32	40	48	μs
PWM STAGE						
A_V	Input-Voltage to Current Sense Attenuation(note)	A_V=$\Delta V_{CS}/\Delta V_{FB}$, 0<$V_{CS}$<0.9V	1/2.75	1/3.00	1/3.25	V
Z_{FB}	Input Impedance(note)	FB>V_G	—	20	—	kΩ
I_{OZ}	Bias Current	FB=V_{OZ}	—	0.2	—	mA
V_{OZ}	Zero Duty-cycle Input Voltage	—	0.7	0.9	1.1	V
V_{FB-OLP}	Open-Loop Protection Threshold Voltage	—	3.9	4.2	4.5	V
t_{FB-OLP}	The Debounce Time for Open Loop Protection	—	20	60	100	ms
t_{ss}	Internal Soft-Start Time(note)	—	—	9.6	—	ms

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DET Pin OVP and Valley Detection Section						
$V_{DET-OVP}$	Comparator Reference Voltage	—	2.45	2.5	2.55	V
$t_{DET-OVP}$	Output OVP Debounce Time	—	100	170	240	μs
$V_{DET-HIGH}$	Upper Clamp Voltage	I_{DET}=1mA	—	5.7	—	V
$V_{DET-LOW}$	Lower Clamp Voltage	I_{DET}=-1mA	—	-0.4	—	V
$t_{VALLEY-DELAY}$	Delay Time from Valley Signal Detected to Output Turn-on(note)	—	150	200	250	ns
$t_{OFF-BNK}$	Leading-Edge Blanking Time for DET-OVP (2.5V) and Valley Signal when PWM MOS Turns Off(note)	—	3	4	5	μs
$t_{TIME-OUT}$	Time-Out After $t_{OFF-MIN}$	—	5	6	7	μs
PWM Oscillator Section						
$t_{ON-MAX-PWM}$	Maximum On Time	—	38	46	54	μs
$t_{OFF-MIN}$	Minimum Off Time	V_{FB}≥V_N	7	8.5	10	μs
		V_{FB}=V_G	31	36	41	μs
V_N	Beginning of Green-On Mode at FB Voltage Level	—	1.95	2.1	2.25	V
V_G	Beginning of Green-Off Mode at FB Voltage Level	—	1.05	1.2	1.35	V
ΔV_G	Hysteresis for Beginning of Green-Off Mode at FB Voltage Level	—	—	0.1	—	V
$V_{CTL-PFC-OFF}$	Threshold Voltage on FB Pin to Disable PFC	SEL open	1.5	1.55	1.6	V
		SEL ground	1.5	1.55	1.6	V
$V_{CTL-PFC-ON}$	Threshold Voltage on FB Pin to Enable PFC	SEL open	1.85	1.9	1.95	V
		SEL ground	1.7	1.75	1.8	V
$t_{PFC-OFF}$	PFC Disable Debounce Time to Disable PFC	PFC status from on to off	400	600	800	ms
t_{PFC-ON}	PFC Disable Debounce Time to Enable PFC	PFC status from off to on	—	150	—	μs
$t_{STARTER-PWM}$	Start Timer (Time-Out Timer)	V_{FB}<V_G	2	2.5	3	ms
PWM Output Section						
V_{CLAMP}	PWM Gate Output Clamping Voltage	V_{CC}=25V	16	17.5	19	V
V_{OL}	PWM Gate Output Voltage Low	V_{CC}=15V, I_O=100mA	—	—	1.5	V
V_{OH}	PWM Gate Output Voltage High	V_{CC}=15V, I_O=100mA	8	—	—	V
t_R	PWM Gate Output Rising Time	C_L=3nF, V_{CC}=12V, 20~80%	—	80	110	ns
t_F	PWM Gate Output Falling Time	C_L=3nF, V_{CC}=12V, 20~80%	—	40	70	ns
Current Sense Section						
t_{PD}	Delay to Output	—	—	70	200	ns
V_{LIMIT}	The Limit Voltage on CSPWM Pin for Over Power Compensation	I_{DET}<75μA, Ta=25°C	0.82	0.85	0.88	V
		I_{DET}=550μA, Ta=25°C	0.37	0.4	0.43	V
V_{SLOPE}	Slope Compensation(note)	t_{ON}=45μs	—	0.3	—	V
		t_{ON}=0μs	—	0	—	V
t_{ON-BNK}	Leading-Edge Blanking Time	—	—	300	—	ns
$V_{CS-FLOATING}$	CSPWM Pin Floating V_{CSPWM} Clamped High Voltage	CSPWM pin floating	—	3.75	—	V
t_{CS-H}	The Delay Time Once CS Pin Floating	CSPWM pin floating	—	150	—	μs

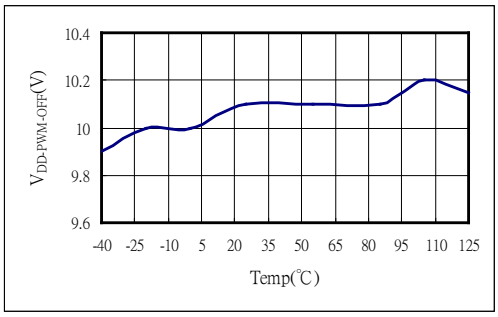
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
RT Pin Over-Temperature Protection Section						
T_{OTP}	Internal Threshold Temperature for OTP (note)	—	125	140	155	°C
I_{RT}	Internal Source Current of RT Pin	—	96	107	118	μA
$V_{RT-TRIGGER}$	Protection triggering Voltage	—	0.95	1	1.05	V
$V_{RT-OTP-LEVEL}$	Threshold Voltage for Two-level Debounce Time	—	0.45	0.5	0.55	V
$t_{RT-OTP-H}$	Debounce Time for OTP	—	—	10	—	ms
$t_{RT-OTP-L}$	Debounce Time for Externally Triggering	V_{RT} <$V_{RT-OTP-LEVEL}$	70	100	130	μs
PFC Stage						
Voltage Error Amplifier Section						
Gm	Transconductance(note)	—	—	150	—	μS
V_{REF}	Feedback Comparator Reference Voltage	—	2.465	2.5	2.535	V
$V_{INV-OVP}$	Over Voltage Protection for INV Input	SEL open	2.65	2.70	2.75	V
		SEL ground	2.575	2.625	2.675	V
$V_{INV-UVP}$	Under-Voltage Protection for INV Input	—	0.25	0.35	0.45	V
$t_{INV-UVP}$	Under-Voltage Protection Debounce Time	—	30	60	90	μs
V_{INV-BO}	PWM and PFC Off Threshold for Brownout Protection	—	1.15	1.2	1.25	V
$V_{COMP-BO}$	Limited Voltage on COMP Pin for Brownout Protection	—	—	1.6	—	V
V_{COMP}	Comparator Output High Voltage	—	5.5	—	6.5	V
V_{OZ}	Zero Duty Cycle Voltage on COMP Pin	—	0.65	0.7	0.75	V
I_{COMP}	Comparator Output Source Current	V_{INV}=2.3V, V_{COMP}=1.5V	—	30	—	μA
	Comparator Output Sink Current	V_{INV}=2.7V, V_{COMP}=5V	—	30	—	μA
PFC Current Sense Section						
V_{CSPFC}	Threshold Voltage for Peak Current Cycle-by-Cycle Limit	V_{COMP}=5V	—	0.8	—	V
t_{PD}	Propagation Delay	—	—	180	300	ns
t_{LEB}	Leading Edge Blanking Time	—	—	200	—	ns
PFC Zero Current Detection Section						
V_{ZCD}	Input Threshold Voltage Rise Edge	V_{ZCD} increasing	—	1.4	—	V
$V_{ZCD-HYST}$	Threshold Voltage Hysteresis	V_{ZCD} decreasing	—	0.7	—	V
$V_{ZCD-HIGH}$	Upper Clamp Voltage	I_{ZCD}=1mA	—	5.7	—	V
$V_{ZCD-LOW}$	Lower Clamp Voltage	I_{ZCD}=-1mA	—	-0.4	—	V
t_{DELAY}	Maximum Delay from ZCD to Output Turn-On	V_{COMP}=5V, f_S=60kHz	100	—	200	ns
$t_{RESTART-PFC}$	Restart Time	—	—	190	—	μs
t_{INHIB}	Inhibit Time (Maximum Switching Frequency Limit)	V_{COMP}=5V	—	1	—	μs
PFC Output Section						
V_Z	PFC Gate Output Clamping Voltage	V_{CC}=25V	16	17.5	19	V
V_{OL}	PFC Gate Output Voltage Low	V_{CC}=15V, I_O=100mA	—	—	1.5	V
V_{OH}	PFC Gate Output Voltage High	V_{CC}=15V, I_O=100mA	8	—	—	V
t_R	PFC Gate Output Rising Time	C_L=3nF, V_{CC}=12V, 20~80%	—	80	110	ns
t_F	PFC Gate Output Falling Time	C_L=3nF, V_{CC}=12V, 20~80%	—	40	70	ns

Note: Guaranteed by design.

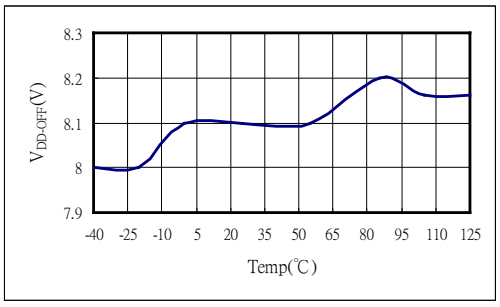
Typical Performance Characteristics



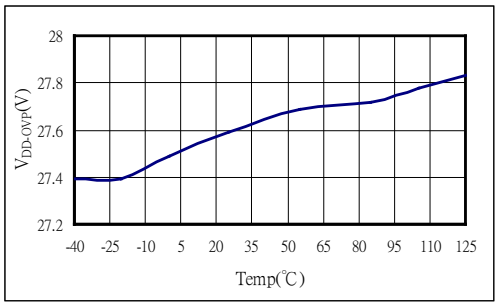
Turn-On Threshold Voltage



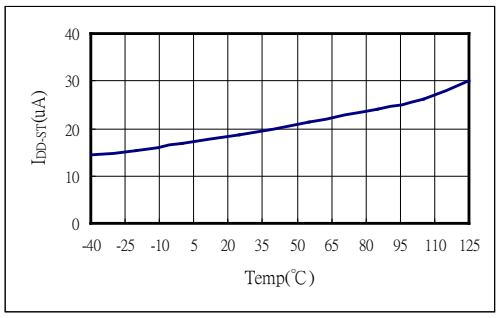
PWM Off Threshold Voltage



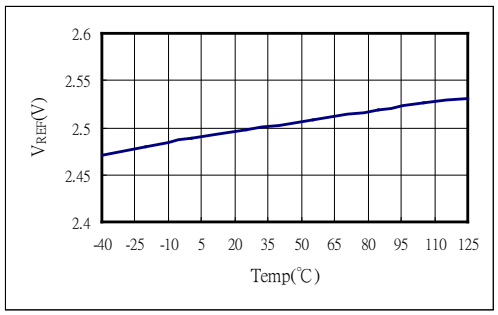
Turn-Off Threshold Voltage



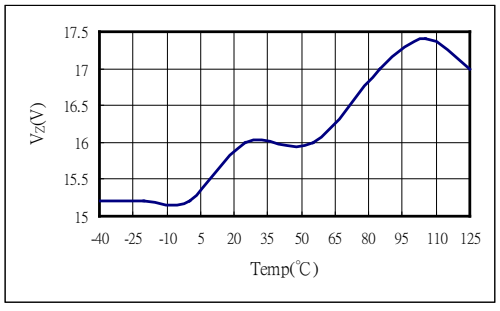
VCC Over-Voltage Protection Threshold



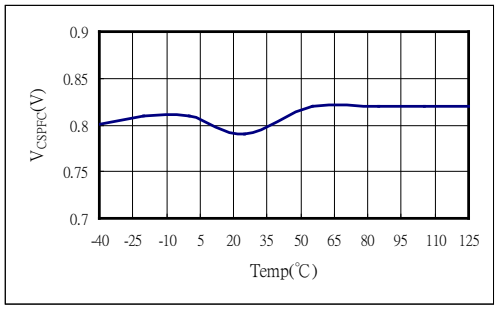
Startup Current



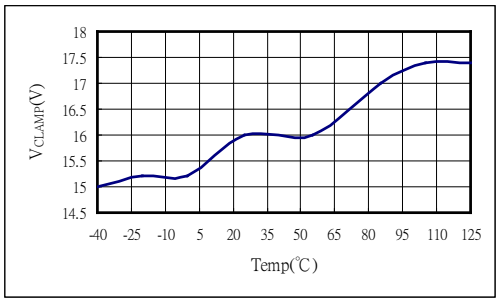
PFC Output Feedback Reference Voltage



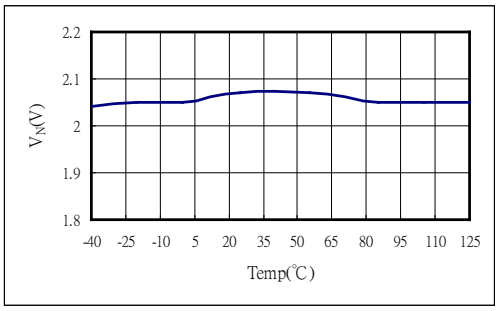
PFC Gate Output Clamping Voltage



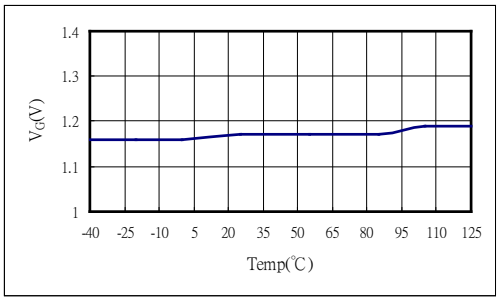
PFC Peak Current Limit Voltage



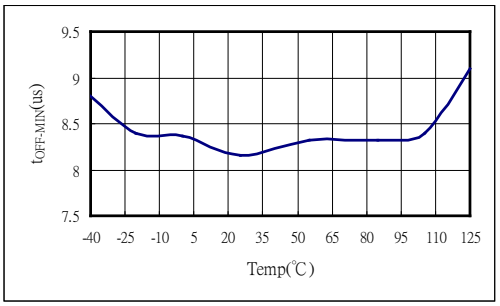
PWM Gate Output Clamping Voltage



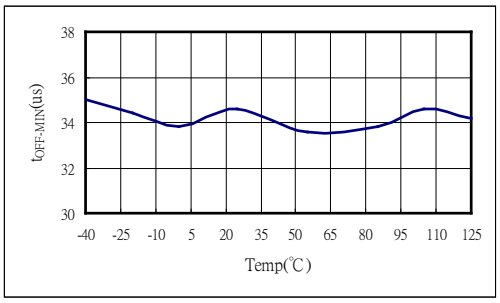
Beginning of Green-On Mode at VFB



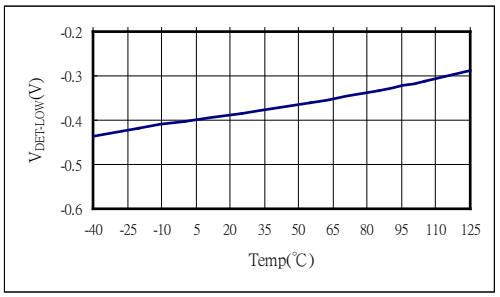
Beginning of Green-Off Mode at VFB



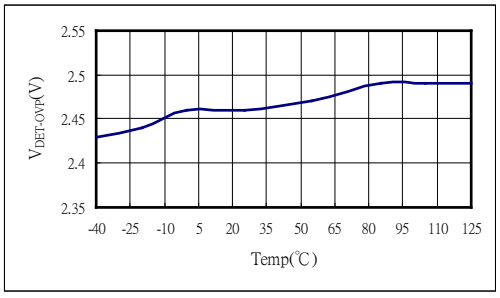
PWM Minimum Off-Time for VFB > VN



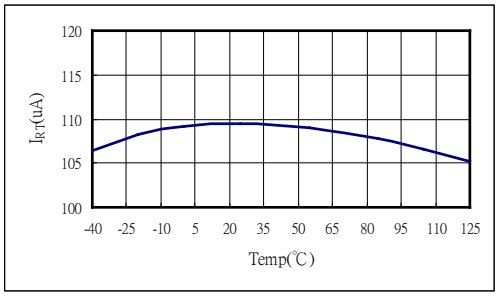
PWM Minimum Off-Time for VFB=VG



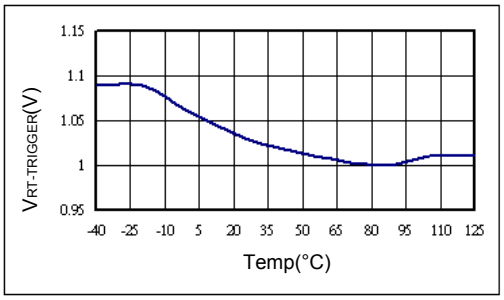
Lower Clamp Voltage of DET Pin



Reference Voltage for Output Over-Voltage Protection of DET Pin



Internal Source Current of RT Pin



Over Temperature Protection Threshold Voltage of RT Pin

Functional Description

PFC Stage

Error Amplifier

The PFC error amplifier is used for regulating the PFC output voltage. The error amplifier input is the INV pin and it is connected to a resistor divider from the PFC output. The error amplifier input voltage is compared with an internal reference voltage of 2.5V to make the error amplifier source or sink current to charge and discharge its output capacitor. The capacitor voltage will determine the on-time of the PFC controller to regulate the output voltage. The sink and source capability of the error amplifier is approximately 30uA during normal the operation and the typical transconductance value is 150μS.

Dynamic Response

The PFC dynamic response is very slow because of the PFC voltage loop low frequency bandwidth. The device provides an enhanced dynamic response for the PFC loop by detecting the feedback voltage on the INV pin. Whenever the INV voltage is lower than the reference value 2.3V, it will increase the error amplifier transconductance and in turn increase the PFC duty cycle directly. This change in duty cycle bypasses the slow change of the COMP voltage and thus results in a fast dynamic response for the PFC stage.

ZCD Pin

The device performs zero current detection by using an auxiliary winding on the PFC boost inductor. During normal operation, when the PFC MOS is switched off, the stored energy in the PFC boost inductor will release its energy to the output. The voltage on the ZCD pin decreases as the stored energy in the PFC boost inductor is released to the output. When the ZCD pin voltage is lower than 0.7V, the internal ZCD comparator is triggered and a PFC gate signal is generated. If no triggering signal is detected on the ZCD pin, the device will generate a restart signal 190μs after the last PFC gate signal. The maximum and minimum voltage of the ZCD pin is internally clamped to 5.7V and 0V respectively

SEL Pin

A built-in low voltage switch can be turned on or off according to VIN voltage level. The drain pin of this internal switch is connected to the SEL pin.

Brown-in/out Protection – VIN Pin

The device features brown-in/out protection using AC voltage detection. The VIN pin is used to detect the AC input voltage using a resistor divider. As the AC voltage drops and the V_{VIN} voltage drops below 0.9V for 100ms, the UVP protection function is activated and the COMP pin voltage is clamped to around 1.6V. Since a lower COMP voltage results in a reduced PFC on-time, the energy concentration is limited and therefore the PFC output voltage decreases. When the INV pin is lower than 1.2V, the device turns off all PFC and PWM switching operations and the V_{CC} voltage enters the hiccup mode. Not until the V_{VIN} voltage increases beyond 1.25V (typical) and V_{CC} reaches its turn-on voltage again will the PWM and PFC gate signals be generated.

Peak Current Limiting – CSPFC Pin

The CSPFC pin is used to sense the PFC switch current. During normal PFC operation, the voltage on the CSPFC pin is compared with a threshold voltage of 0.8V using the internal comparator. When the CSPFC pin voltage is greater than the threshold voltage, the PFC switch will be turned off immediately. The current-sense resistor is adjustable to determine the PFC switch peak current.

Output Voltage OVP and UVP – INV Pin

Over-voltage and under-voltage protection functions are integrated into the device for the PFC stage. Both are detected and determined using the INV pin voltage. The OVP or UVP circuit is activated to stop PFC switching operations immediately when the INV pin voltage is greater than 2.65V or less than 0.35V. In addition, the de-bounce time of the OVP and UVP is set to about 70μs to avoid overshoot or abnormal conditions.

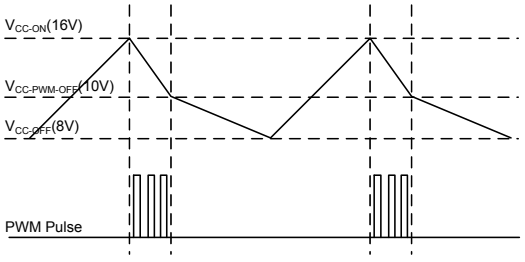
QR Flyback Stage

Startup Current – HVS Pin

For startup purposes the HVS pin is connected to the AC line input through a resistor. Using an integrated high-voltage startup circuit, the device provides a high current to charge the external VCC capacitor to reduce the controller's startup time. To reduce power consumption, when the VCC voltage exceeds the turn-on voltage and enters normal operation, this high voltage startup circuit will be switched off to avoid power losses due to power consumption in the startup resistor.

Under-Voltage Lockout (UVLO) – VCC Pin

The turn-on, PWM-off and turn-off thresholds are fixed internally at 16V/10V/8V, respectively. During startup, the hold-up capacitor (V_{CC} cap.) is charged by the HV startup current until the V_{CC} voltage reaches the turn-on voltage. The hold-up capacitor continues to supply V_{CC} until energy can be delivered from the auxiliary winding. During this startup process, V_{CC} must not drop below $V_{CC\ PWM\text{-}OFF}$. This UVLO hysteresis window ensures that hold-up capacitor is suitable for supplying V_{CC} during startup. The following figure shows the V_{CC} waveform in the hiccup mode.



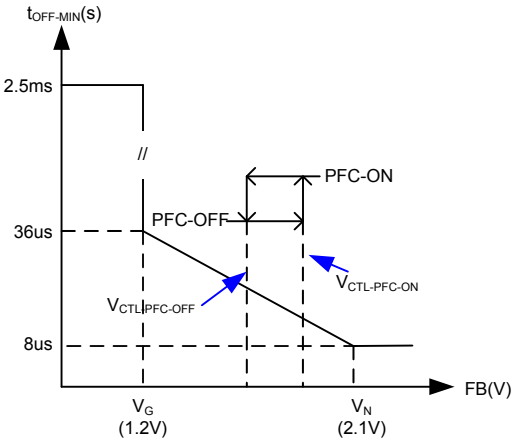
V_{CC} during Hiccup Mode Operation

Valley Detection – DET Pin

The DET pin is connected to an auxiliary winding of the transformer using divider resistors. During the PWM off time, when the transformer inductor current discharges to zero, the transformer inductor and parasitic capacitors of the PWM switch start to resonate concurrently. As the drain voltage on the PWM switch falls, the voltage on the auxiliary winding V_{AUX} decreases as well. Then, the internal DET comparator detects the valley voltage of the switching waveform to achieve valley voltage switching. This ensures QR operation, minimises switching losses and reduces EMI. The maximum and minimum voltage of the DET pin is internally clamped to 5.7V and -0.4V respectively.

Green-Mode and PFC On/Off Control – FB Pin

A Green Mode mechanism is adopted to reduce switching losses in the power system under conditions of light load. The device uses a linear off-time modulation to decrease switching frequency according to the FB pin voltage. The following figure shows the FB versus $t_{OFF\text{-}MIN}$ characteristic curve. As FB pin Voltage is lower than V_N (2.1V), the $t_{OFF\text{-}MIN}$ time increases with lower FB pin voltage. The valley voltage detection signal does not activate until the $t_{OFF\text{-}MIN}$ time finishes which extends valley voltage switching during DCM operation and reduces switching losses to obtain higher conversion efficiencies. In addition, in order to reduce the standby power under conditions of no load or very light-load, the FB pin voltage is also used to control the PFC on/off operation. As the FB voltage falls below the $V_{CTL\text{-}PFC\text{-}OFF}$ threshold voltage the controller will stop PFC switching until the FB pin voltage returns to $V_{CTL\text{-}PFC\text{-}ON}$.

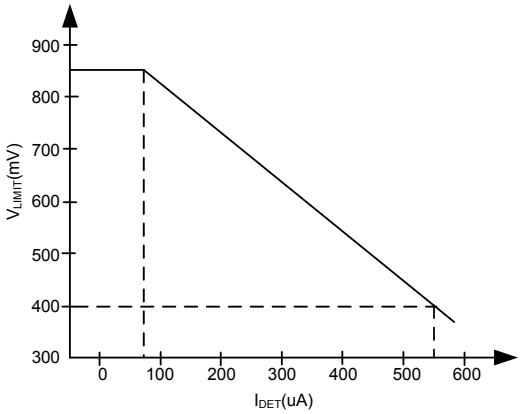


FB vs $T_{off\text{-}min}$ Characteristic Curve

High/Low Line Over-Power Compensation – DET Pin

The power delivered by a flyback power supply is proportional to the square of the peak current during QR control. However, due to the inherent propagation delay of the logic, the actual peak current is higher for a high input voltage than for a low input voltage. This results in a significant difference between the maximum output power delivered by the power supply. To compensate for this variation for a universal input range, the DET pin produces an offset voltage to compensate the threshold voltage of the peak current limit.

This offset voltage is generated by sensing the current drawn from the DET pin when the power switch turns on. The following figure shows the I_{DET} versus V_{LIMIT} characteristic curve.



I_{DET} vs V_{LIMIT} Characteristic Curve

Leading Edge Blanking – LEB

Each time the PFC or PWM switches are turned on, a voltage spike occurs on the current sense resistor. To avoid faulty triggering, a leading-edge blanking time is built into the device. During the blanking period the current limit comparator is disabled and cannot switch off the gate driver.

VCC Pin Over-Voltage Protection – VCC OVP

The VCC OVP function is used to prevent device damage. If the V_{CC} voltage is higher than $V_{CC\text{-}OVP}$ and lasts for a time $t_{VCC\text{-}OVP}$, the controller stops all switching operations and enters the latch mode until the AC plug is removed.

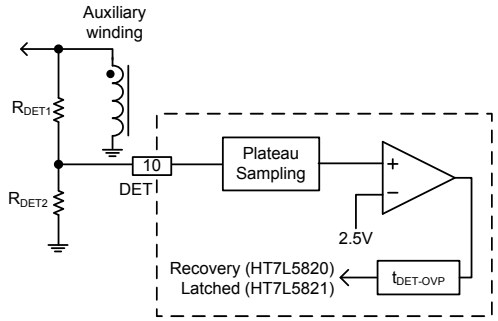
Adjustable Over-Temperature Protection and External Protection Triggering – RT Pin

The RT pin is used to achieve over-temperature protection using an NTC resistor and provides external protection triggering for additional protection. Typically, since the external protection triggerig is usually used to protect the power system from abnormal conditions it needs a fast reaction speed or a short reaction time. Therefore, the protection debounce time of the external protection triggering is set to around 100μs once the RT pin voltage is lower than 0.5V. For over temperature protection, since the temperature cannot change rapidly, the protection debounce time should not be activated quickly. The protection debounce time for the OTP is set to around 10ms. In addition, to avoid improper triggering due to a lightning test, the RT pin triggering voltage of the OTP is set to 1.0V, which is higher than the external triggering voltage of 0.5V.

DET Pin Over-Voltage Protection – DET OVP

An output over-voltage protection is implemented by sensing the auxiliary winding voltage on the DET pin. The QR OVP works by sampling the plateau voltage on the DET pin after the PWM switch-off sequence. A 4μs internal blanking time guarantees a clean plateau provided that the leakage inductance ringing has been fully damped. If the sampled plateau voltage exceeds the OVP trip level of 2.5V and lasts for $t_{DET\text{-}OVP}$, the device will enter auto-recovery protection (HT7L5820) or the latch mode (HT7L5821) until the AC power is removed. The protection voltage level can be determined by the ratio of the external resistor divider R_{DET1} and R_{DET2}, as shown in the following figure. The flat voltage on the DET pin can be expressed by the following equation:

$$V_{DET} = (N_A/N_S)\times V_O\times \frac{R_{DET2}}{R_{DET1}+R_{DET2}}$$



DET Over-Voltage Protection

Output Open-Loop and Over-Load Protection

To protect the circuit from being damaged during conditions of output open-loop or overload, the device includes an OLP function. Under such fault conditions, the output voltage is decreased and the sink current of the photo-coupler is reduced. This will force the FB pin voltage to increase using an internal bias. When the FB pin voltage ramps up to 4.2V for 50ms the OLP protection is activated to turn off the power switch and stop all switching operations.

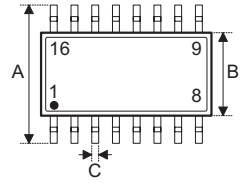
Package Information

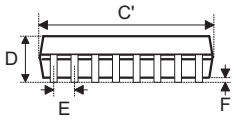
Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the package information.

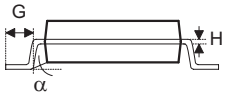
Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

16-pin NSOP (150mil) Outline Dimensions







Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.012	—	0.020
C'	—	0.390 BSC	—
D	—	—	0.069
E	—	0.050 BSC	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.000 BSC	—
B	—	3.900 BSC	—
C	0.31	—	0.51
C'	—	9.900 BSC	—
D	—	—	1.75
E	—	1.270 BSC	—
F	0.10	—	0.25
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°

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