Absolute Maximum Ratings

Operating Temperature (Commercial) ..... 0°C to 70°C

Storage Temperature ..... –50°C to 125°C

Applied VCC Voltage with Respect to VSS ..... V_{SS} –0.3V to V_{SS}+6.0V

Applied Voltage on any Pin with Respect to VSS ..... V_{SS} –0.3V to V_{CC}+0.3V

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=0°C to 70°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
V_{CC}	Operating Voltage	—	—	2.4	—	5.5	V
I_{CC1}	Operating Current	5V	Read at 100kHz	—	—	2	mA
I_{CC2}	Operating Current	5V	Write at 100kHz	—	—	5	mA
V_{IL}	Input Low Voltage	—	—	–1	—	$0.3V_{CC}$	V
V_{IH}	Input High Voltage	—	—	$0.7V_{CC}$	—	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	2.4V	I_{OL}=2.1mA	—	—	0.4	V
I_{LI}	Input Leakage Current	5V	V_{IN}=0 or V_{CC}	—	—	1	μA
I_{LO}	Output Leakage Current	5V	V_{OUT}=0 or V_{CC}	—	—	1	μA
I_{STB1}	Standby Current	5V	V_{IN}=0 or V_{CC}	—	—	5	μA
I_{STB2}	Standby Current	2.4V	V_{IN}=0 or V_{CC}	—	—	4	μA
C_{IN}	Input Capacitance (See Note)	—	f=1MHz 25°C	—	—	6	pF
C_{OUT}	Output Capacitance (See Note)	—	f=1MHz 25°C	—	—	8	pF

Note: These parameters are periodically sampled but not 100% tested.

A.C. Characteristics

Ta=0°C to 70°C

Symbol	Parameter	Remark	Standard Mode*		V_{CC}=5V±10%		Unit
			Min.	Max.	Min.	Max.	
f_{SK}	Clock Frequency	—	—	100	—	400	kHz
t_{HIGH}	Clock High Time	—	4000	—	600	—	ns
t_{LOW}	Clock Low Time	—	4700	—	1200	—	ns
t_R	SDA and SCL Rise Time	Note	—	1000	—	300	ns
t_F	SDA and SCL Fall Time	Note	—	300	—	300	ns
$t_{HD:STA}$	START Condition Hold Time	After this period, the first clock pulse is generated.	4000	—	600	—	ns
$t_{SU:STA}$	START Condition Setup Time	Only relevant for repeated START condition.	4000	—	600	—	ns
$t_{HD:DAT}$	Data Input Hold Time	—	0	—	0	—	ns
$t_{SU:DAT}$	Data Input Setup Time	—	200	—	100	—	ns
$t_{SU:STO}$	STOP Condition Setup Time	—	4000	—	600	—	ns
t_{AA}	Output Valid from Clock	—	—	3500	—	900	ns

Symbol	Parameter	Remark	Standard Mode*		V_{CC}=5V±10%		Unit
			Min.	Max.	Min.	Max.	
t_{BUF}	Bus Free Time	Time in which the bus must be free before a new transmission can start	4700	—	1200	—	ns
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	100	—	50	ns
t_{WR}	Write Cycle Time	—	—	5	—	5	ms

Note: These parameters are periodically sampled but not 100% tested

* The standard mode means V_{CC}=2.4V to 5.5V

For relative timing, refer to timing diagrams

Functional Description

- Serial clock (SCL)
  The SCL input is used for positive edge clock data into each EEPROM device and negative edge clock data out of each device.
- Serial data (SDA)
  The SDA pin is bidirectional for serial data transfer. The pin is open drain driven and may be wired-OR with any number of other open drain or open collector devices.
- A0, A1, A2
  The A2, A1 and A0 pins are device address inputs that are hard wired or left not connected for hardware compatibility with HT24LC64. When the pins are hardwired, as many as eight 64K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). These inputs must be tied to V_{CC} or V_{SS}, to establish the device select code.
- Write protect (WP)
  The HT24LC64 has a write protect pin that provides hardware data protection. The write protect pin allows normal read/write operations when the connection is grounded. When the write protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following table.

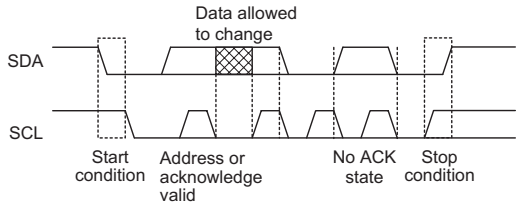
WP Pin Status	Protect Array
At V_{CC}	Full Array (64K)
At V_{SS} (floating)	Normal Read/Write Operations

Memory Organization

Internally organized with 8192 8-bit words, the 64K requires a 13-bit data word address for random word addressing.

Device Operations

- Clock and data transition
  Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever the clock line is high. Changes in data line while the clock line is high will be interpreted as a START or STOP condition.
- Start condition
  A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition Timing diagram).
- Stop condition
  A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition Timing Diagram).
- Acknowledge
  All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.



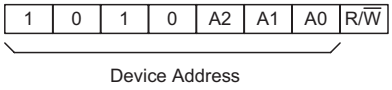
Device Addressing

The 64K EEPROM devices require an 8-bit device address word following a start condition to enable the chip for a read or write operation. The device address word consist of a mandatory one, zero sequence for the first four most significant bits (refer to the diagram showing the Device Address). This is common to all the EEPROM device.

The 64K EEPROM uses the three device address bits A2, A1, A0 to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins.

The 8th bit device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

If the comparison of the device address succeed the EEPROM will output a zero at ACK bit. If not, the chip will return to a standby state.



Device Address

Write Operations

- Byte write

  A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. After receiving the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle to the nonvolatile memory. All inputs are disabled during this write cycle and EEPROM will not respond until the write operation is completed (refer to Byte write timing).

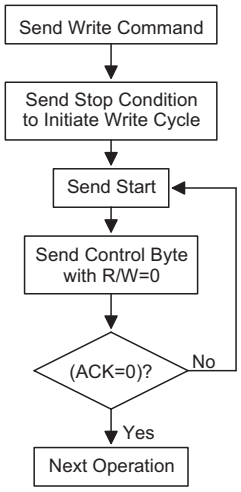
- Page write

  The 64K EEPROM is capable of a 32-byte page write. A page write is initiated in the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges the receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Page write timing).

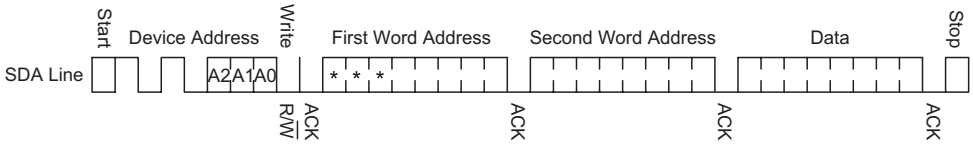
  The data word address lower 5 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data word address will ″roll over″ and previous data will be overwritten.

- Acknowledge polling

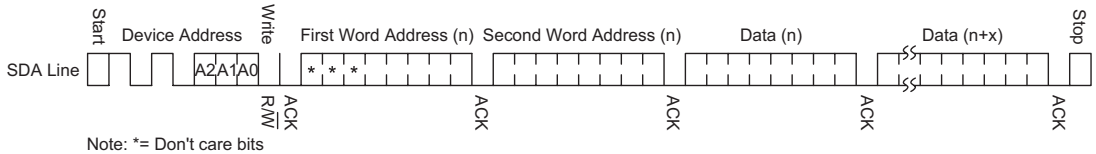
  To maximize bus throughput, one technique is to allow the master to poll for an acknowledge signal after the start condition and the control byte for a write command have been sent. If the device is still busy implementing its write cycle, then no ACK will be returned. The master can send the next read/write command when the ACK signal has finally been received.



Acknowledge Polling Flow



Byte Write Timing



Page Write Timing

- Write protect

  The HT24LC64 has a write-protect function and programming will then be inhibited when the WP pin is connected to VCC. Under this mode, the HT24LC64 is used as a serial ROM.

- Read operations

  The HT24LC64 supports three read operations, namely, current address read, random address read and sequential read. During read operation execution, the read/write select bit should be set to ″1″.

- Current address read

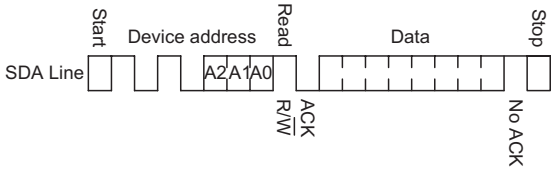
  The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address remains valid between operations as long as the chip power is maintained. The address will roll over during read from the last byte of the last memory page to the first byte of the first page. The address will roll over during write from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but generates a following stop condition (refer to Current read timing).

- Random read

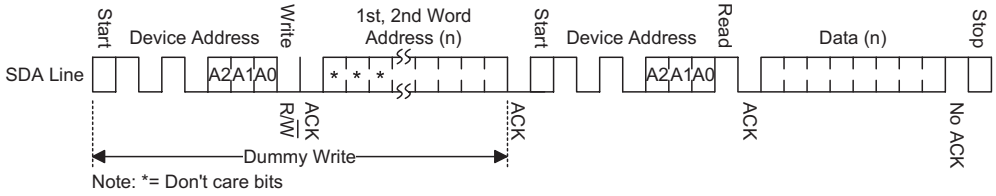
  A random read requires a dummy byte write sequence to load in the data word address which is then clocked in and acknowledged by the EEPROM. The microcontroller must then generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller should respond with a ″no ACK″ signal (high) followed by a stop condition (refer to Random read timing).

- Sequential read

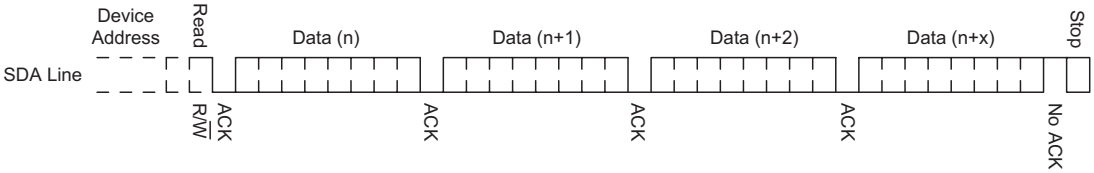
  Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledgment. As long as the EEPROM receives an acknowledgment, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll over and the sequential read continues. The sequential read operation is terminated when the microcontroller does not respond with a zero but generates a following stop condition.



Current Address Read Timing

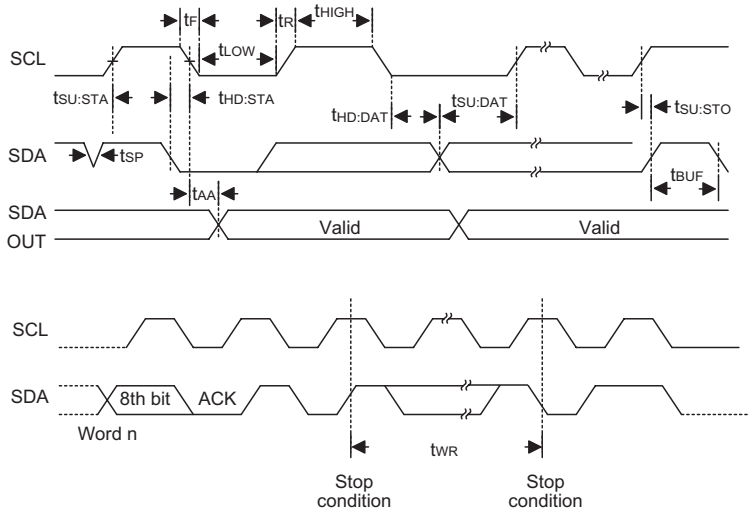


Random Read Timing



Sequential Read Timing

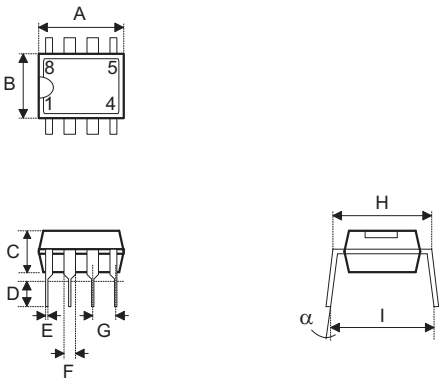
Timing Diagrams



Note: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the valid start condition of sequential command.

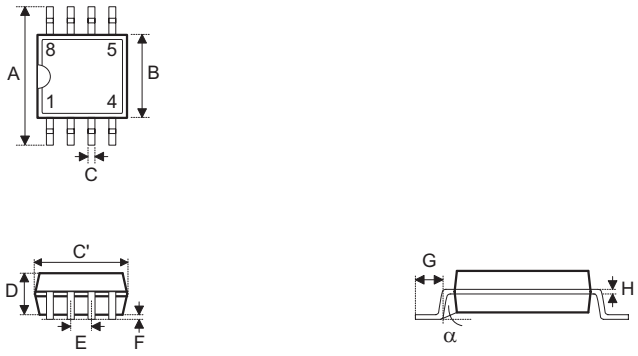
Package Information

8-pin DIP (300mil) Outline Dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	355	—	375
B	240	—	260
C	125	—	135
D	125	—	145
E	16	—	20
F	50	—	70
G	—	100	—
H	295	—	315
I	335	—	375
α	0°	—	15°

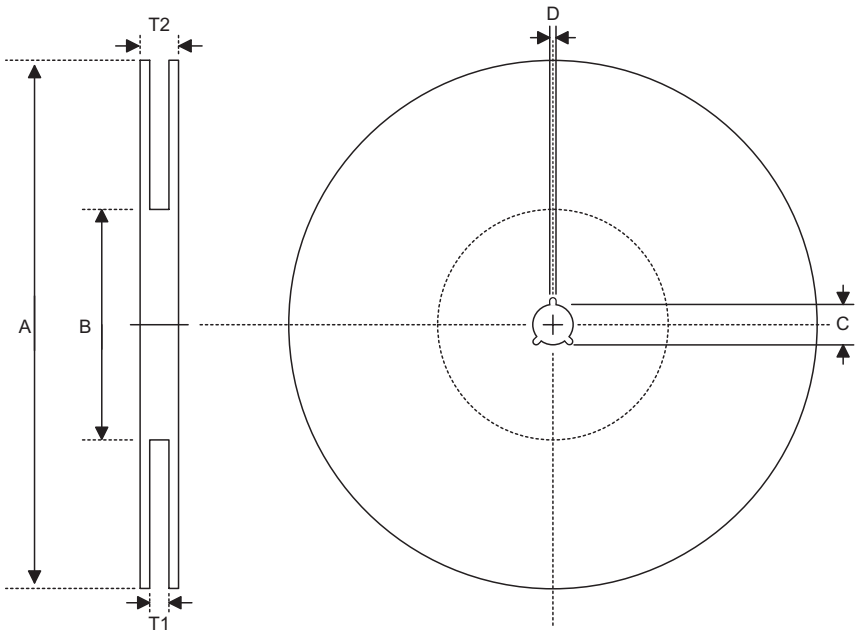
8-pin SOP (150mil) Outline Dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	228	—	244
B	149	—	157
C	14	—	20
C′	189	—	197
D	53	—	69
E	—	50	—
F	4	—	10
G	22	—	28
H	4	—	12
α	0°	—	10°

Product Tape and Reel Specifications

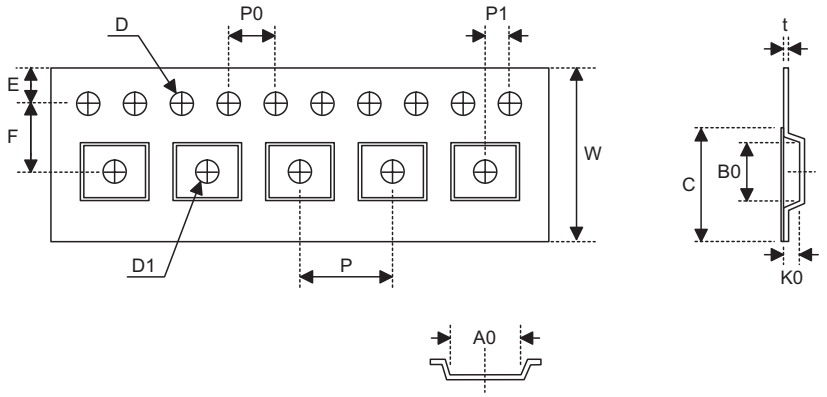
Reel Dimensions



SOP 8N

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330±1.0
B	Reel Inner Diameter	62±1.5
C	Spindle Hole Diameter	13.0+0.5 −0.2
D	Key Slit Width	2.0±0.15
T1	Space Between Flange	12.8+0.3 −0.2
T2	Reel Thickness	18.2±0.2

Carrier Tape Dimensions



SOP 8N

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	12.0+0.3 −0.1
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	5.5±0.1
D	Perforation Diameter	1.55±0.1
D1	Cavity Hole Diameter	1.5+0.25
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.4±0.1
B0	Cavity Width	5.20±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.3±0.05
C	Cover Tape Width	9.3

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