HT24LC02
CMOS 2K 2-Wire Serial EEPROM

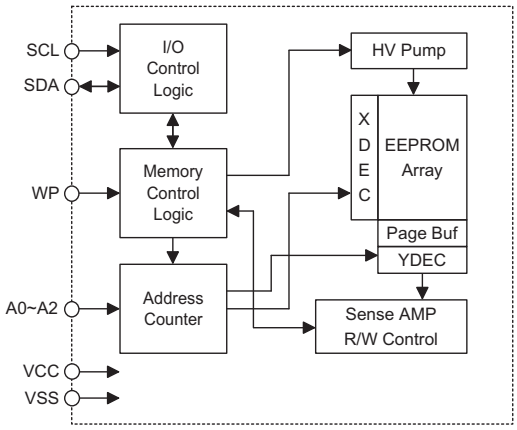
Features

- Operating voltage:
  2.2V~5.5V for temperature –40°C to +85°C
- Low power consumption
  - Operation: 5mA max.
  - Standby: 2μA max.
- Internal organization: 256×8
- 2-wire serial interface
- Write cycle time: 5ms max.
- Automatic erase-before-write operation
- Partial page write allowed
- 8-byte Page write modes
- Write operation with built-in timer
- Hardware controlled write protection
- 40-year data retention
- 10^6 erase/write cycles per word
- Industrial temperature range (–40°C to +85°C)
- 8-pin DIP/SOP/TSSOP , SOT23-5 package.

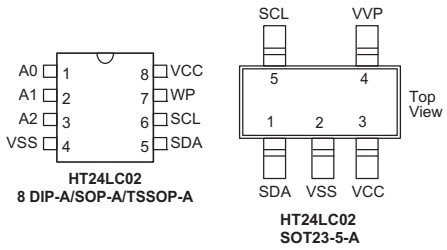
General Description

The HT24LC02 is a 2K-bit serial read/write non-volatile memory device using the CMOS floating gate process. Its 2048 bits of memory are organized into 256 words and each word is 8 bits. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. Up to eight HT24LC02 devices may be connected to the same 2-wire bus. The HT24LC02 is guaranteed for 1M erase/write cycles and 40-year data retention.

Block Diagram



Pin Assignment



Note: For use of SOT23-5 package, the software A2, A1, and A0 bits in the device address word must be set to zero to properly communicate.

Pin Description

Pin Name	I/O	Description
A0~A2	I	Address inputs
SDA	I/O	Serial data inputs/output
SCL	I	Serial clock data input
WP	I	Write protect
VSS	—	Negative power supply, ground
VCC	—	Positive power supply

Absolute Maximum Ratings

Supply Voltage .....V_{SS}–0.3V to V_{SS}+6.0V

Input Voltage .....V_{SS}–0.3V to V_{CC}+0.3V

Storage Temperature .....–50°C to 125°C

Operating Temperature.....–40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{CC}	Conditions				
V_{CC}	Operating Voltage	—	–40°C to +85°C	2.2	—	5.5	V
I_{CC1}	Operating Current	5V	Read at 100kHz	—	—	2	mA
I_{CC2}	Operating Current	5V	Write at 100kHz	—	—	5	mA
V_{IL}	Input Low Voltage	—	—	–1	—	$0.3V_{CC}$	V
V_{IH}	Input High Voltage	—	—	$0.7V_{CC}$	—	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	2.4V	I_{OL}=2.1mA	—	—	0.4	V
I_{LI}	Input Leakage Current	5V	V_{IN}=0 or V_{CC}	—	—	1	μA
I_{LO}	Output Leakage Current	5V	V_{OUT}=0 or V_{CC}	—	—	1	μA
I_{STB}	Standby Current	2.2V~5.5V	V_{IN}=0 or V_{CC}	—	—	2	μA
C_{IN}	Input Capacitance (See Note)	—	f=1MHz 25°C	—	—	6	pF
C_{OUT}	Output Capacitance (See Note)	—	f=1MHz 25°C	—	—	8	pF

Note: These parameters are periodically sampled but not 100% tested

A.C. Characteristics

Symbol	Parameter	Remark	Standard Mode*		V_{CC}=3V±10%		V_{CC}=5V±10%		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{SK}	Clock Frequency	—	—	100	—	400	—	1000	kHz
t_{HIGH}	Clock High Time	—	4000	—	600	—	400	—	ns
t_{LOW}	Clock Low Time	—	4700	—	1200	—	600	—	ns
t_r	SDA and SCL Rise Time	Note	—	1000	—	300	—	300	ns
t_f	SDA and SCL Fall Time	Note	—	300	—	300	—	100	ns
$t_{HD:STA}$	START Condition Hold Time	After this period the first clock pulse is generated	4000	—	600	—	250	—	ns
$t_{SU:STA}$	START Condition Setup Time	Only relevant for repeated START condition	4000	—	600	—	250	—	ns
$t_{HD:DAT}$	Data Input Hold Time	—	0	—	0	—	—	—	ns
$t_{SU:DAT}$	Data Input Setup Time	—	200	—	100	—	100	—	ns
$t_{SU:STO}$	STOP Condition Setup Time	—	4000	—	600	—	250	—	ns
t_{AA}	Output Valid from Clock	—	—	3500	—	900	50	550	ns
t_{BUF}	Bus Free Time	Time in which the bus must be free before a new transmission can start	4700	—	1200	—	500	—	ns
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	100	—	50	—	50	ns
t_{WR}	Write Cycle Time	—	—	5	—	5	—	5	ms

Note: These parameters are periodically sampled but not 100% tested

* The standard mode means V_{CC}= 2.2V to 5.5V at Ta= –40°C to +85°C

For relative timing, refer to timing diagrams

Functional Description

- Serial clock (SCL)
  The SCL input is used for positive edge clock data into each EEPROM device and negative edge clock data out of each device.
- Serial data (SDA)
  The SDA pin is bidirectional for serial data transfer. The pin is open-drain driven and may be wired-OR with any number of other open-drain or open collector devices.
- A0, A1, A2
  The A2, A1 and A0 pins are device address inputs that are hard wired for the HT24LC02. As many as eight 2K devices may be addressed on a single bus system (the device addressing is discussed in detail under the Device Addressing section).
- Write protect (WP)
  The HT24LC02 has a write protect pin that provides hardware data protection. The write protect pin allows normal read/write operations when connected to the V_{SS}. When the write protect pin is connected to Vcc, the write protection feature is enabled and operates as shown in the following table.

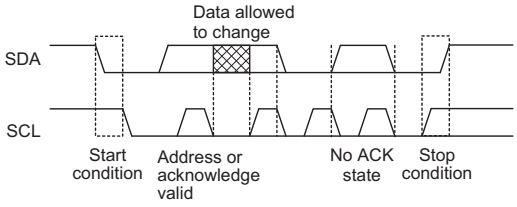
WP Pin Status	Protect Array
At V_{CC}	Full Array (2K)
At V_{SS}	Normal Read/Write Operations

Memory Organization

- HT24LC02, 2K Serial EEPROM
  Internally organized with 256 8-bit words, the 2K requires an 8-bit data word address for random word addressing.

Device Operations

- Clock and data transition
  Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever the clock line is high. Changes in data line while the clock line is high will be interpreted as a START or STOP condition.
- Start condition
  A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition Timing diagram).
- Stop condition
  A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition Timing Diagram).
- Acknowledge
  All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.



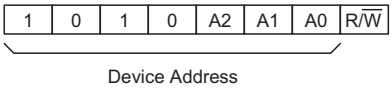
Device Addressing

The 2K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation. The device address word consist of a mandatory one, zero sequence for the first four most significant bits (refer to the diagram showing the Device Address). This is common to all the EEPROM device.

The next three bits are the A2, A1 and A0 device address bits for the 2K EEPROM. These three bits must compare to their corresponding hard-wired input pins.

The 8th bit of device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

If the comparison of the device address succeed the EEPROM will output a zero at ACK bit. If not, the chip will return to a standby state.



Write Operations

- Byte write
  A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. After receiving the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle to the non-volatile memory. All inputs are disabled during this write cycle and EEPROM will not respond until the write is completed (refer to Byte write timing).

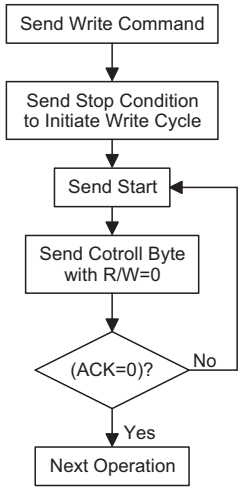
- Page write

  The 2K EEPROM is capable of an 8-byte page write. A page write is initiated the same as byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges the receipt of the first data word, the microcontroller can transmit up to seven more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition.
  The data word address lower three (2K) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location (refer to Page write timing).

- Acknowledge polling
  To maximise bus throughput, one technique is to allow the master to poll for an acknowledge signal after the start condition and the control byte for a write command have been sent. If the device is still busy implementing its write cycle, then no ACK will be returned. The master can send the next read/write command when the ACK signal has finally been received.

- Write protect
  The HT24LC02 has a write-protect function and programming will then be inhibited when the WP pin is connected to VCC. Under this mode, the HT24LC02 is used as a serial ROM.

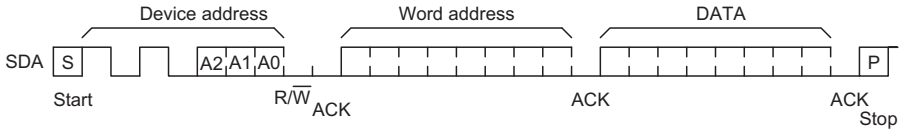
- Read operations
  The HT24LC02 supports three read operations, namely, current address read, random address read and sequential read. During read operation execution, the read/write select bit should be set to ″1″.



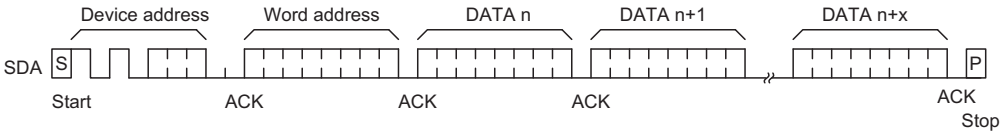
Acknowledge Polling Flow

- Current address read
  The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll over during read from the last byte of the last memory page to the first byte of the first page. The address roll over during write from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller should respond a No ACK (High) signal and following stop condition (refer to Current read timing).

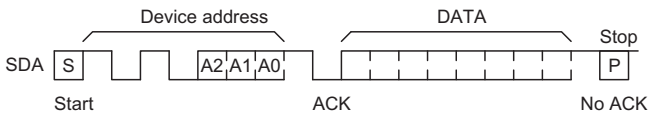
Byte Write Timing



Page Write Timing



Current Read Timing



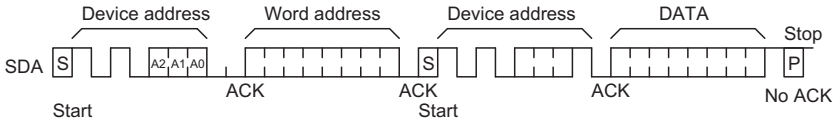
- Random read

  A random read requires a dummy byte write sequence to load in the data word address which is then clocked in and acknowledged by the EEPROM. The microcontroller must then generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller should respond with a ″no ACK″ signal (high) followed by a stop condition. (refer to Random read timing).

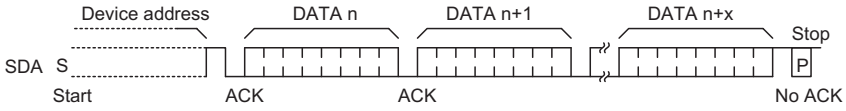
- Sequential read

  Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledgment. As long as the EEPROM receives an acknowledgment, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll over and the sequential read continues. The sequential read operation is terminated when the microcontroller responds with a ″no ACK″ signal (high) followed by a stop condition.

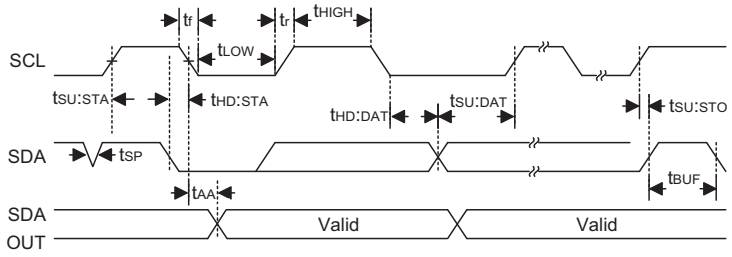
Random Read Timing

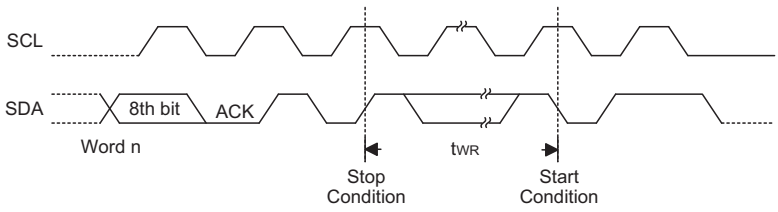


Sequential Read Timing



Timing Diagrams

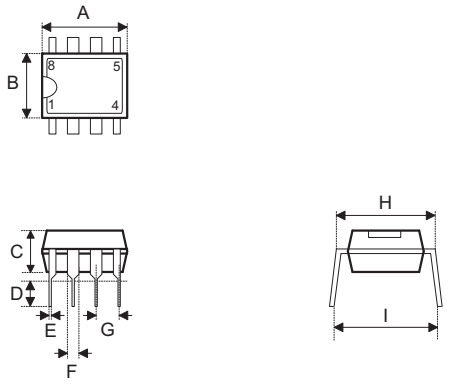




Note: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the valid start condition of sequential command.

Package Information

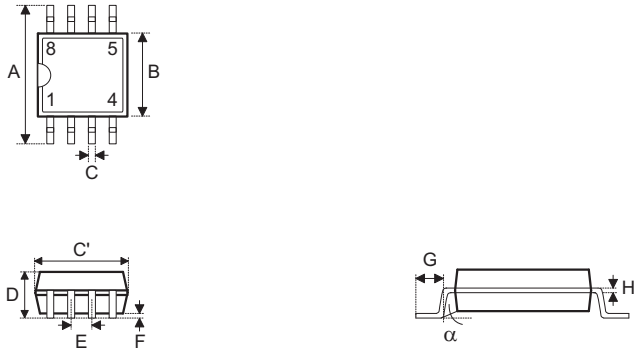
8-pin DIP (300mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.355	—	0.375
B	0.240	—	0.260
C	0.125	—	0.135
D	0.125	—	0.145
E	0.016	—	0.020
F	0.050	—	0.070
G	—	0.100	—
H	0.295	—	0.315
I	—	0.375	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	9.02	—	9.53
B	6.10	—	6.60
C	3.18	—	3.43
D	3.18	—	3.68
E	0.41	—	0.51
F	1.27	—	1.78
G	—	2.54	—
H	7.49	—	8.00
I	—	9.53	—

8-pin SOP (150mil) Outline Dimensions

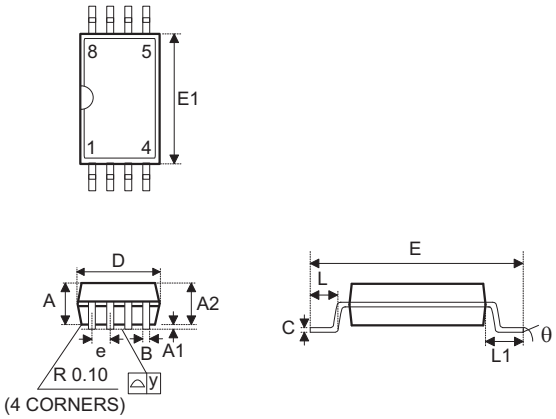


• MS-012

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.228	—	0.244
B	0.150	—	0.157
C	0.012	—	0.020
C′	0.188	—	0.197
D	—	—	0.069
E	—	0.050	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.007	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	5.79	—	6.20
B	3.81	—	3.99
C	0.30	—	0.51
C′	4.78	—	5.00
D	—	—	1.75
E	—	1.27	—
F	0.10	—	0.25
G	0.41	—	1.27
H	0.18	—	0.25
α	0°	—	8°

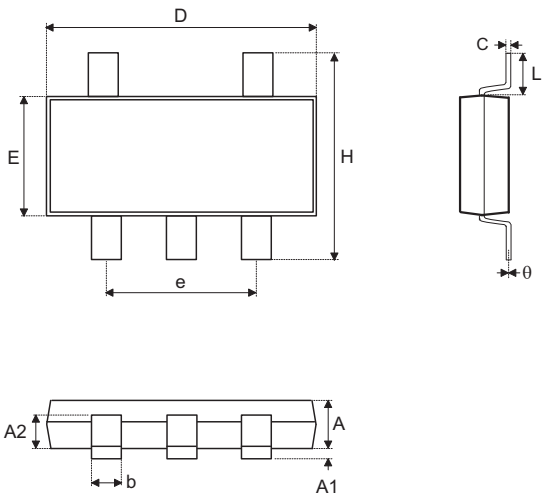
8-pin TSSOP Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.041	—	0.047
A1	0.002	—	0.006
A2	0.031	—	0.041
B	—	0.010	—
C	0.004	—	0.006
D	0.114	—	0.122
E	0.244	—	0.260
E1	0.169	—	0.177
e	—	0.026	—
L	0.020	—	0.028
L1	0.035	—	0.043
y	—	—	0.004
θ	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	1.05	—	1.20
A1	0.05	—	0.15
A2	0.80	—	1.05
B	—	0.25	—
C	0.11	—	0.15
D	2.90	—	3.10
E	6.20	—	6.60
E1	4.30	—	4.50
e	—	0.65	—
L	0.50	—	0.70
L1	0.90	—	1.10
y	—	—	0.10
θ	0°	—	8°

5-pin SOT23-5 Outline Dimensions

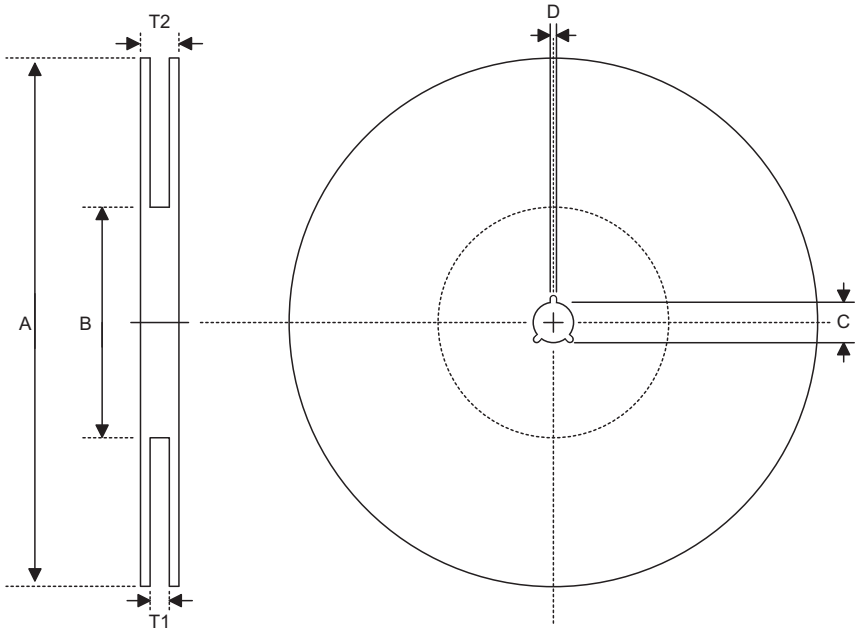


Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.039	—	0.051
A1	—	—	0.004
A2	0.028	—	0.035
b	0.014	—	0.020
C	0.004	—	0.010
D	0.106	—	0.122
E	0.055	—	0.071
e	—	0.075	—
H	0.102	—	0.118
L	0.015	—	—
θ	0°	—	9°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	1.00	—	1.30
A1	—	—	0.10
A2	0.70	—	0.90
b	0.35	—	0.50
C	0.10	—	0.25
D	2.70	—	3.10
E	1.40	—	1.80
e	—	1.90	—
H	2.60	—	3.00
L	0.37	—	—
θ	0°	—	9°

Product Tape and Reel Specifications

Reel Dimensions



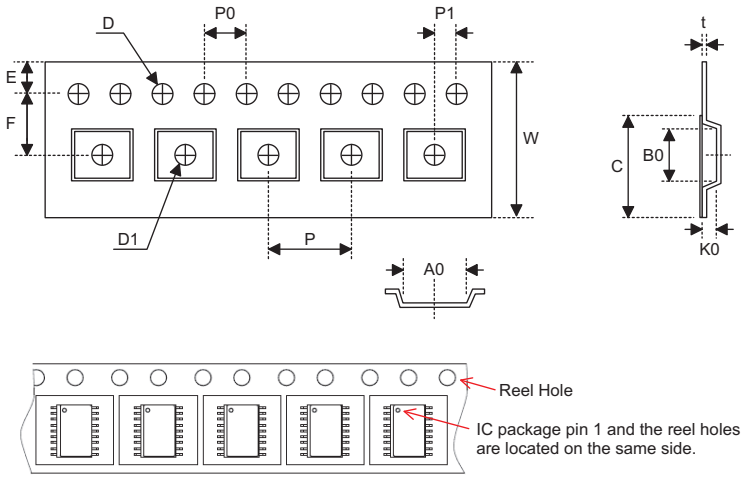
SOP 8N, TSSOP 8L

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	$13.0^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	$12.8^{+0.3/-0.2}$
T2	Reel Thickness	18.2±0.2

SOT23-5

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	178.0±1.0
B	Reel Inner Diameter	62.0±1.0
C	Spindle Hole Diameter	13.0±0.2
D	Key Slit Width	2.50±0.25
T1	Space Between Flange	$8.4^{+1.5/-0.0}$
T2	Reel Thickness	$11.4^{+1.5/-0.0}$

Carrier Tape Dimensions



SOP 8N

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	$12.0^{+0.3/-0.1}$
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	5.5±0.1
D	Perforation Diameter	1.55±0.10
D1	Cavity Hole Diameter	1.50+0.25
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.4±0.1
B0	Cavity Width	5.2±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	9.3±0.1

TSSOP 8L

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	$12.0^{+0.3/-0.1}$
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.10
F	Cavity to Perforation (Width Direction)	5.5±0.5
D	Perforation Diameter	$1.5^{+0.1/-0.0}$
D1	Cavity Hole Diameter	$1.5^{+0.1/-0.0}$
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	7.0±0.1
B0	Cavity Width	3.6±0.1
K0	Cavity Depth	1.6±0.1
t	Carrier Tape Thickness	0.300±0.013
C	Cover Tape Width	9.3±0.1

SOT23-5

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	8.0±0.3
P	Cavity Pitch	4.0±0.1
E	Perforation Position	1.75±0.10
F	Cavity to Perforation (Width Direction)	3.50±0.05
D	Perforation Diameter	$1.5^{+0.1/-0.0}$
D1	Cavity Hole Diameter	$1.5^{+0.1/-0.0}$
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.00±0.05
A0	Cavity Length	3.15±0.10
B0	Cavity Width	3.2±0.1
K0	Cavity Depth	1.4±0.1
t	Carrier Tape Thickness	0.20±0.03
C	Cover Tape Width	5.3±0.1

Holtek Semiconductor Inc. (Headquarters)
No.3, Creation Rd. II, Science Park, Hsinchu, Taiwan
Tel: 886-3-563-1999
Fax: 886-3-563-1189
http://www.holtek.com.tw

Holtek Semiconductor Inc. (Taipei Sales Office)
4F-2, No. 3-2, YuanQu St., Nankang Software Park, Taipei 115, Taiwan
Tel: 886-2-2655-7070
Fax: 886-2-2655-7373
Fax: 886-2-2655-7383 (International sales hotline)

Holtek Semiconductor Inc. (Shenzhen Sales Office)
5F, Unit A, Productivity Building, No.5 Gaoxin M 2nd Road, Nanshan District, Shenzhen, China 518057
Tel: 86-755-8616-9908, 86-755-8616-9308
Fax: 86-755-8616-9722

Holtek Semiconductor (USA), Inc. (North America Sales Office)
46729 Fremont Blvd., Fremont, CA 94538, USA
Tel: 1-510-252-9880
Fax: 1-510-252-9885
http://www.holtek.com

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