HT16D595
8-Bit Constant Current LED Driver

Feature

- Logic supply voltage: 3.3V~5.5V
- 8-channel constant current output
- Channel output current is fixed at 48mA
- Build-in current setting resistor
- High output current accuracy:
  Variation between chips is less than ±6%
- Up to 25MHz serial interface clock frequency
- Maximum output terminal voltage 17V
- Schmitt trigger input structure
- 16-pin NSOP package

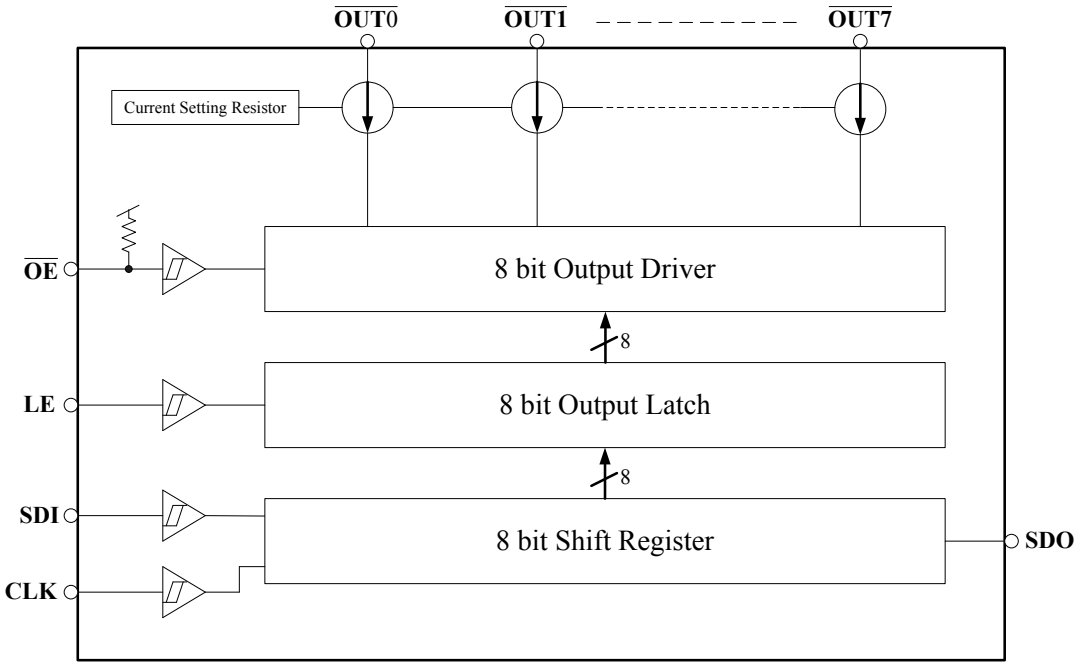
Applications

- LED Display
- Digital clock, thermometer, counter, voltmeter
- Other consumer application

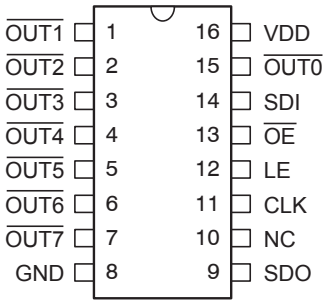
General Description

The HT16D595 is a high accuracy constant current driver which is specifically designed for LED display applications. The device provides 8-channel stable and constant current outputs for driving LEDs which may have different forward voltage characteristics, VF, due to process variations. Communication with the outside world is catered for by including a fully integrated serial interface function, which provides designers with a means of easy communication with external peripheral hardware. In this way, many devices can be cascaded together to drive larger LED displays. Furthermore, with this serial-to-serial or serial-to-parallel structure, the device is very suitable as a replacement for the 74HC595, in applications and related products which include an 8-bit serial input and serial or parallel output.

Block Diagram



Pin Assignment



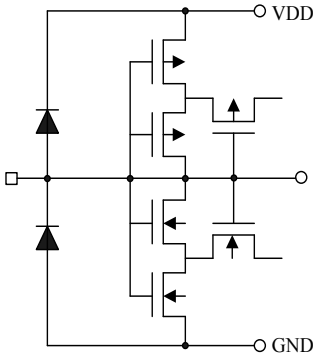
HT16D595
16 NSOP-A

Pin Description

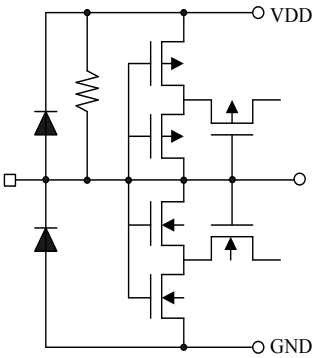
Pin Name	I/O	Description
VDD	—	Power supply
GND	—	Ground
SDI	I	Serial data input
CLK	I	Clock input. Each data bit is shifted in to the shift register on the rising edge of the input clock signal.
LE	I	Data Latch control. Data will be latched into the internal register on high level on the LE pin.
$\overline{OE}$	O	Output enable control: 1: all outputs disabled 0: all outputs enabled
SDO	O	Serial data output
$\overline{OUT0}$~$\overline{OUT7}$	O	Parallel data output

Generic Input / Output Structure

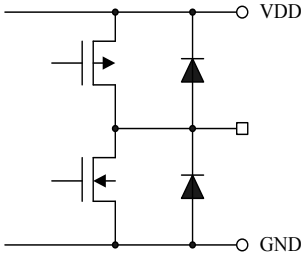
SDI,CLK, LE



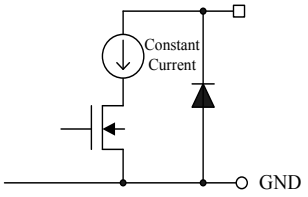
$\overline{OE}$



SDO



$\overline{OUT0}$~$\overline{OUT7}$



Absolute Maximum Ratings

Logic Supply Voltage (VDD) ..... VGND-0.3V to VGND+6.0V
Logic Input Voltage ..... VGND-0.3V to VDD+0.3V
Output Voltage 20V
Output Current 60mA
GND Terminal Current..... 450mA
Storage Temperature ..... -55°C to 150°C
Operating Temperature..... -40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25ºC

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Logic Supply Voltage	—	—	3.3	5.0	5.5	V
V_{OUT}	Output Voltage	5V	$\overline{OUT0}$~$\overline{OUT7}$	—	—	17	V
V_{IH}	High Input Voltage	5V	SDI, CLK	0.7V_{DD}	—	V_{DD}	V
V_{IL}	Low Input Voltage	5V	SDI, CLK	0	—	0.3V_{DD}	V
V_{OH}	High-Level Output Voltage	5V	SDO, I_{OUT}=-4mA	4.6	—	—	V
V_{OL}	Low-Level Output Voltage	5V	SDO, I_{OUT}=+4mA	—	—	0.4	V
I_{OZ}	Output Leakage Current	5V	V_{DS}=17V	—	—	0.5	μA
I_{OUT}	Output Current	5V	V_{DS}=1V	—	48	—	mA
dI_{OUT2}	Current Skew(chip)	5V	V_{DS}=1V	—	±3	±6	%
%/dV_{DS}	Output Current VS Output Voltage Regulation	5V	V_{DS} within 1.0V and 3.0V	—	±0.5	±1	%/V
%/dV_{DD}	Output Current VS Supply Voltage Regulation	—	V_{DD} within 4.5V and 5.5V	—	±1	±2	%/V
R_{PU}	Pull High Resistance	5V	$\overline{OE}$	250	500	800	KΩ
I_{DD1}	Supply Current	5V	$\overline{OUT0}$~$\overline{OUT7}$=off	—	3	4.5	mA
I_{DD2}	Supply Current	5V	$\overline{OUT0}$~$\overline{OUT7}$=on	—	3.5	5.3	mA

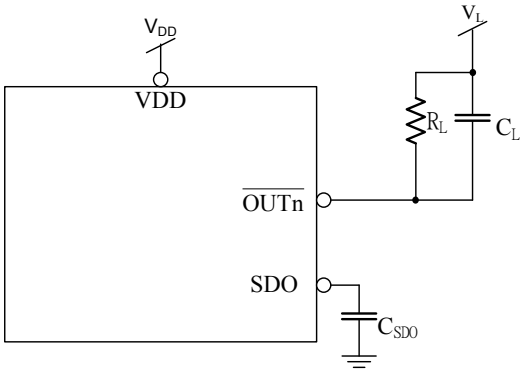
A.C. Characteristics

Ta=25°C

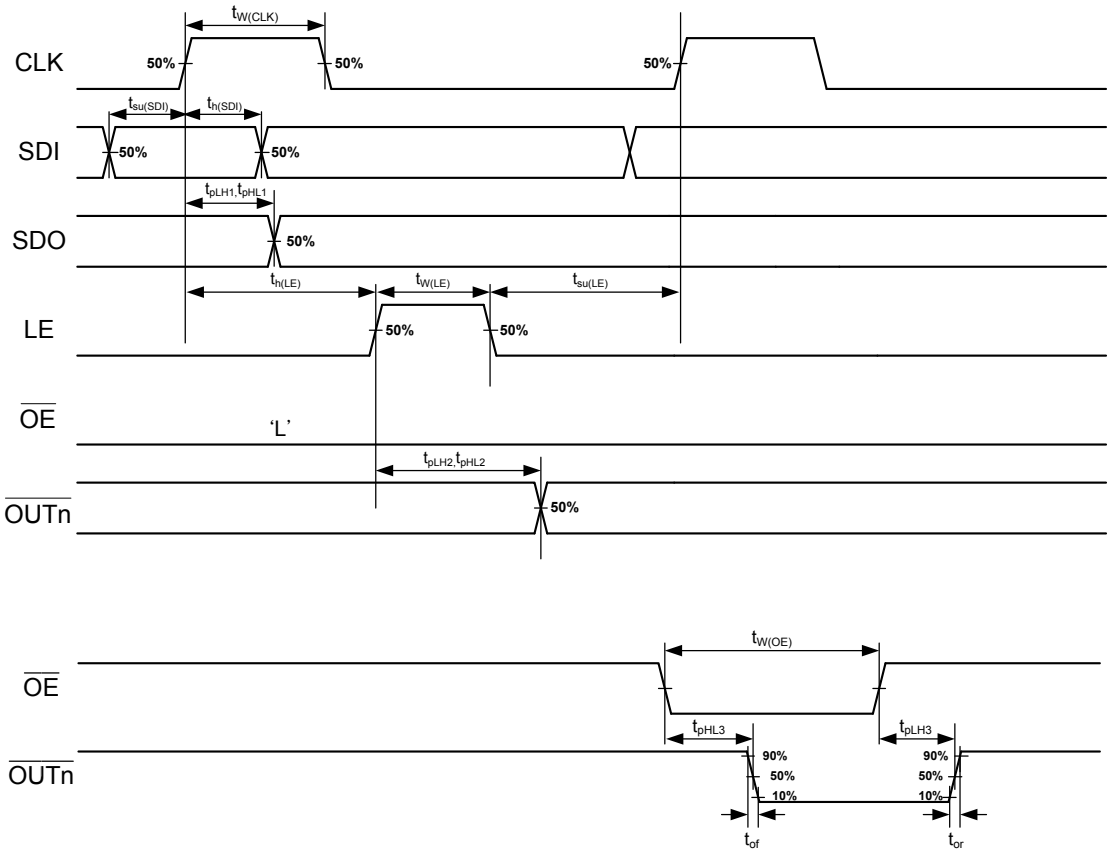
Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
t_{pLH1}	Propagation Delay Time (“L” to “H”, CLK→SDO)	5V	V_{DS}=0.9V V_{IH}=VDD V_{IL}=GND V_L=4V R_L=62Ω C_L=10pF C_{SDO} = 50pF	—	17	25	ns
t_{pLH2}	Propagation Delay Time (“L” to “H”, LE→$\overline{OUTn}$)	5V		—	200	250	ns
t_{pLH3}	Propagation Delay Time (“L” to “H”, $\overline{OE}$→$\overline{OUTn}$)	5V		—	200	250	ns
t_{pHL1}	Propagation Delay Time (“H” to “L”, CLK→SDO)	5V		—	17	25	ns
t_{pHL2}	Propagation Delay Time (“H” to “L”, LE→$\overline{OUTn}$)	5V		—	150	200	ns
t_{pHL3}	Propagation Delay Time (“H” to “L”, $\overline{OE}$→$\overline{OUTn}$)	5V		—	150	200	ns
$t_{W(CLK)}$	Pulse Width	5V		10	—	—	ns
$t_{W(LE)}$	Pulse Width	5V		10	—	—	ns
$t_{W(OE)}$	Pulse Width	5V		300	—	—	ns
$t_{h(LE)}$	Hold Time For LE	5V		7	—	—	ns
$t_{su(LE)}$	Setup Time For LE	5V		10	—	—	ns
$t_{h(SDI)}$	Hold Time For SDI	5V		5	—	—	ns
$t_{su(SDI)}$	Setup Time For SDI	5V		3	—	—	ns
f_{CLK}	Clock Frequency	5V	Cascade operation	—	—	25	MHz
t_r	Maximum CLK Rise Time	5V	(Note1)	—	—	500	ns
t_f	Maximum CLK Fall Time	5V		—	—	500	ns
t_{or}	Output Rise Time of V_{OUT}	5V		—	70	200	ns
t_{of}	Output Fall Time of V_{OUT}	5V		—	40	120	ns

Note 1: If the devices are connected in cascade and if t_r or t_f is large, then these timings may be critical to achieve the correct timings for data transfer between two cascaded devices.

Test Circuit for AC Characteristics



Timing Waveform

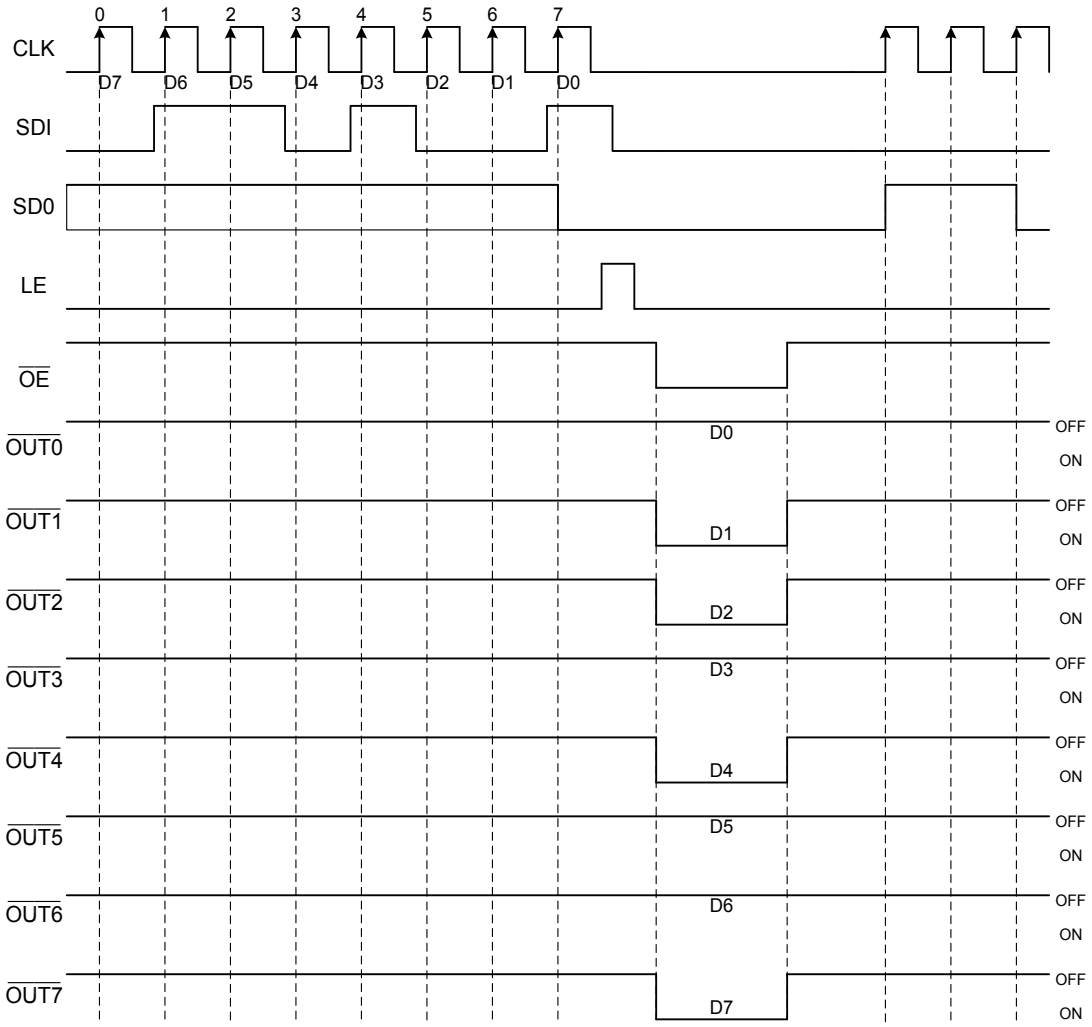


Serial-to-Serial Operation

The serial-to-serial function is implemented using the SDI and SDO pins. The SDI pin is used to receive serial input data for transfer into the LSB of the internal shift register while the SDO pin is used to transmit the MSB of the internal shift register to cascaded devices. Each bit of the data is shifted in from the SDI pin into the register on the rising edge of the CLK input signal where it will become the LSB of the internal shift register. At the same time, the SDO pin will shift out the MSB in the shift register to any connected cascaded devices.

Serial-to-Parallel Output Operation

If the LE pin is high, then data will be latched from the shift register into an internal latch for transfer to the OUT pins. Data from the internal latch is transferred to the OUT pins using the OE pin. If the OE pin is low, then the data in the shift register will be transmitted to the output pins. The OUT pins can be disabled by setting the OE pin to a high level. The SDO pin will not be affected by the LE or OE pin status. The following timing diagram illustrates the serial-to-serial and serial-to-parallel operational waveform.

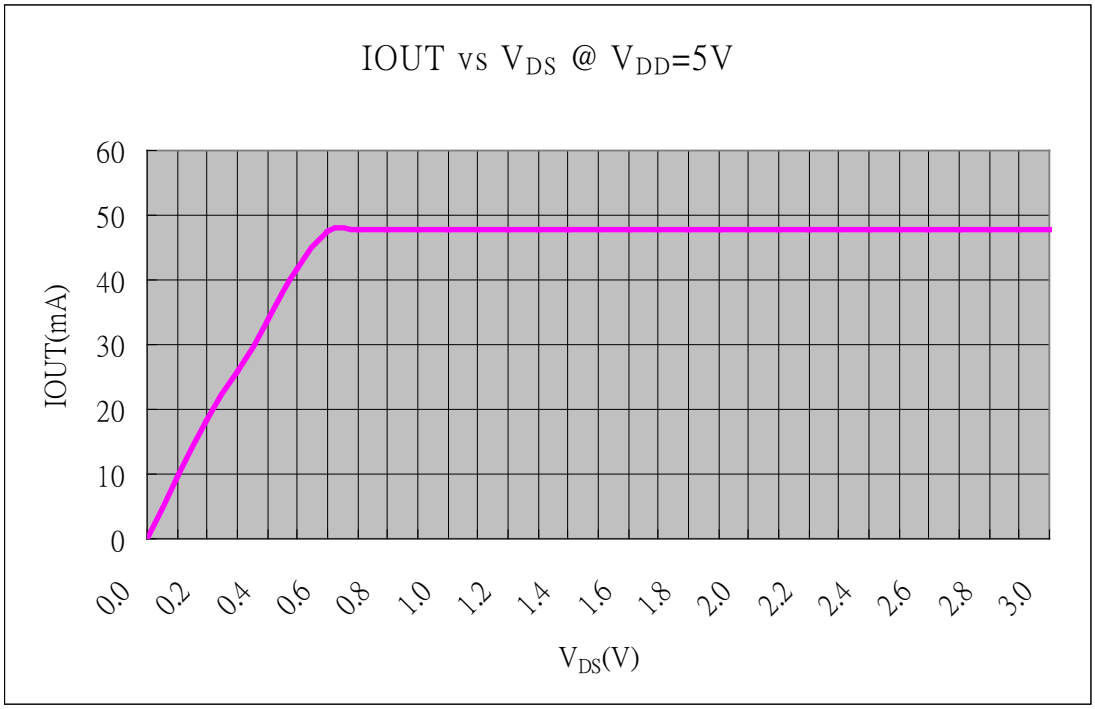


Truth Table

CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}$...$\overline{OUT3}$...$\overline{OUT7}$	SDO
↑	H	L	D_n	D_n....D_{n-3}....D_{n-7}	D_{n-7}
↑	L	L	D_{n+1}	No Change	D_{n-6}
↑	H	L	D_{n+2}	D_{n+2}....D_{n-1}....D_{n-5}	D_{n-5}
↓	X	L	D_{n+3}	D_{n+2}....D_{n-1}....D_{n-5}	D_{n-5}
↓	X	H	D_{n+3}	Off	D_{n-5}

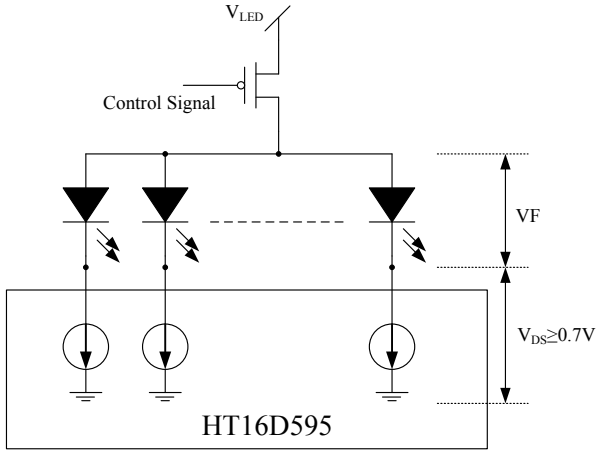
Constant Current Output

The output constant current is fixed at 48mA for the 8 output channels. The constant current variation between devices is less than ±6%.

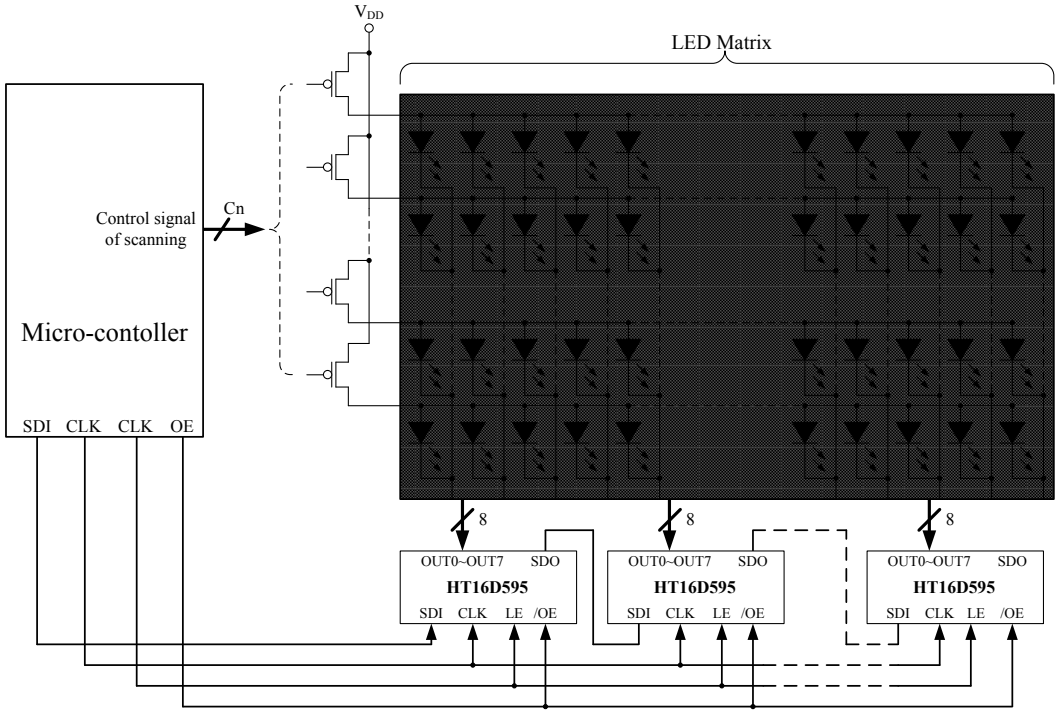


Load Supply Voltage (V_{LED})

HT16D595 can be operated very well when V_{DS} is set from 0.7V to 2V. It is recommended to use the lowest supply voltage (V_{LED}) to reduce the V_{DS} value in order to lower both the power consumption of HT16D595 and IC temperature.

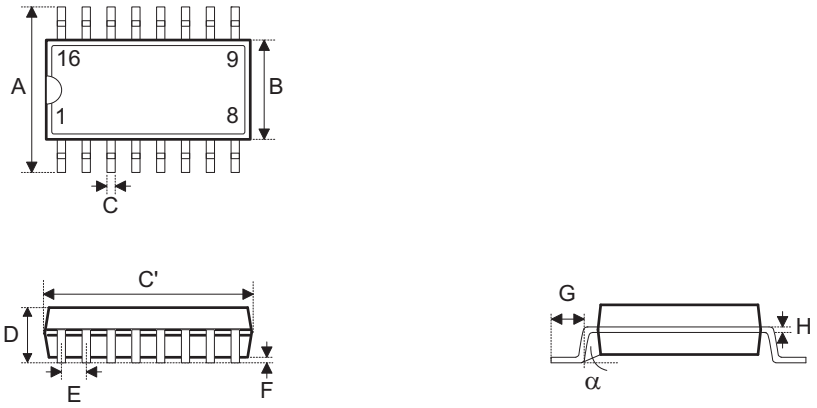


Application Circuit



Package Information

16-pin NSOP (150mil) Outline Dimensions



MS-012

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.228	—	0.244
B	0.150	—	0.157
C	0.012	—	0.020
C'	0.386	—	0.402
D	—	—	0.069
E	—	0.050	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.007	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	5.79	—	6.20
B	3.81	—	3.99
C	0.30	—	0.51
C'	9.80	—	10.21
D	—	—	1.75
E	—	1.27	—
F	0.10	—	0.25
G	0.41	—	1.27
H	0.18	—	0.25
α	0°	—	8°

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