PATENTED

PAT No. : 099352

Technical Document

- Application Note

Features

- Operating voltage: 2.7V~5.2V
- Built-in RC oscillator
- External 32.768kHz crystal or 32kHz frequency source input
- 1/5 bias, 1/16 duty, frame frequency is 64Hz
- Max. 48×16 patterns, 16 commons, 48 segments
- Built-in internal resistor type bias generator
- 3-wire serial interface
- 8 kinds of time base or WDT selection
- Time base or WDT overflow output
- Built-in LCD display RAM
- R/W address auto increment
- Two selection buzzer frequencies (2kHz or 4kHz)
- Power down command reduces power consumption
- Software configuration feature
- Data mode and Command mode instructions
- Three data accessing modes
- VLCD pin to adjust LCD operating voltage
- 100-pin QFP package

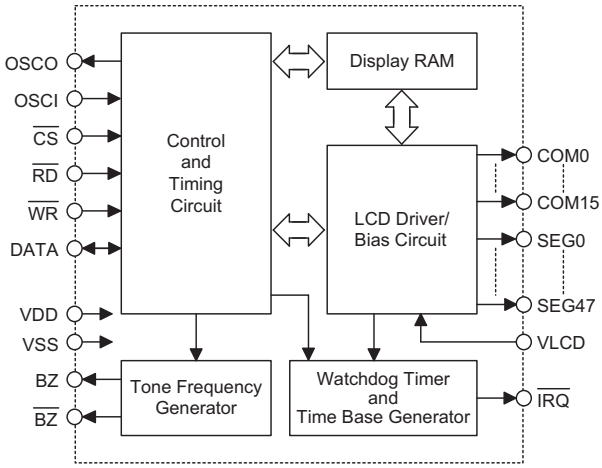
General Description

HT1626 is a peripheral device specially designed for I/O type MCU used to expand the display capability. The max. display segment of the device are 768 patterns (48×16). It also supports serial interface, buzzer sound, Watchdog Timer or time base timer functions. The HT1626 is a memory mapping and multi-function LCD controller. The software configuration feature of the HT1626 make it suitable for multiple LCD applications including LCD modules and display subsystems. Only three lines are required for the interface between the host controller and the HT1626. The HT162X series have many kinds of products that match various applications.

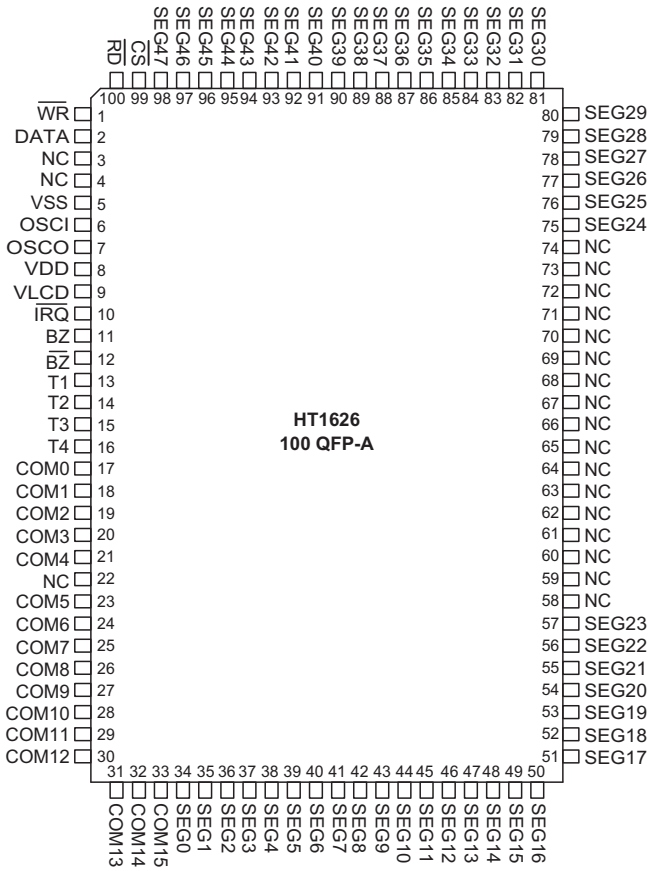
Selection Table

HT162X	HT1620	HT1621	HT1622	HT16220	HT1623	HT1625	HT1626
COM	4	4	8	8	8	8	**16**
SEG	32	32	32	32	48	64	**48**
Built-in Osc.	—	√	√	—	√	√	√
Crystal Osc.	√	√	—	√	√	√	√

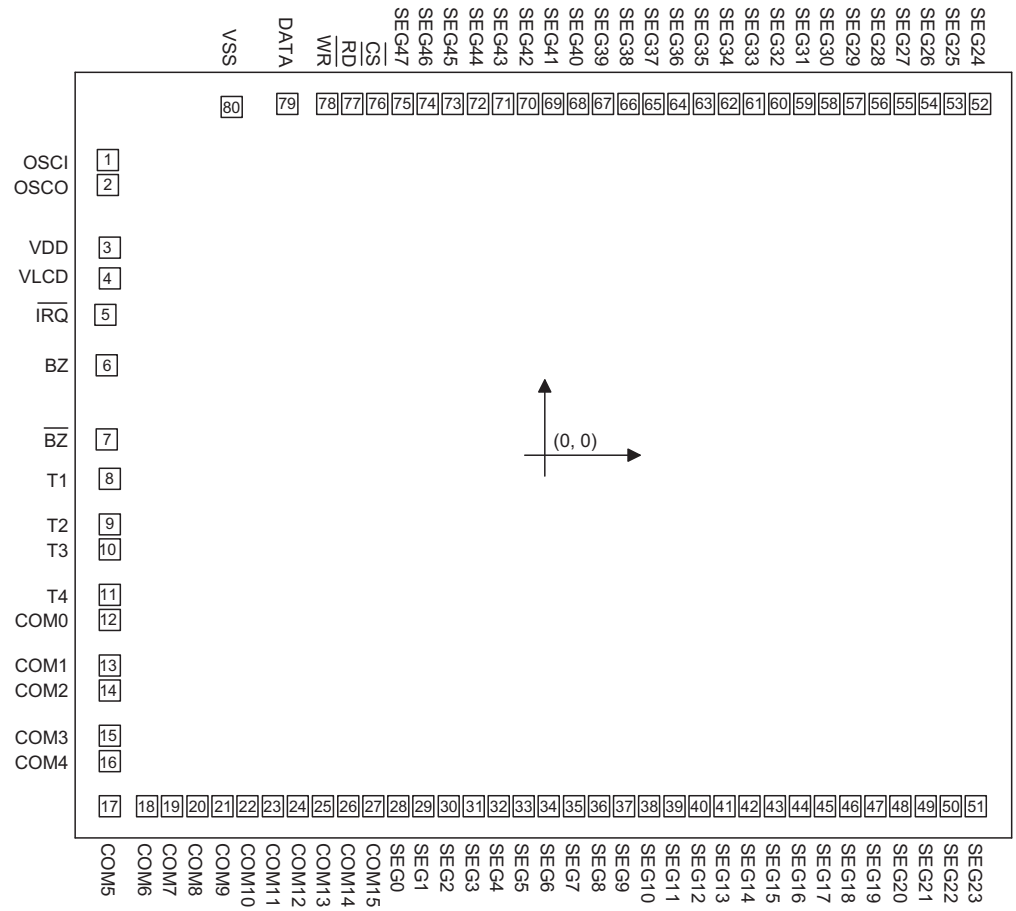
Block Diagram



Pin Assignment



Pad Assignment



Chip size: 148 × 123 (mil)^2

* The IC substrate should be connected to VDD in the PCB layout artwork.

Pad Coordinates

Unit: μm

Pad No.	X	Y	Pad No.	X	Y
1	–1745.115	1195.533	41	729.836	–1455.425
2	–1745.115	1096.513	42	828.935	–1455.425
3	–1744.679	775.806	43	927.956	–1455.425
4	–1744.765	651.256	44	1027.055	–1455.425
5	–1751.917	505.882	45	1126.075	–1455.425
6	–1746.120	308.253	46	1225.175	–1455.425
7	–1746.120	19.855	47	1324.196	–1455.425
8	–1744.765	–131.999	48	1423.294	–1455.425
9	–1744.765	–317.380	49	1522.315	–1455.425
10	–1744.765	–416.479	50	1621.415	–1455.425
11	–1744.765	–601.860	51	1720.436	–1455.425
12	–1744.765	–700.959	52	1766.902	1453.104
13	–1744.765	–886.341	53	1667.883	1453.104
14	–1744.765	–985.440	54	1568.782	1453.104
15	–1744.765	–1170.821	55	1469.762	1453.104
16	–1744.765	–1269.919	56	1370.662	1453.104
17	–1744.765	–1455.300	57	1271.642	1453.104
18	–1548.505	–1455.425	58	1172.542	1453.104
19	–1449.484	–1455.425	59	1073.522	1453.104
20	–1350.385	–1455.425	60	974.422	1453.104
21	–1251.365	–1455.425	61	875.402	1453.104
22	–1152.266	–1455.425	62	776.302	1453.104
23	–1053.245	–1455.425	63	677.282	1453.104
24	–954.146	–1455.425	64	578.182	1453.104
25	–855.125	–1455.425	65	479.163	1453.104
26	–756.026	–1455.425	66	380.062	1453.104
27	–657.005	–1455.425	67	281.042	1453.104
28	–557.906	–1455.425	68	181.943	1453.104
29	–458.885	–1455.425	69	82.923	1453.104
30	–359.786	–1455.425	70	–16.177	1453.104
31	–260.764	–1455.425	71	–115.197	1453.104
32	–161.665	–1455.425	72	–214.298	1453.104
33	–62.645	–1455.425	73	–313.318	1453.104
34	36.454	–1455.425	74	–412.417	1453.104
35	135.475	–1455.425	75	–511.438	1453.104
36	234.574	–1455.425	76	–610.536	1453.104
37	333.596	–1455.425	77	–709.557	1453.104
38	432.695	–1455.425	78	–808.656	1453.104
39	531.716	–1455.425	79	–977.680	1453.104
40	630.815	–1455.425	80	–1207.287	1453.629

Pad Description

Pad No.	Pad Name	I/O	Description
1	OSCI	I	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open.
2	OSCO	O	
3	VDD	—	Positive power supply
4	VLCD	I	LCD operating voltage input pad.
5	$\overline{IRQ}$	O	Time base or Watchdog Timer overflow flag, NMOS open drain output
6, 7	BZ, $\overline{BZ}$	O	2kHz or 4kHz tone frequency output pair
8~11	T1~T4	I	Not connected
12~27	COM0~COM15	O	LCD common outputs
28~75	SEG0~SEG47	O	LCD segment outputs
76	$\overline{CS}$	I	Chip selection input with pull-high resistor. When the $\overline{CS}$ is logic high, the data and command read from or write to the HT1626 are disabled. The serial interface circuit is also reset. But if the $\overline{CS}$ is at logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the HT1626 are all enabled.
77	$\overline{RD}$	I	READ clock input with pull-high resistor. Data in the RAM of the HT1626 are clocked out on the falling edge of the $\overline{RD}$ signal. The clocked out data will appear on the data line. The host controller can use the next rising edge to latch the clocked out data.
78	$\overline{WR}$	I	WRITE clock input with pull-high resistor. Data on the DATA line are latched into the HT1626 on the rising edge of the $\overline{WR}$ signal.
79	DATA	I/O	Serial data input or output with pull-high resistor
80	VSS	—	Negative power supply, ground

Absolute Maximum Ratings

Supply Voltage .....–0.3V to 5.5V

Input Voltage.....V_{SS}–0.3V to V_{DD}+0.3V

Storage Temperature .....–50°C to 125°C

Operating Temperature.....–25°C to 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.7	—	5.2	V
I_{DD1}	Operating Current	3V	No load or LCD ON On-chip RC oscillator	—	155	310	μA
		5V		—	260	420	μA
I_{DD2}	Operating Current	3V	No load or LCD ON Crystal oscillator	—	150	310	μA
		5V		—	250	420	μA
I_{DD11}	Operating Current	3V	No load or LCD OFF On-chip RC oscillator	—	8	30	μA
		5V		—	20	60	μA
I_{DD22}	Operating Current	3V	No load or LCD OFF Crystal oscillator	—	—	20	μA
		5V		—	—	35	μA
I_{STB}	Standby Current	3V	No load, Power down mode	—	1	12	μA
		5V		—	2	24	μA
V_{IL}	Input Low Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	0	—	0.6	V
		5V		0	—	1.0	V
V_{IH}	Input High Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	2.4	—	3.0	V
		5V		4.0	—	5.0	V
I_{OL1}	BZ, $\overline{BZ}$, $\overline{IRQ}$	3V	V_{OL}=0.3V	0.9	1.8	—	mA
		5V	V_{OL}=0.5V	1.7	3.0	—	mA
I_{OH1}	BZ, $\overline{BZ}$	3V	V_{OH}=2.7V	–0.9	–1.8	—	mA
		5V	V_{OH}=4.5V	–1.7	–3.0	—	mA
I_{OL2}	DATA	3V	V_{OL}=0.3V	0.9	1.8	—	mA
		5V	V_{OL}=0.5V	1.7	3.0	—	mA
I_{OH2}	DATA	3V	V_{OH}=2.7V	–0.9	–1.8	—	mA
		5V	V_{OH}=4.5V	–1.7	–3.0	—	mA
I_{OL3}	LCD Common Sink Current	3V	V_{OL}=0.3V	80	160	—	μA
		5V	V_{OL}=0.5V	180	360	—	μA
I_{OH3}	LCD Common Source Current	3V	V_{OH}=2.7V	–40	–80	—	μA
		5V	V_{OH}=4.5V	–90	–180	—	μA
I_{OL4}	LCD Segment Sink Current	3V	V_{OL}=0.3V	50	100	—	μA
		5V	V_{OL}=0.5V	120	240	—	μA
I_{OH4}	LCD Segment Source Current	3V	V_{OH}=2.7V	–30	–60	—	μA
		5V	V_{OH}=4.5V	–70	–140	—	μA
R_{PH}	Pull-high Resistor	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	100	200	300	kΩ
		5V		50	100	150	kΩ

A.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS1}	System Clock	5V	On-chip RC oscillator	24	32	40	kHz
f_{SYS2}	System Clock	—	External clock source	—	32	—	kHz
f_{LCD1}	LCD Frame Frequency	5V	On-chip RC oscillator	48	64	80	Hz
f_{LCD2}	LCD Frame Frequency	—	External clock source	—	64	—	Hz
t_{COM}	LCD Common Period	—	n: Number of COM	—	n/f_{LCD}	—	sec
f_{CLK1}	Serial Data Clock ($\overline{WR}$ Pin)	3V	Duty cycle 50%	4	—	150	kHz
		5V		4	—	300	kHz
f_{CLK2}	Serial Data Clock ($\overline{RD}$ Pin)	3V	Duty cycle 50%	—	—	75	kHz
		5V		—	—	150	kHz
t_{CS}	Serial Interface Reset Pulse Width (Figure 3)	—	$\overline{CS}$	500	600	—	ns
t_{CLK}	$\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode	3.34	—	125	μs
			Read mode	6.67	—	—	
		5V	Write mode	1.67	—	125	μs
			Read mode	3.34	—	—	
t_r, t_f	Rise or Fall Time Serial Data Clock Width (Figure 1)	—	—	—	120	160	ns
t_{su}	Setup Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	—	—	60	120	—	ns
t_{su1}	Setup Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	—	—	500	600	—	ns
t_h	Hold Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	—	—	500	600	—	ns
t_{h1}	Hold Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	—	—	50	100	—	ns
f_{TONE}	Tone Frequency (2kHz)	5V	On-chip RC oscillator	1.5	2.0	2.5	kHz
	Tone Frequency (4kHz)			3.0	4.0	5.0	kHz
t_{OFF}	V_{DD} OFF Times (Figure 4)	—	VDD drop down to 0V	20	—	—	ms
t_{SR}	V_{DD} Rising Slew Rate (Figure 4)	—	—	0.05	—	—	V/ms
t_{RSTD}	Delay Time after Reset (Figure 4)	—	—	1	—	—	ms

Note: 1. If the conditions of Power-on Reset timing are not satisfied in power On/Off sequence, the internal Power-on Reset (POR) circuit will not operate normally.

2. If the VDD drops below the minimum voltage of operating voltage spec. during operating, the conditions of Power-on Reset timing must be satisfied also. That is, the VDD must drop to 0V and keep at 0V for 20ms (min.) before rising to the normal operating voltage.

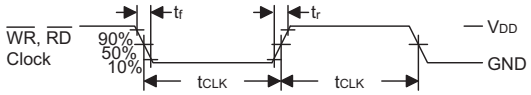


Figure 1

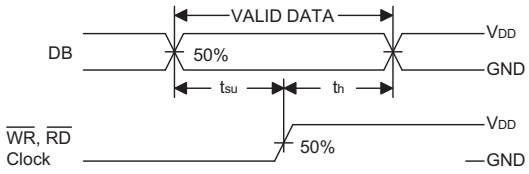


Figure 2

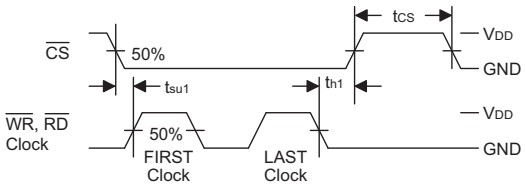


Figure 3

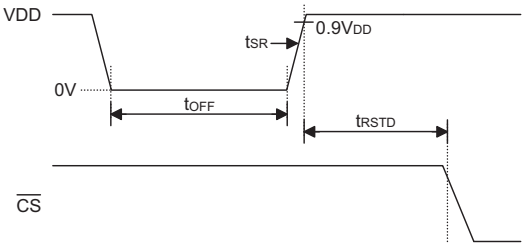


Figure 4. Power-on Reset Timing

Functional Description

Display Memory – RAM Structure

The static display RAM is organized into 192×4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MOD-
IFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.

Time Base and Watchdog Timer – WDT

The time base generator and WDT share the same divided (/256) counter. TIMER DIS/EN/CLR, WDT DIS/EN/CLR and $\overline{IRQ}$ EN/DIS are independent from each other. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will remain at logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued.

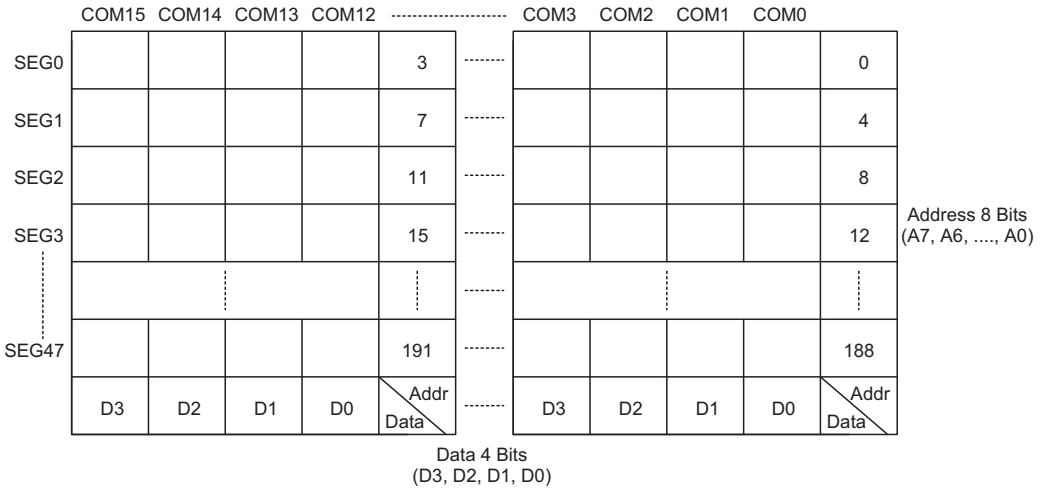
If an external clock is selected as the source of system frequency, the SYS DIS command turns out invalid and the power down mode fails to be carried out until the external clock source is removed.

Buzzer Tone Output

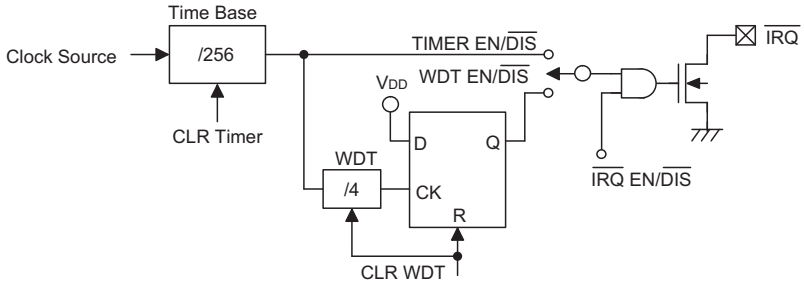
A simple tone generator is implemented in the HT1626. The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$ which are used to generate a single tone.

Command Format

The HT1626 can be configured by the software setting. There are two mode commands to configure the HT1626 resource and to transfer the LCD display data.



RAM Mapping



Timer and WDT Configurations

The following are the data mode ID and the command mode ID:

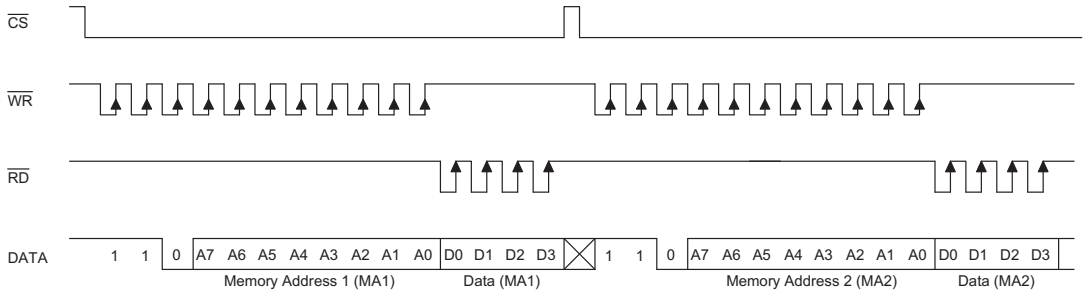
Operation	Mode	ID
READ	Data	1 1 0
WRITE	Data	1 0 1
READ-MODIFY-WRITE	Data	1 0 1
COMMAND	Command	1 0 0

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the $\overline{CS}$ pin should be set to "1", and the previous operation mode will be reset also. The $\overline{CS}$ pin returns to "0", a new operation mode ID should be issued first.

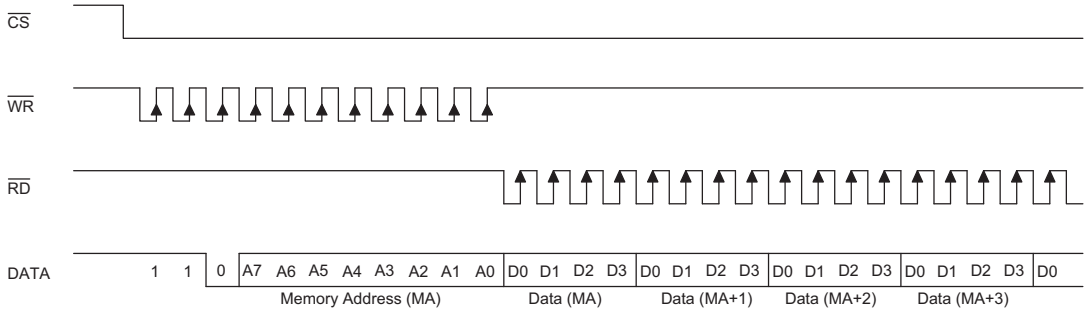
Name	Command Code	Function
TONE OFF	0000-1000-X	Turn-off tone output
TONE 4K	010X-XXXX-X	Turn-on tone output, tone frequency is 4kHz
TONE 2K	0110-XXXX-X	Turn-on tone output, tone frequency is 2kHz

Timing Diagrams

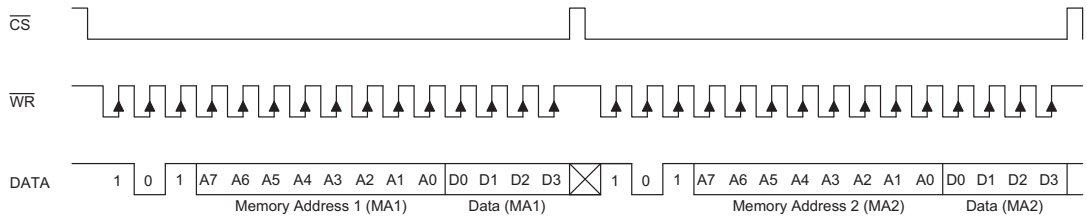
READ Mode (Command Code : 1 1 0)



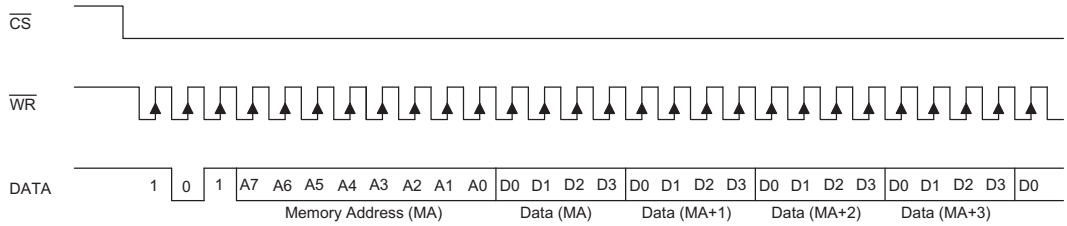
READ Mode (Successive Address Reading)



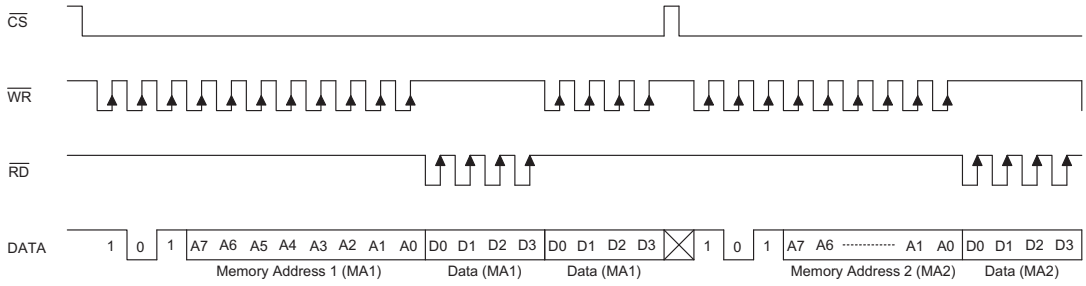
WRITE Mode (Command Code : 1 0 1)



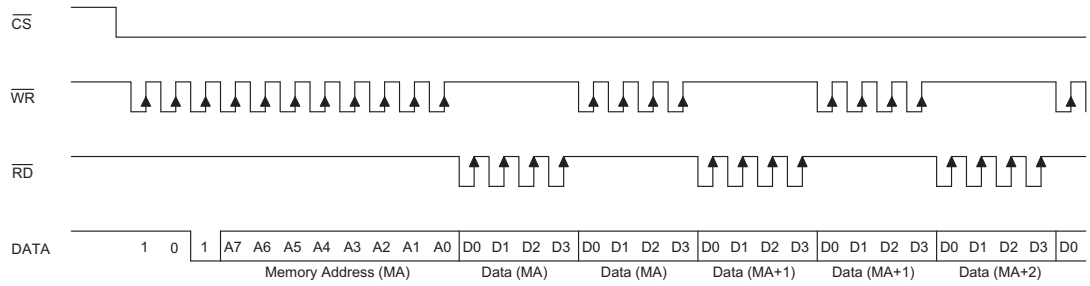
WRITE Mode (Successive Address Writing)



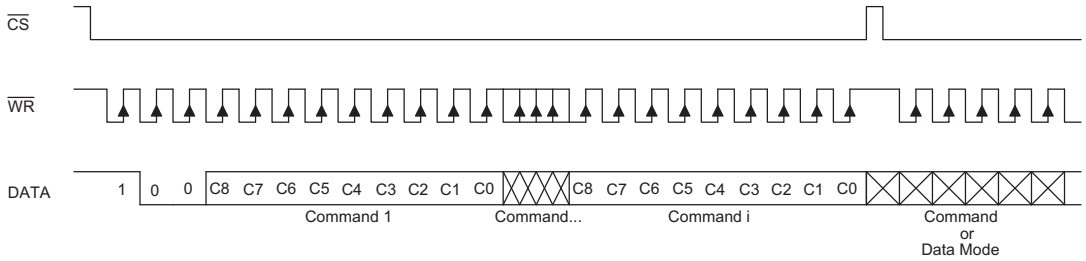
READ-MODIFY-WRITE Mode (Command Code : 1 0 1)



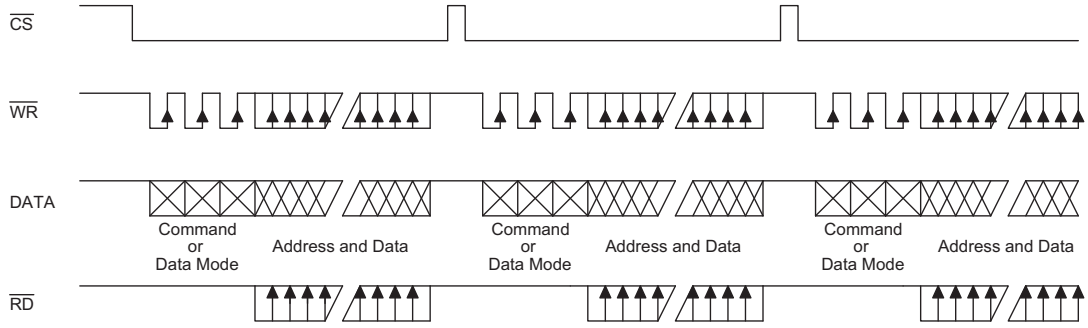
READ-MODIFY-WRITE Mode (Successive Address Accessing)



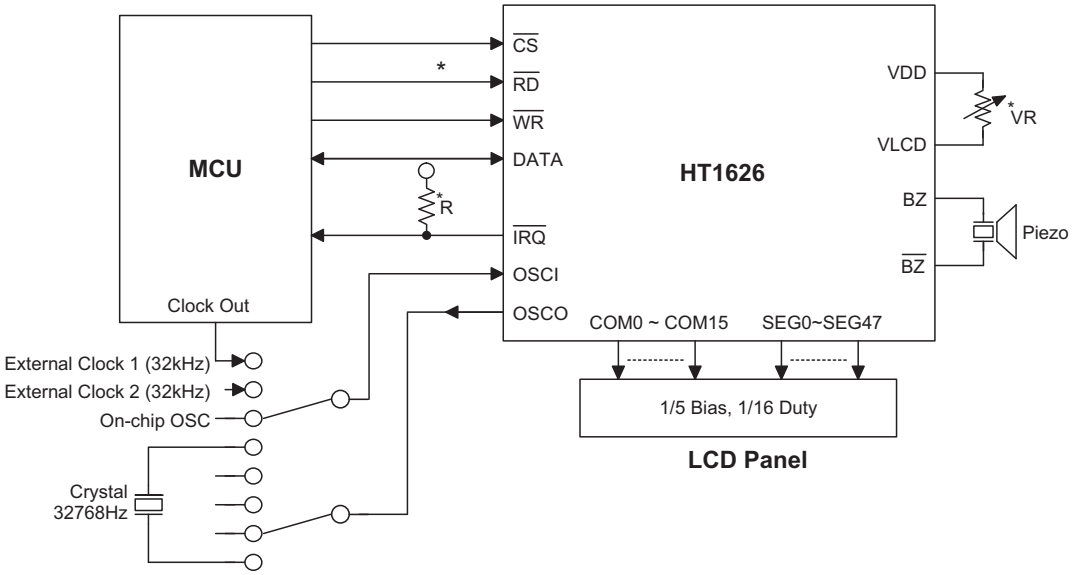
Command Mode (Command Code : 1 0 0)



Mode (Data And Command Mode)



Application Circuits



Note: The connection of $\overline{IRQ}$ and $\overline{RD}$ pin can be selected depending on the requirement of the MCU.

The volatage applied to V_{LCD} pin must be equal to or lower than V_{DD}.

Adjust VR to fit LCD display, at V_{DD}=5V, V_{LCD}=4V, VR=15kΩ±20%.

Adjust R (external pull-high resistance) to fit user's time base clock.

Instruction Set Summary

Name	ID	Command Code	D/C	Function	Def.
READ	**1 1 0**	A7A6A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	**1 0 1**	A7A6A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	**1 0 1**	A7A6A5A4A3A2A1A0D0D1D2D3	D	Read and Write data to the RAM	
SYS DIS	**1 0 0**	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	**1 0 0**	0000-0001-X	C	Turn on system oscillator	
LCD OFF	**1 0 0**	0000-0010-X	C	Turn off LCD display	Yes
LCD ON	**1 0 0**	0000-0011-X	C	Turn on LCD display	
TIMER DIS	**1 0 0**	0000-0100-X	C	Disable time base output	Yes
WDT DIS	**1 0 0**	0000-0101-X	C	Disable WDT time-out flag output	Yes
TIMER EN	**1 0 0**	0000-0110-X	C	Enable time base output	
WDT EN	**1 0 0**	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	**1 0 0**	0000-1000-X	C	Turn off tone outputs	Yes
CLR TIMER	**1 0 0**	0000-1101-X	C	Clear the contents of the time base generator	
CLR WDT	**1 0 0**	0000-1111-X	C	Clear the contents of the WDT stage	
RC 32K	**1 0 0**	0001-10XX-X	C	System clock source, on-chip RC oscillator	Yes

Name	ID	Command Code	D/C	Function	Def.
EXT (XTAL) 32K	**1 0 0**	0001-11XX-X	C	System clock source, external 32kHz clock source or crystal oscillator 32.768kHz	
TONE 4K	**1 0 0**	010X-XXXX-X	C	Tone frequency output: 4kHz	
TONE 2K	**1 0 0**	0110-XXXX-X	C	Tone frequency output: 2kHz	
$\overline{\text{IRQ}}$ DIS	**1 0 0**	100X-0XXX-X	C	Disable $\overline{\text{IRQ}}$ output	Yes
$\overline{\text{IRQ}}$ EN	**1 0 0**	100X-1XXX-X	C	Enable $\overline{\text{IRQ}}$ output	
F1	**1 0 0**	101X-0000-X	C	Time base clock output: 1Hz The WDT time-out flag after: 4s	
F2	**1 0 0**	101X-0001-X	C	Time base clock output: 2Hz The WDT time-out flag after: 2s	
F4	**1 0 0**	101X-0010-X	C	Time base clock output: 4Hz The WDT time-out flag after: 1s	
F8	**1 0 0**	101X-0011-X	C	Time base clock output: 8Hz The WDT time-out flag after: 1/2s	
F16	**1 0 0**	101X-0100-X	C	Time base clock output: 16Hz The WDT time-out flag after: 1/4s	
F32	**1 0 0**	101X-0101-X	C	Time base clock output: 32Hz The WDT time-out flag after: 1/8s	
F64	**1 0 0**	101X-0110-X	C	Time base clock output: 64Hz The WDT time-out flag after: 1/16s	
F128	**1 0 0**	101X-0111-X	C	Time base clock output: 128Hz The WDT time-out flag after: 1/32s	Yes
TEST	**1 0 0**	1110-0000-X	C	Test mode, user don't use.	
NORMAL	**1 0 0**	1110-0011-X	C	Normal mode	Yes

Note: X : Don't care

A7~A0 : RAM address

D3~D0 : RAM data

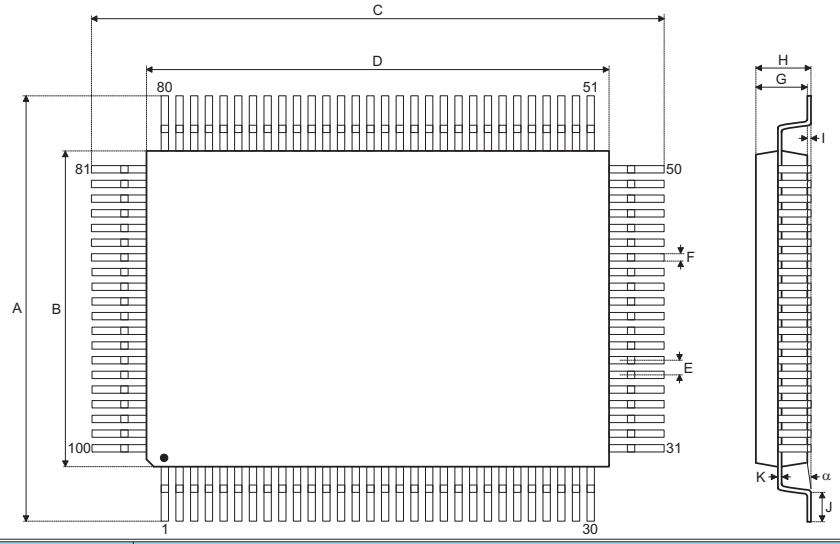
D/C : Data/Command mode

Def. : Power on reset default

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base or WDT clock frequency can be derived from an on-chip 32kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 32kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the HT1626 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the HT1626.

Package Information

100-pin QFP (14mm×20mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.728	—	0.756
B	0.547	—	0.555
C	0.965	—	0.992
D	0.783	—	0.791
E	—	0.026	—
F	—	0.012	—
G	0.098	—	0.122
H	—	—	0.134
I	—	0.004	—
J	0.039	—	0.055
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	18.50	—	19.20
B	13.90	—	14.10
C	24.50	—	25.20
D	19.90	—	20.10
E	—	0.65	—
F	—	0.30	—
G	2.50	—	3.10
H	—	—	3.40
I	—	0.1	—
J	1.00	—	1.40
K	0.10	—	0.20
α	0°	—	7°

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