# HSP50306

July 2004

## Digital QPSK Demodulator

### Features

- **25.6MHz or 26.97MHz Clock Rates**
- **Single Chip QPSK Demodulator with 10kHz Tracking Loop**
- **Square Root of Raised Cosine ($\alpha$ = 0.4) Matched Filtering**
- **2.048 MBPS Reconstructed Output Data Stream**
- **Bit Synchronization with 3kHz Loop Bandwidth**
- **Internal Equalization for Multipath Distortion**
- **6-Bit Real Input: Digitized 10.7MHz or 2.1MHz IF**
- **Level Detection for External IF AGC Loop**
- **0.1s Acquisition Time**
- **$10^{-9}$ BER**
- **<116mA on +5.0V Supply**

### Applications

- **Cable Data Link Receivers**
- **Cable Control Channel Receivers**

### Ordering Information

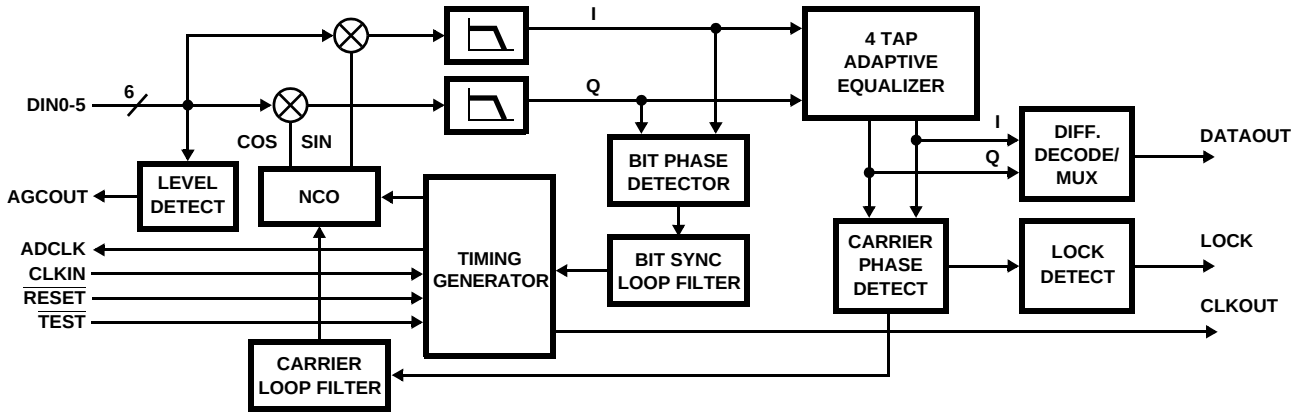
| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|---|---|---|---|
| HSP50306SC-27 | 0 to 70 | 16 Ld SOIC | M16.3 |

### Description

The HSP50306 is a 6-bit QPSK demodulator chip designed for use in high signal to noise environments which have some multipath distortion. The part recovers 2.048 MBPS data from samples of a QPSK modulated 10.7MHz or 2.1MHz carrier. The chip coherently demodulates the waveform, recovers symbol timing, adaptively equalizes the signal to remove multipath distortion, differentially decodes and multiplexes the data decisions. 8-A lock signal is provided to indicate when the tracking loops are locked and the data decisions are valid. To optimize performance, a gain error feedback signal is provided which can be filtered and used to close an I.F. AGC loop around the A/D converter.

The QPSK demodulator derives all timing from CLKIN. The chip divides this clock by 2 to provide the sample clock for the external A/D converter. The -27 version operates at a clock input of 26.97MHz and demodulates a 10.7MHz QPSK signal to recover the 2048 KSPS data. The -25 version operates at a clock input of 25.6MHz and demodulates a 2.1MHz QPSK signal to recover the 2048 KSPS data. Variation from these CLKIN frequencies will progressively degrade the receive data rate, the receive IF, acquisition sweep rate, acquisition sweep range and loop bandwidths as the deviation increases from normal CLKIN. Details on the maximum allowable deviation are found in the Input Characteristics section. The HSP50306 processes 6-bit offset binary data. 4-bit data provides adequate performance for many applications.

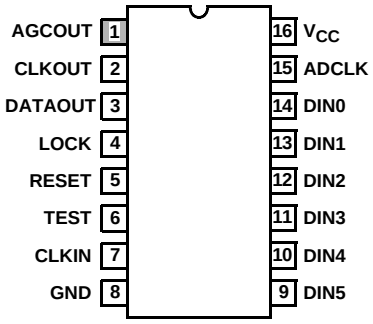
### Block Diagram




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## Pinout

**16 LEAD SOIC**
TOP VIEW




## Pin Description

| NAME | SOIC PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| $V_{CC}$ | 16 | - | +5V Power Supply |
| GND | 8 | - | Ground |
| CLKIN | 7 | I | Clock input. This is the processing clock for the part. All timing is derived from this clock. |
| DIN (5:0) | 9-14 | I | I.F. input samples from the A/D converter. These bits interpreted as offset binary format. DIN5 is the MSB. If fewer than 6 bits are used, the bits from the A/D should be connected to the MSBs of the input and the unused LSBs grounded. |
| ADCLK | 15 | O | This output clock is the clock for the A/D converter. |
| AGCOUT | 1 | O | This output indicates whether the magnitude of the input samples are above or below the expected level. This output is provided as an error detector for an external AGC loop. The output is low when the input is greater than nominal, and high when the input is lower than nominal. |
| DATAOUT | 3 | O | This is the recovered data. |
| CLKOUT | 2 | O | This is the recovered clock. |
| LOCK | 4 | O | This signal indicates that the carrier tracking loop is locked and data on the DOUT pin should be valid. |
| $\overline{\text{RESET}}$ | 5 | I | This input is provided to for initialization and test. Active low. |
| $\overline{\text{TEST}}$ | 6 | I | This input is provided for test. Pull high for normal operation. |

The Block Diagram of the QPSK Demodulator is shown on page 1. To demodulate the data, the I.F. samples are multiplied by sine and cosine samples from a numerically controlled oscillator. The digital mixer outputs are then low pass filtered to remove mixer products. The filtered data is then equalized by a 4 tap equalizer (1 precursor, one reference tap, and a 2 tap Decision Feedback Equalizer (DFE) to remove distortion caused by multipath. The output of the equalizer is differentially decoded and multiplexed into the output data stream. The carrier tracking loop providing the L.O. for the digital mixer is a second order digital Costas loop with a tracking bandwidth of ~10kHz. A sweep circuit searches the carrier uncertainty using a triangle sweep algorithm during acquisition. A lock detector controls the sweep and indicates when valid data is available. The recovered data rate clock is generated by another numerically controlled oscillator. The timing recovery loop is a first order decision directed digital phase locked with a loop bandwidth of ~3kHz. The Level Detect circuitry generates the AGC error signal by rectifying the I.F. input samples and comparing them against a threshold. The error signal is low if the signal magnitude is above the upper threshold, high if the magnitude is below the lower limit.

Figure 1 shows the circuit of a typical demodulator application. The typical Bit Error Rate (BER) performance is shown in Figure 2 for both 4-bit and 6-bit quantized inputs. The theoretical QPSK BER Performance Curve is provided for reference. Note that the BER performance shown in Figure 2 includes a multipath distortion element at the input, in addition to the desired signal. This multipath distortion is representative of receive signal distortions found in cable data links.

Table 1 details the BER, Acquisition and Delay Performance Specifications of the HSP50306 QPSK demodulator chip, based on an input that complies with the specifications detailed in Table 2.

## Application Example

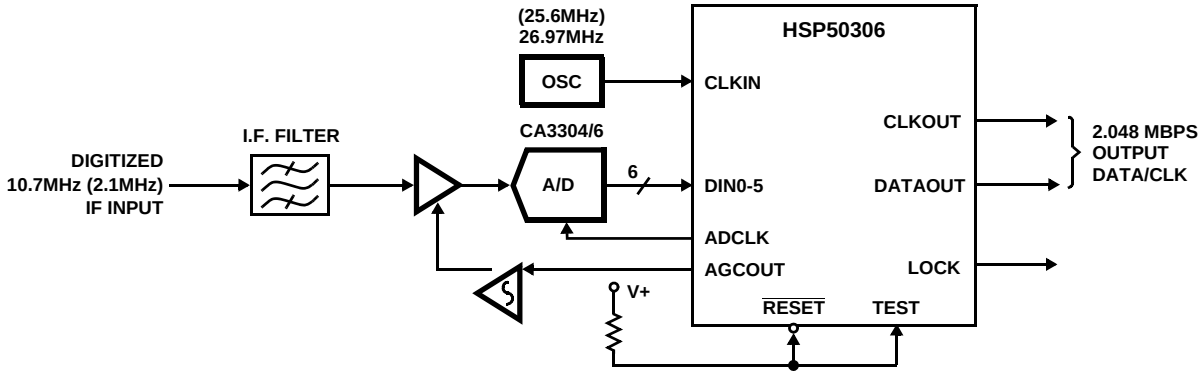
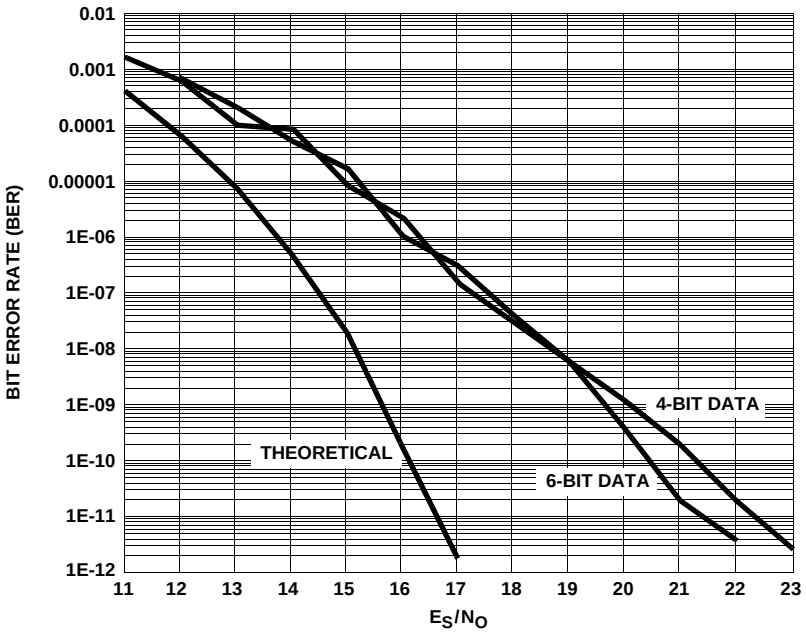



**FIGURE 1. APPLICATIONS CIRCUIT EXAMPLE**




NOTE: Simulation performed using alpha = 0.4 Root Raised Cosine Transmit Filtering, Multipath -10dBc at 72° at 1.6μs.

**FIGURE 2. TYPICAL BIT ERROR RATE PERFORMANCE**

**TABLE 1. PERFORMANCE SPECIFICATIONS**

| SPECIFICATION | PERFORMANCE |
|---|---|
| BER | Better than $1.0 \times 10^{-9}$ with specified input signal characteristics. (See Figure 1.) |
| Acquisition Time | Acquisition within 0.1s from applying an input signal with the specified characteristics. |
| Carrier Loop Bandwidth | 10kHz |
| Bit Sync Loop Bandwidth | 3kHz |
| Throughput Delay | Less than 6 output bit times. |

**TABLE 2. INPUT SIGNAL CHARACTERISTICS** (NOTE 1)

| PARAMETER | SPECIFICATION |
|---|---|
| Carrier Frequency | $10.7 \times 10^6 \pm 40$kHz. |
| Bit Rate | $2.048 \times 10^6 \pm 0.01\%$. |
| Modulation Format | QPSK w/differential encoding specified as:<br>00: 0° phase change 10: +90° phase change<br>01: -90° phase change 11: 180° phase change (Note 2) |
| Filtering | Square root of raised cosine matched filtering ($\alpha = 0.4$). |
| Input RMS Signal Level | Set input p-p signal to full scale on the A/D converter. |
| Input Data Format | 6 bits, offset binary. |
| Input Clock Frequency | 26.97MHz $\pm 0.015\%$ (Note 3) for -27; 25.6MHz $\pm 0.015\%$ for -25. |
| SINAD | >25.5dB SNR (thermal (AWGN)), >28dB (adjacent channel interference). |
| Multipath Distortion | Total energy in multipath distortion -10dBc<br>>95% of multipath energy within 2μs from main path. If the multipath changes rapidly, the bit error rate may exceed the above specification until the equalizer has readjusted. |

NOTES:

1. All frequencies are relative to the input clock frequency. For example, the bit rate is actually ~0.075936 * $f_{CLK}$. The frequencies provided in this document are only valid for a 26.97MHz or 25.6MHz clock.
2. Each pair of input bits is encoded into a phase change relative to the previous symbol. In the HSP50306, the symbol to symbol phase change is decoded into the transmitted bit pair which is multiplexed into the output data stream.
3. While the device is static CMOS and can be clocked down to close to DC, the specified range indicates the accuracy needed to maintain the data rate inside the bit sync tracking loop bandwidth assuming 50ppm tx and 100ppm rx crystal accuracies.

## Two Versions: Different Applications

The -27 and -25 versions of the HSP50306 Digital QPSK Demodulator are not simply different speed grades of the same device, but are designs which have proportionally scaled clocks and bandwidths for different applications. ***NOTE: While these parts are pin for pin compatible, in most applications they cannot be used as functional equivalent substitutes for each other.*** Key differences are:

- The -27 version of the HSP50306 has an input IF of 10.7MHz with an input clock of 26. 97MHz.
- The -25 version of the HSP50306 has an input IF of 2.1MHz with an input clock of 25. 6MHz.

In both the -27 and -25 designs, the sample rate clock for the input IF signal is half of the CLK frequency. ***NOTE: Sample rate clock is designated by $f_S = f_{CLK}/2$.*** Aside from input IF and input clock, all other performance parameters of the two parts are identical for their respective IF inputs.

## 10.7MHz Input IF Applications

Both the -27 and -25 parts can be used in 10.7MHz IF Applications. Figures 3 and 4 show the frequency spectrum for the sampled 10.7MHz IF input signals for both the -27 and -25 versions, respectively. In the 10.7MHz IF Application, the -25 version offers tighter filtering capability than the -27 version because the lower IF allows use of low pass filtering. Also, the lower IF of the -25 version has inherently lower internal processing spectral spurs than the -27 version. Note that the receive IF for the HSP50306SC-27 is the input IF to the demodulator. For the HSP50306SC-25, the receive IF is 10.7MHz, but the processing is done on the spectral image at 2.1MHz. Examine the spectral inversion between the 10.7MHz Receive IF and the 2.1MHz demodulator input in Figure 4. **The transmit differential encoder must take into account this spectral reversal.** The required encoding is shown in Table 3. This part was designed to be paired with the HSP50307 Burst Modulator, and can be operated from the same 25.6MHz reference clock.

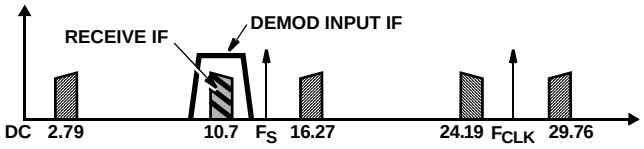



**FIGURE 3. SAMPLED SPECTRUM FOR THE -27 VERSIONS ($f_{CLK}$ = 26.97MHz)**

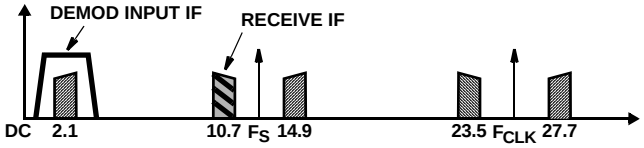



**FIGURE 4. SAMPLED SPECTRUM FOR THE -25 VERSIONS ($f_{CLK}$ = 25.6MHz)**

**TABLE 3. DIFFERENTIAL ENCODING REQUIRED FOR THE -27 AND -25 DEMODULATORS RECEIVING 10.7MHz IF**

| INPUT BITS | PHASE CHANGE REQUIRED FOR -27 DEMODULATION | PHASE CHANGE REQUIRED FOR -25 DEMODULATION |
|---|---|---|
| 00 | $0^o$ | $0^o$ |
| 01 | $-90^o$ | $90^o$ |
| 10 | $90^o$ | $-90^o$ |
| 11 | $180^o$ | $180^o$ |

## Absolute Maximum Ratings $T_A = 25°C$

Supply Voltage . . . . . +6.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to $V_{CC}$ +0.5V
Typical Derating Factor . . . . . 4mA/MHz Increase in $I_{CCOP}$
ESD Classification . . . . . Class 1

## Operating Conditions

Operating Voltage Range . . . . . 4.75V to 5.25V
Operating Temperature Range. . . . . 0°C to 70°C

## Thermal Information

Thermal Resistance (Typical, Note 4) $\theta_{JA}$ (°C/W)
SOIC Package. . . . . 100
Maximum Junction Temperature. . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s). . . . . 300°C
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

4. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

## DC Electrical Specifications $V_{CC} = 5.0V \pm 5\%$, $T_A = 0°C$ to $70°C$

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| Power Supply Current | $I_{CCOP}$ | $V_{CC}$ = Max, CLK = 28.6MHz (Notes 5, 6) | - | 114 | mA |
| Standby Power Supply Current | $I_{CCSB}$ | $V_{CC}$ = Max, Outputs Not Loaded | - | 500 | µA |
| Input Leakage Current | $I_I$ | $V_{CC}$ = Max, Input = 0V or $V_{CC}$ | -10 | 10 | µA |
| CMOS Output High (ADCLK, AGCOUT) | $V_{OHC}$ | $V_{CC}$ = Min, $I_{OH}$ = -400µA | 3.7 | - | V |
| CMOS Output Low (ADCLK, AGCOUT) | $V_{OLC}$ | $V_{CC}$ = Min, $I_{OL}$ = 2mA | - | 0.4 | V |
| Logical One Input Voltage | $V_{IH}$ | $V_{CC}$ = Max | 2.0 | - | V |
| Logical Zero Input Voltage | $V_{IL}$ | $V_{CC}$ = Min | - | 0.8 | V |
| Logical One Output Voltage | $V_{OH}$ | $I_{OH}$ = -400µA, $V_{CC}$ = Min | 2.4 | - | V |
| Logical Zero Output Voltage | $V_{OL}$ | $I_{OL}$ = 2mA, $V_{CC}$ = Min | - | 0.4 | V |
| Input Capacitance | $C_{IN}$ | CLK = 1MHz<br>All measurements referenced to GND.<br>$T_A$ = 25°C, (Note 7) | - | 10 | pF |
| Output Capacitance | $C_{OUT}$ | | - | 10 | pF |

NOTES:

5. Power supply current is proportional to frequency. Typical rating is 4mA/MHz.
6. Output load per test circuit and $C_L$ = 40pF.
7. Not tested, but characterized at initial design and at major process/design changes.

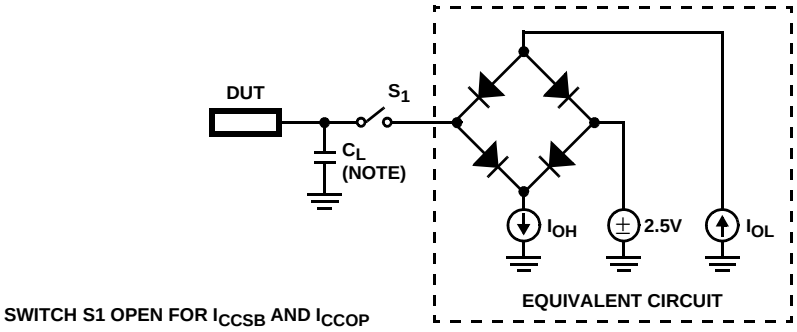
**AC Electrical Specifications** 27MHz Clock Rate, $V_{CC}$ = 5.0V ±5%, $T_A$ = 0°C to 70°C (Note 8)

| PARAMETER | SYMBOL | NOTES | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| CLK Period | $t_{CP}$ | | 36 | - | ns |
| CLK High | $t_{CH}$ | | 12 | - | ns |
| CLK Low | $t_{CL}$ | | 12 | - | ns |
| Setup RESET to CLK | $t_{RS}$ | | 15 | - | ns |
| Hold Time RESET to CLK | $t_{RH}$ | | 1 | - | ns |
| Setup Time DIN0-5 to ADCLK | $t_{DS}$ | 9 | 15 | - | ns |
| Hold Time DIN0-5 to ADCLK | $t_{DH}$ | 9 | 2 | - | ns |
| CLK to DATAOUT, LOCK, AGCOUT | $t_{PD}$ | | - | 25 | ns |
| Output Rise, Fall Time | $t_{RF}$ | 10 | - | 8 | ns |
| Output Rise, Fall Time (CMOS Outputs) | $t_{TC}$ | 10 | - | 12 | ns |

NOTES:

8. AC Testing is performed as follows: Input levels 0.0V to 3.0V. Timing reference levels = 1.5V. Output load circuit with $C_L$ = 40pF. Output transition measured at $V_{OH}$_1.5V and $V_{OL}$_1.5V.
9. The set up and hold times for DIN (5:0) are with respect to the rising edge of ADCLKOUT. These parameters are guaranteed by design and characterization but not tested. An A/D converter with a clock to data out specification of 55ns and a data hold from clock specification of 2ns will meet these requirements at an oscillator clock frequency of 26.97MHz. Intersil recommends the CA3304 or CA3306 A/D converters for use with the HSP50306.
10. Controlled via design or process parameters and not directly tested. Characterized upon initial design and at major process or design changes.

## *AC Test Load Circuit*




NOTE: Test head capacitance

## Waveforms

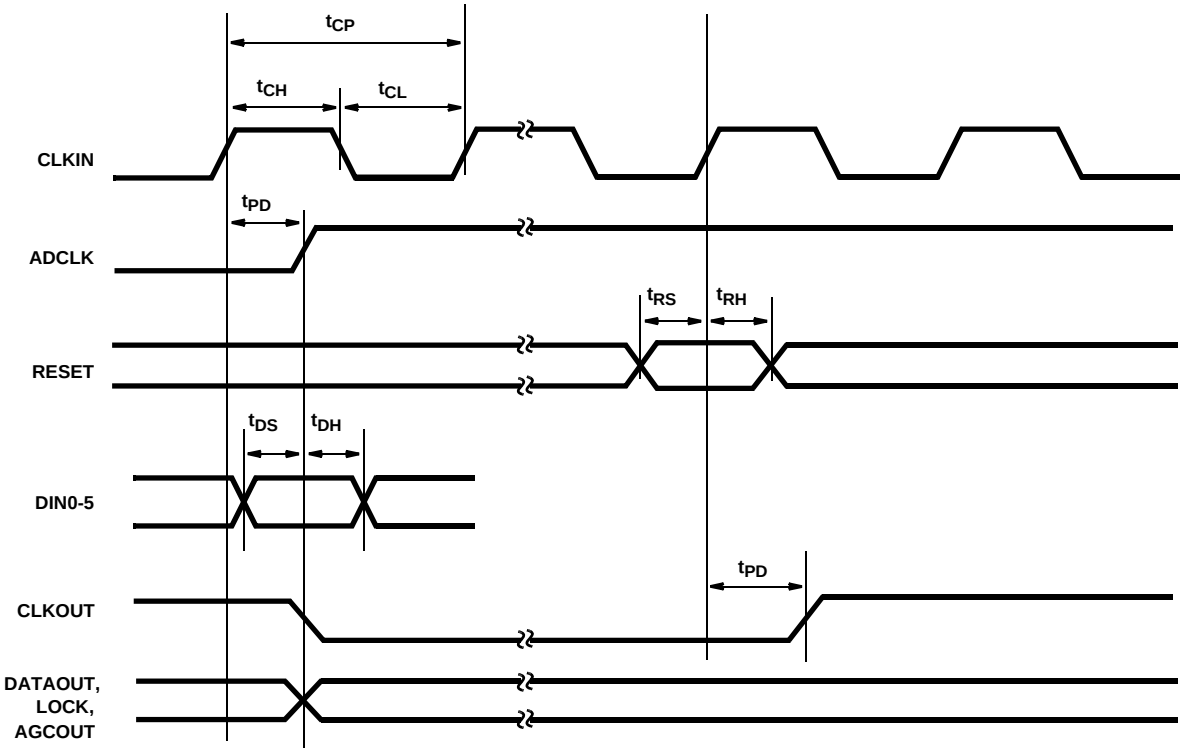



FIGURE 5.

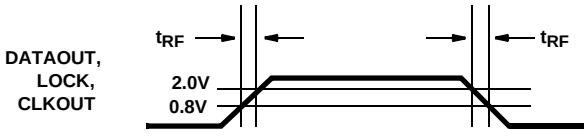



FIGURE 6. OUTPUT RISE AND FALL TIMES

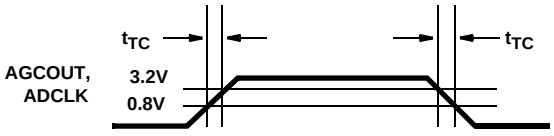



FIGURE 7. OUTPUT RISE AND FALL TIMES

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