HSMP-386J
High Power RF PIN Diode

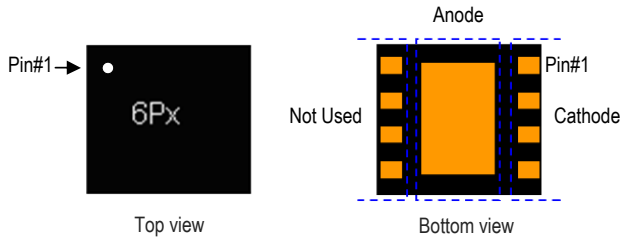
Data Sheet

Description

Avago Technologies' HSMP-386J is a High Power RF PIN Diode specifically design for high power handling and low distortion Transmit/Receive switching application. It is housed in QFN 2x2mm size package which is having good thermal resistance.

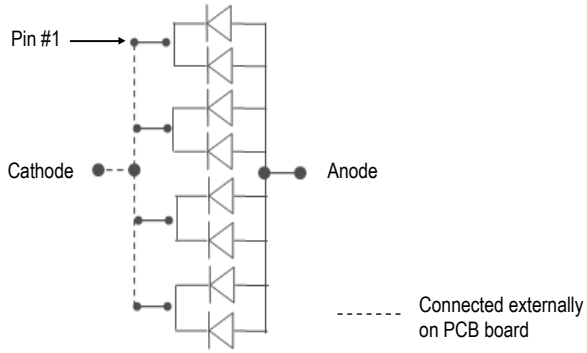
The unique with 8 dies in parallel configuration results to low IL performance and low series resistance. The HSMP-386J Power diode is built with match diode to ensure consistency in performance.

Package Marking & Orientation



Notes:
6P = Device Code
x = Month code indicates the month of manufacture

Circuit Diagram of HSMP-386J



Features

- High Power Surface Mount Package QFN 2x2
- Match Diode for Consistent Performance
- Low Bias Current Requirement
- Low Series Resistance
- Low Insertion Loss & High Isolation
- Better Thermal Conductivity for Higher Power Dissipation
- Low Failure in Time (FIT) Rate
- Lead-free Option Available
- MSL1 & Lead Free
- Tape & Reel Option Available

Specifications

- Low RS Switching typically 0.65Ω @ 100MHz., 50mA
- High Power Handling Up to 10W (40dBm) at 2GHz, 50mA

Application

- High Power Transmit / Receive Switch for Cellular Infrastructure and Two Way Radio

Table 1. Absolute Maximum Ratings [1] at T_C = +25°C

Symbol	Parameter	Unit	Max Rating
I_F	Forward Current (1µs Pulse) per die [2]	Amp	1
P_{IV}	Peak Inverse Voltage	V	100
T_j	Junction Temperature	°C	150
T_{stg}	Storage Temperature	°C	-60 to 150
θ_{jc}	Thermal Resistance [3]	°C/W	45
DC P_{diss}	DC Power Dissipation [4]	W	2.0

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. Eight dice are connected in parallel for this device.
3. TC = +25°C, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.
4. Maximum DC P_{diss} measured without RF input and maximum rating is base on device junction temperature.

$$P_{diss} = \frac{T\,(\text{Max.Operating}) - 25\,^{\circ}\text{C}}{\text{Thermal Resistance}}$$

Table 2. Electrical Performance at T_C = +25°C

	Minimum Breakdown Voltage V_{BR} (V)	Typical Forward Voltage V_f (V)	Maximum Series Resistance R_S (Ohm)	Maximum Total Capacitance C_T (pF)
	100	0.85	0.77	1.25
Test Conditions	$V_R = V_{BR}$ Measure $I_R \leq$ 5uA	I_F = 50mA	I_F = 50 mA f = 100 MHz	V_R = 50V f = 1MHz

Table 3. Typical Performance at T_C = +25°C

	Series Resistance R_S (Ω)	Carrier Lifetime (nS)	Reverse Recovery Time T_{rr} (nS)	Total Capacitance C_T (pF)
	0.65	260	130	0.75
Test Conditions	I_F = 50mA f = 100MHz	I_F = 50mA I_R = 100mA	V_R = 5V I_F = 50mA 90% Recovery	V_R = 50V f = 1MHz

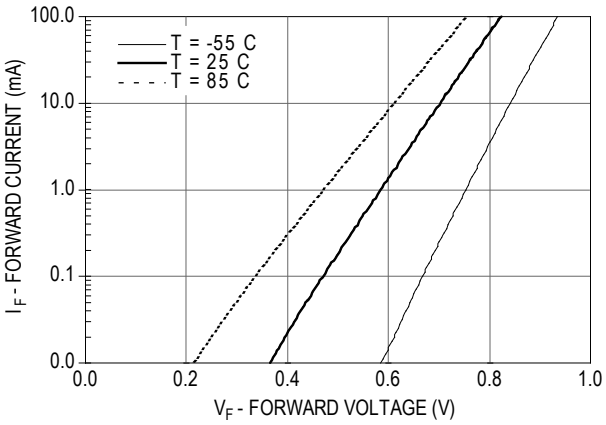


Figure 1. Forward Current vs. Forward Voltage

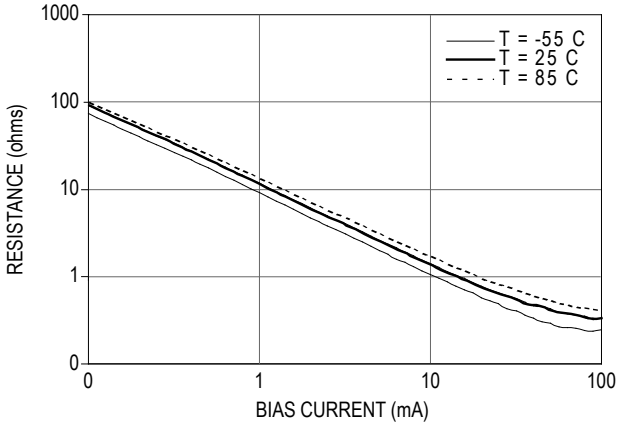


Figure 2. Typical RF Resistance vs. Forward Bias Current.

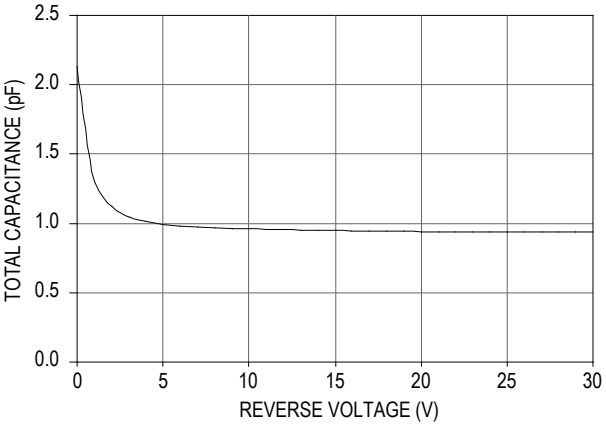


Figure 3. RF Capacitance vs. Reverse Bias Voltage

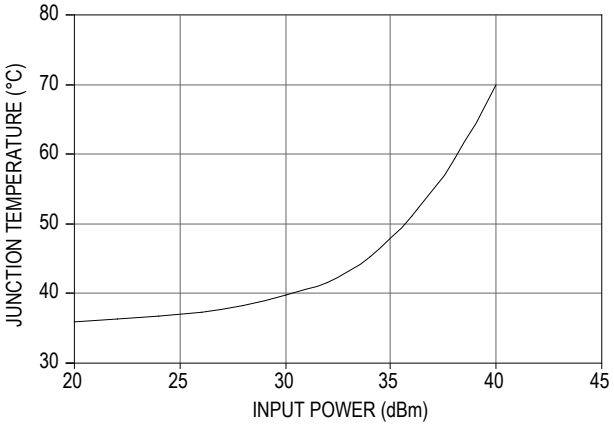
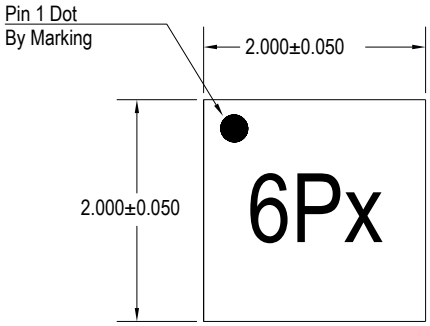


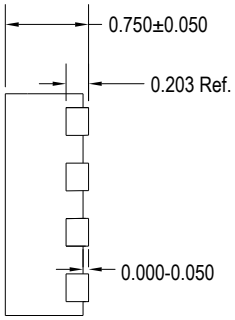
Figure 4. Input Power vs. Junction Temperature [1]

Notes:
1. Test conditions: f = 2.1GHz, I_F = 50mA
2. Typical values were derived using limited samples during initial product characterization and may not be representative of the overall distribution.

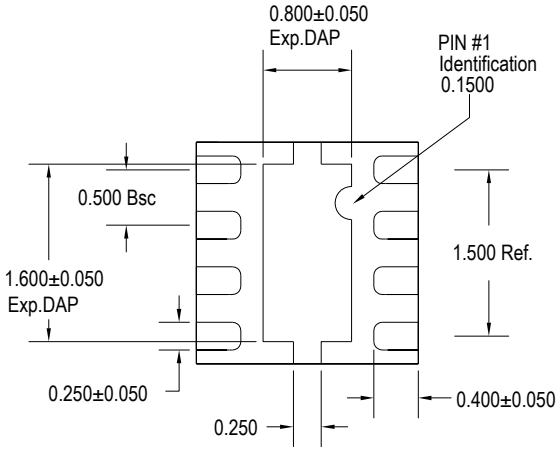
QFN 2x2 Package Dimension



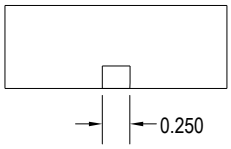
Top View



Side View



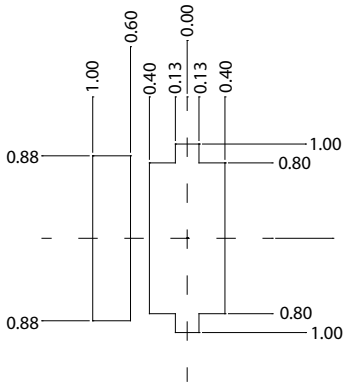
Bottom View



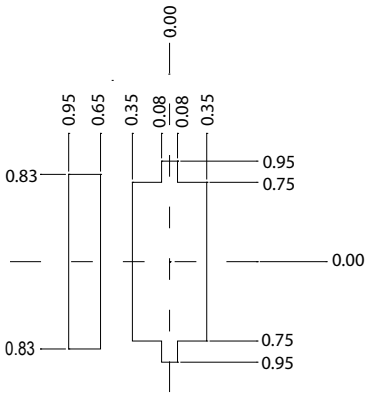
Top View

Note:
1. All dimensions in millimeters.
2. Dimensions are inclusive of plating.
3. Dimensions are exclusive of mold flash and metal burr.

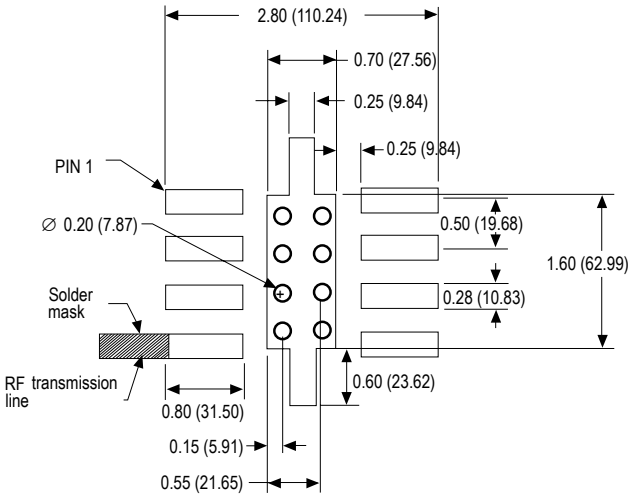
PCB Land Pattern and Stencil Design



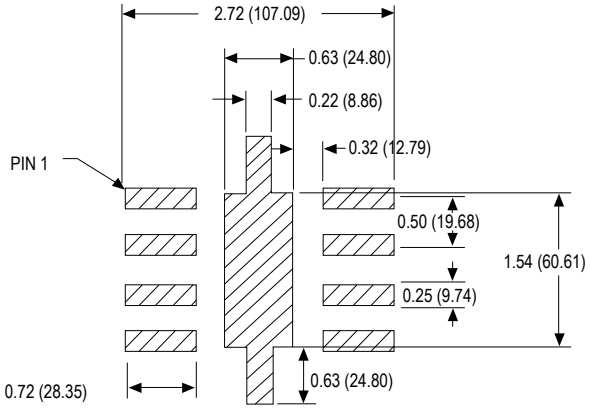
PCB Land Pattern A (top view)



Stencil Layout A (top view)



PCB Land Pattern B (top view)



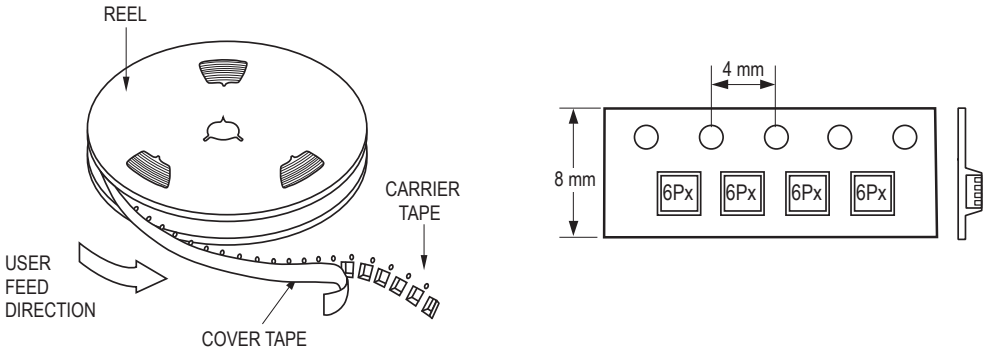
Stencil Layout B (top view)

Note :
1. All dimensions in millimeters (mils).
2. For PCB land pattern B and stencil layout B, external trace is required to connect all cathode pads as one single pad.

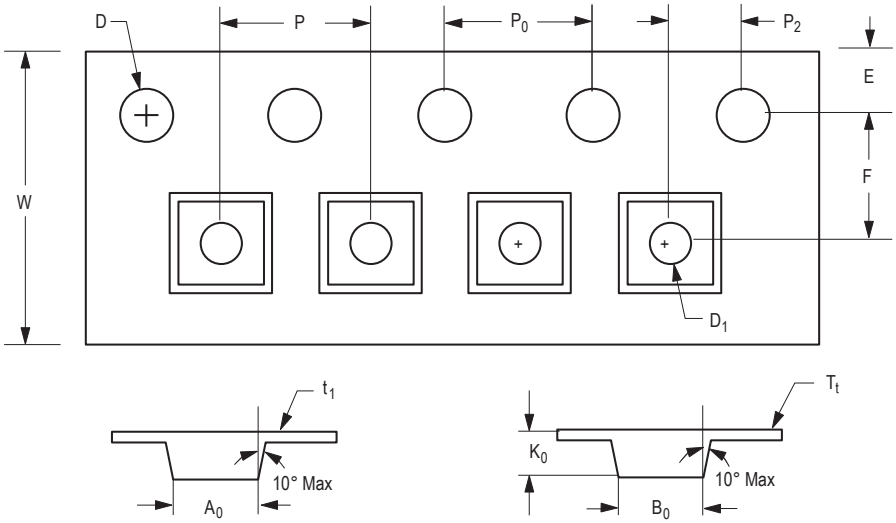
Ordering Information

Part Number	No. of Devices	Container
HSMP-386J-TR1G	3000	7″ Reel
HSMP-386J-TR2G	10000	13″ Reel
HSMP-386J-BLKG	100	antistatic bag

Device Orientation



Tape Dimensions



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (inches)
CAVITY	LENGTH	A_0	2.30 ± 0.05	0.091 ± 0.004
	WIDTH	B_0	2.30 ± 0.05	0.091 ± 0.004
	DEPTH	K_0	1.00 ± 0.05	0.039 ± 0.002
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.002
PERFORATION	DIAMETER	D	1.50 ± 0.10	0.060 ± 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 + 0.30 8.00 ± 0.10	0.315 ± 0.012 0.315 ± 0.004
	THICKNESS	t_1	0.254 ± 0.02	0.010 ± 0.0008
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.0004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

Avago, Avago Technologies, and the A logo are trademarks of Avago Technologies, Limited in the United States and other countries.
Data subject to change. Copyright © 2007 Avago Technologies Limited. All rights reserved.
AV02-0819EN - December 25, 2007