Radiation Hardened CMOS Dual DPST Analog Switch

HS-302RH, HS-302EH

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD Total Dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

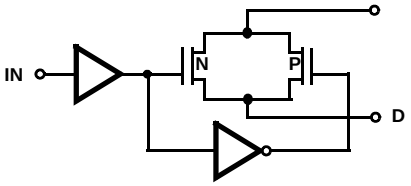
The HS-302RH, HS-302EH analog switch is a monolithic device fabricated using Radiation Hardened CMOS technology and the Intersil dielectric isolation process for latch-up free operation. Improved total dose hardness is obtained by layout (thin oxide tabs extending to a channel stop) and processing (hardened gate oxide). These switches offer low-resistance switching performance for analog voltages up to the supply rails. "ON" resistance is low and stays reasonably constant over the full range of operating voltage and current. "ON" resistance also stays reasonably constant when exposed to radiation, being typically 30Ω pre-rad and 35Ω post 100kRAD(Si). This device provide break-before-make switching.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the HS-302RH, HS-302EH are contained in SMD# 5962-95812.

Functional Diagram



TRUTH TABLE

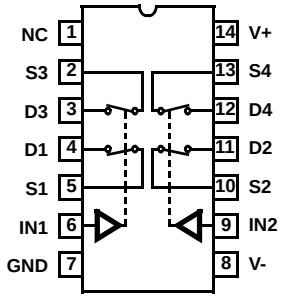
LOGIC	ALL SWITCHES
0	OFF
1	ON

Features

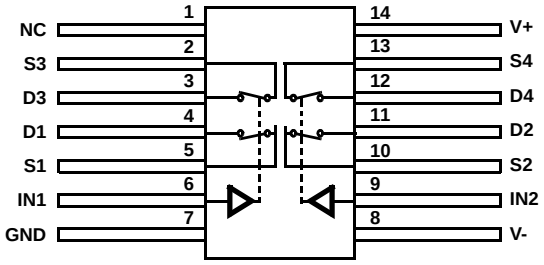
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose (γ) 1 x 10^5 RAD(Si)
- No Latch-Up, Dielectrically Isolated Device Islands
- Pin for Pin Compatible with Intersil HI-302 Series Analog Switches
- Analog Signal Range 15V
- Low Leakage. . . . . .100nA (Max, Post Rad)
- Low R_{ON} . . . . . .60Ω (Max, Post Rad)
- Low Operating Power. . . . . .100µA (Max, Post Rad)

Pin Configurations

HS1-302RH, HS1-302EH
(SBDIP), CDIP2-T14
TOP VIEW



HS9-302RH, HS9-302EH
(FLATPACK), CDFP3-F14
TOP VIEW



Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
5962R9581201V9A	HS0-302RH-Q	-55 to +125	Die	N/A
5962R9581202V9A	HS0-302EH-Q	-55 to +125	Die	N/A
5962R9581201QCC	HS1-302RH-8	-55 to +125	14 Ld SBDIP	D14.3
5962R9581201VCC	HS1-302RH-Q	-55 to +125	14 Ld SBDIP	D14.3
5962R9581202VCC	HS1-302EH-Q	-55 to +125	14 Ld SBDIP	D14.3
5962R9581201QXC	HS9-302RH-8	-55 to +125	Flatpack	K14.A
5962R9581201VXC	HS9-302RH-Q	-55 to +125	Flatpack	K14.A
5962R9581202VXC	HS9-302EH-Q	-55 to +125	Flatpack	K14.A
HS9-302RH/PROTO	HS9-302RH/PROTO	-55 to +125	Flatpack	K14.A

NOTE: These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Die Characteristics

DIE DIMENSIONS:

(2130µm x 1930µm x 533µm ±25.4µm)

84 x 76 x 21mils ±1mil

METALLIZATION:

Type: Al

Thickness: 12.5kÅ ±2kÅ

SUBSTRATE POTENTIAL:

Unbiased (DI)

BACKSIDE FINISH:

Silicon

PASSIVATION:

Type: Silox (S_iO_2)

Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm^2

TRANSISTOR COUNT:

76

PROCESS:

Metal Gate CMOS, Dielectric Isolation

Metallization Mask Layout

HS-302RH, HS-302EH