Data Sheet | March 24, 2006 | FN4874.1

Radiation Hardened High Speed, Quad SPST, CMOS Analog Switch

The HS-201HSRH is a monolithic CMOS analog switch featuring power-off high input impedance, very fast switching speeds and low ON resistance. Fabrication on our DI RSG process assures SEL immunity and only very slight sensitivity to low dose rate (ELDRS). These Class V/Q devices are tested and guaranteed for 300krad (Si) total dose performance.

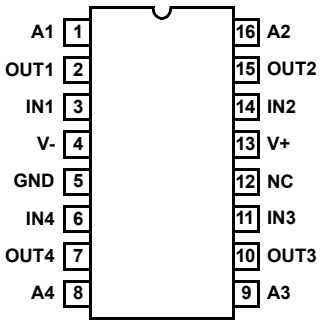
Power-off high input impedance enables the use of this device in redundant circuits without causing data bus signal degradation. ESD protection, overvoltage protection, fast switching times, low ON resistance, and guaranteed radiation hardness, make the HS-201HSRH ideal for any space application where improved switching performance is required.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center (DSCC). The SMD numbers listed here must be used when ordering flight units.

Detailed electrical specifications for this device are contained in SMD 5962-99618. A "hot-link" is provided on our homepage for downloading.
www.intersil.com/spacedefense/space.asp

Pinout

HS1-201HSRH, SBDIP (CDIP2-T16)
HS9-201HSRH, FLATPACK (CDFP4-F16)
TOP VIEW



Features

- Electrically Screened to DSCC SMD 5962-99618
- QML Qualified per MIL-PRF-38535
- Radiation Performance
  - Guaranteed Total Dose Performance . . . . . 300krad (Si)
  - SEL Immune . . . . . .DI RSG Process
- Overvoltage Protection (Power On, Switch Off) . . . . . $\pm$30V
- Power Off High Impedance . . . . . $\pm$17V
- Fast Switching Times
  - t_{ON} . . . . . 110ns (Max)
  - t_{OFF} . . . . . 80ns (Max)
- Low "ON" Resistance . . . . . 50Ω (Max)
- Pin Compatible with Industry Standard 201 Types
- Operating Supply Range . . . . . $\pm$10V to $\pm$15V
- Wide Analog Voltage Range ($\pm$15V Supplies) . . . . . $\pm$15V
- TTL Compatible

Applications

- High Speed Multiplexing
- Sample and Hold Circuits
- Digital Filters
- Operational Amplifier Gain Switching Networks
- Integrator Reset Circuits

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
5962F9961801VEC	HS1-201HSRH-Q	Q 5962F9961801VEC	-55 to 125	16 Ld SBDIP	D16.3
5962F9961801QEC	HS1-201HSRH-8	Q 5962F9961801QEC	-55 to 125	16 Ld SBDIP	D16.3
5962F9961801VXC	HS9-201HSRH-Q	Q 5962F9961801VXC	-55 to 125	16 Ld Flatpack	K16.A
5962F9961801QXC	HS9-201HSRH-8	Q 5962F9961801QXC	-55 to 125	16 Ld Flatpack	K16.A
5962F9961801V9A	HS0-201HSRH-Q	-	-55 to 125	-	-
HS1-201HSRH/PROTO	HS1-201HSRH/PROTO	HS1-201HSRH/PROTO	-55 to 125	16 Ld SBDIP	D16.3
HS9-201HSRH/PROTO	HS9-201HSRH/PROTO	HS9-201HSRH/PROTO	-55 to 125	16 Ld Flatpack	K16.A

Die Characteristics

DIE DIMENSIONS

2790μm x 4950μm (110 mils x 195 mils)
Thickness: 483μm ±25.4μm (19 mils ±1 mil)

INTERFACE MATERIALS

Glassivation

Type: Phosphorus Silicon Glass (PSG)
Thickness: 8.0kÅ +/-1.0kÅ

Metallization

Type: Ti/AlCu
Thickness: 16.0kÅ +/- 2kÅ

Substrate

Rad Hard Silicon Gate, Dielectric Isolation

Backside Finish

Silicon

ASSEMBLY RELATED INFORMATION

Substrate Potential

Unbiased (DI)

ADDITIONAL INFORMATION

Worst Case Current Density

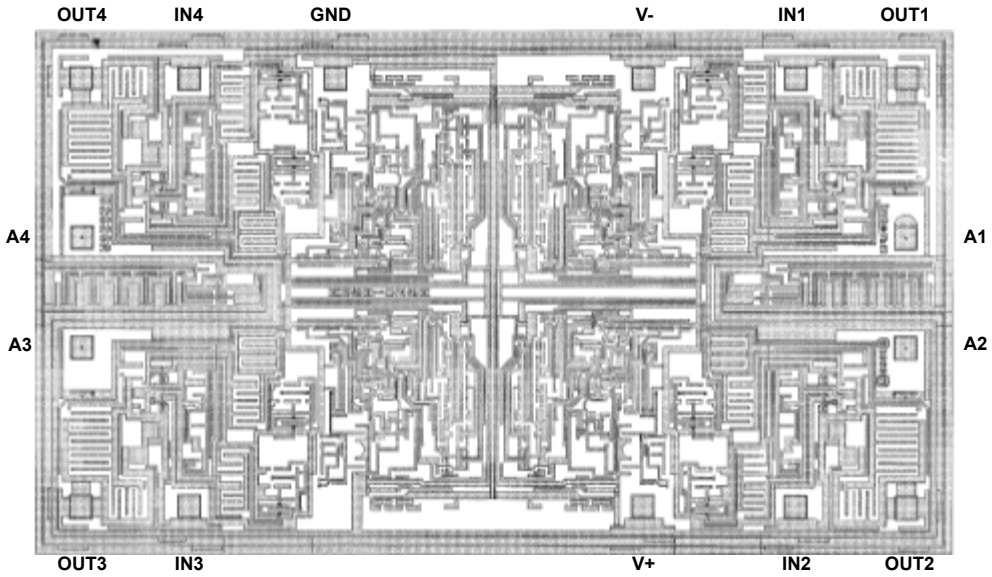
$<2.0 \times 10^5$ A/cm^2

Transistor Count

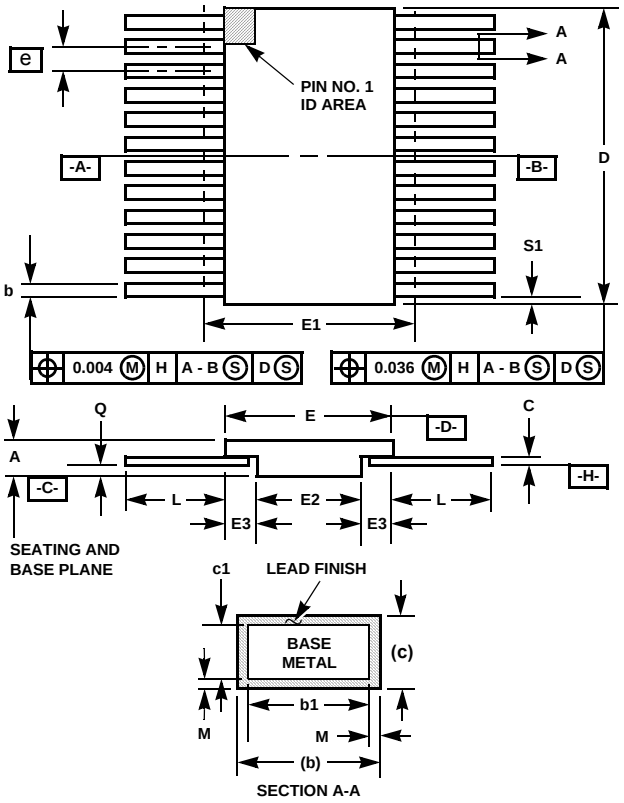
328

Metallization Mask Layout

HS-201HSRH



Ceramic Metal Seal Flatpack Packages (Flatpack)



K16.A MIL-STD-1835 CDFP4-F16 (F-5A, CONFIGURATION B)
16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.440	-	11.18	3
E	0.245	0.285	6.22	7.24	-
E1	-	0.315	-	8.00	3
E2	0.130	-	3.30	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	16		16		-

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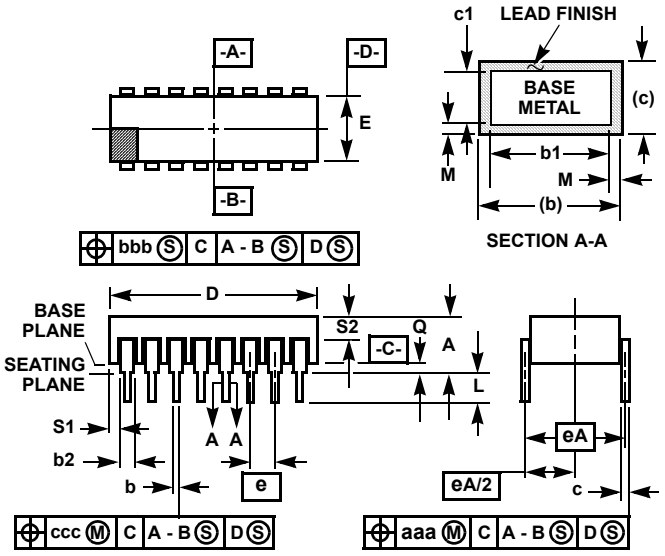
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

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