intersil

HS-0506RH, HS-0507RH

NOT RECOMMENDED FOR NEW DESIGNS
See HS-0546RH, HS-0547RH
contact our Technical Service Center at
1-888-INTERSIL or www.intersil.com/tsc

Radiation Hardened Single 16/Differential 8 Channel CMOS Analog Multiplexer

September 1997

Features

- **Low On Resistance 400Ω Max**
- **Wide Analog Signal Range ±15V**
- **TTL/CMOS Compatible 2.4V (Logic "1")**
- **Access Time 1000ns Max**
- **44V Maximum Power Supply**
- **Break-Before-Make Switching**
- **No Latch-up**
- **Gamma Dose 1 x 10^4 RAD (Si)**

Applications

- **Data Acquisition Systems**
- **Precision Instrumentation**
- **Demultiplexing**
- **Selector Switch**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HS1-0506RH-Q	-55°C to 125°C	28 Lead CerDIP
HS1-0507RH-Q	-55°C to 125°C	28 Lead CerDIP

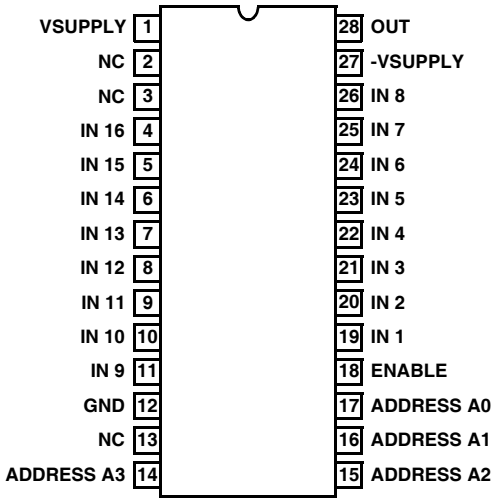
Description

These radiation hardened monolithic CMOS multiplexers each include an array of sixteen analog switches, a digital decode circuit for channel selection, voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

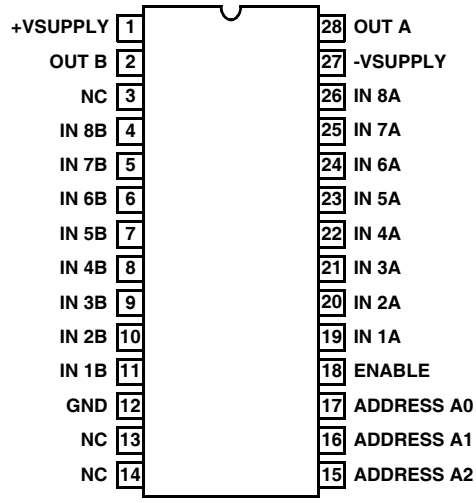
The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latchup. Also, DI offers much lower substate leakage and parasitic capacitance than conventional junction isolated CMOS. The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for logic "1" and maximum 0.8V for logic "0". This allows direct interface without pullup resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and diode clamp to each supply. The HS-0506RH is a sixteen channel single-ended multiplexer, and the HS-0507RH is an eight channel differential version. If input overvoltage protection is needed, the HS-0506RH or HS-0507RH multiplexers are recommended. For further information see Application Notes 520 and 521.

Pinouts

HS-0506RH 28 LEAD CERAMIC DUAL-IN-LINE
FRIT SEAL PACKAGE (CerDIP)
MIL-STD-1835 GDIP1-T28
TOP VIEW



HS-0507RH 28 LEAD CERAMIC DUAL-IN-LINE
FRIT SEAL PACKAGE (CerDIP)
MIL-STD-1835 GDIP1-T28
TOP VIEW

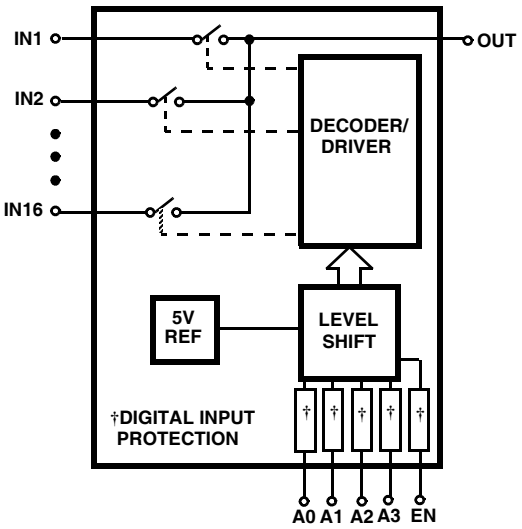


CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 321-724-7143 | Intersil (and design) is a registered trademark of Intersil Americas Inc.
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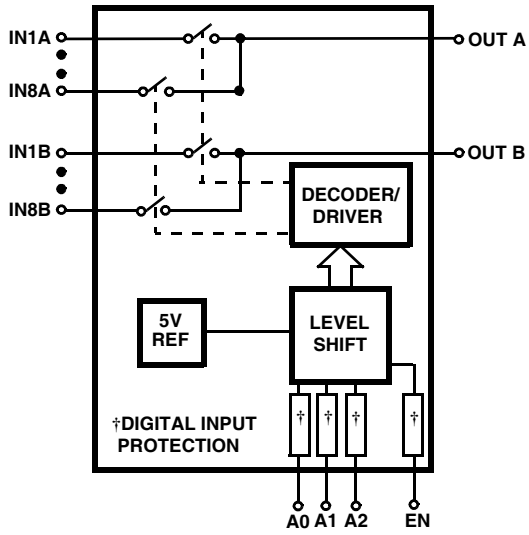
Spec Number **518860**
File Number **4028.1**

Functional Diagrams

HS-0506RH



HS-0507RH



HS-0506RH TRUTH TABLE

A3	A2	A1	A0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HS-0507RH TRUTH TABLE

A2	A1	A0	EN	"ON" CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

Absolute Maximum Ratings

Voltage Between Supply Pins . . . . . +44V
+VSUPPLY to Ground . . . . . +22V
-VSUPPLY to Ground. . . . . -25V
Analog Input Overvoltage:
+VS. . . . . +VSUPPLY +2V
-VS . . . . . -VSUPPLY -2V
Digital Input Overvoltage:
+VEN, +VA . . . . . +VSUPPLY +4V
-VEN, -VA . . . . . -VSUPPLY -4V
or 20mA, Whichever Occurs First
Continuous Current, S or D 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% Duty Cycle Maximum 40mA
Storage Temperature Range . . . . . -65^oC to $+150^oC$
Lead Temperature (Soldering 10s). . . . . $+275^oC$

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
CerDIP Package	$51^oC/W$	$18^oC/W$

Maximum Package Power Dissipation at $+125^oC$
CerDIP Package 0.98W
If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:
CerDIP Package . . . . . $19.6mW/^oC$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range. . . . . -55^oC to $+125^oC$
Operating Supply Voltage (±VSUPPLY). . . . . ±15V
Analog Input Voltage (VS) . . . . . VSUPPLY
Logic Low Level (VAL) . . . . . 0V to 0.8V
Logic High Level (VAH). . . . . +4V to +VSUPPLY
Max RMS Current, S or D 8mA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device tested at +VSUPPLY = +15V. -VSUPPLY = -15V, VEN = 2.4V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS		GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	IIH	Measure Inputs Sequentially GND All Unused Inputs		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-1.0	1.0	µA
	IIL			1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-1.0	1.0	µA
Leakage Current into the Source Terminal of an "OFF" Switch	+IS(OFF)	VS = +10V, VD = -10V, VEN = 0.8V, All Unused Inputs = -10V		1	$+25^oC$	-10	+10	nA
				2, 3	$+125^oC$, -55^oC	-50	+50	nA
	-IS(OFF)	VS = -10V, VD = +10V, VEN = 0.8V All Unused Inputs = +10V		1	$+25^oC$	-10	+10	nA
				2, 3	$+125^oC$, -55^oC	-50	+50	nA
Leakage Current into the Drain Terminal of an "OFF" Switch	+ID(OFF)	VD = +10V, VEN = 0.8V All Unused Inputs = -10V	HS-0506RH HS-0507RH	1	$+25^oC$	-10	+10	nA
			HS-0506RH	2, 3	$+125^oC$, -55^oC	-300	+300	nA
			HS-0507RH	2, 3	$+125^oC$, -55^oC	-200	+200	nA
	-ID(OFF)	VD = -10V, VEN = 0.8V All Unused Inputs = +10V	HS-0506RH HS-0507RH	1	$+25^oC$	-10	+10	nA
			HS-0506RH	2, 3	$+125^oC$, -55^oC	-300	+300	nA
			HS-0507RH	2, 3	$+125^oC$, -55^oC	-200	+200	nA
Leakage Current F from an "ON" Driver into the Switch (Drain)	+ID(ON)	VS = VD = +10V All Unused Inputs = 10V	HS-0506RH HS-0507RH	1	$+25^oC$	-10	+10	nA
			HS-0506RH	2, 3	$+125^oC$, -55^oC	-300	+300	nA
			HS-0507RH	2, 3	$+125^oC$, -55^oC	-200	+200	nA
	-ID(ON)	VS = VD = -10V All Unused Inputs = +10V	HS-0506RH HS-0507RH	1	$+25^oC$	-10	+10	nA
			HS-0506RH	2, 3	$+125^oC$, -55^oC	-300	+300	nA
			HS-0507RH	2, 3	$+125^oC$, -55^oC	-200	+200	nA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device tested at +VSUPPLY = +15V. -VSUPPLY = -15V, VEN = 2.4V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Positive Supply Current	I(+)	VA = 0V, VEN = 2.4V	1, 2, 3	+25°C, +125°C, -55°C	-	3.0	mA
Negative Supply Current	I(-)	VA = 0V, VEN = 2.4V	1, 2, 3	+25°C, +125°C, -55°C	-1.0	-	mA
Standby Positive Supply Current	+ISBY	VA = 0V, VEN = 0V	1, 2, 3	+25°C,+ 125°C, -55°C	-	3.0	mA
Standby Negative Supply Current	-ISBY	VA = 0V, VEN = 0V	1, 2, 3	+25°C,+125°C, -55°C	-1.0	-	mA
Switch "ON" Resistance	+RDS1	VS = +10V, ID = -1mA	1	+25°C	-	300	Ω
			2, 3	+125°C, -55°C	-	400	Ω
	-RDS1	VS = -10V, ID = +1mA	1	+25°C	-	300	Ω
			2, 3	+125°C, -55°C	-	400	Ω
Logic Level Voltage	VAL	Note 1	1, 2, 3	+25°C, +125°C, -55°C		0.8	V
	VAH	Note 1	1, 2, 3	+25°C, +125°C, -55°C	2.4	-	V

NOTE:

1. Use for forcing conditions for all DC tests unless otherwise specified.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device tested at +VSUPPLY = +15V. -VSUPPLY = -15V, VEN = 2.4V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Break-Before-Make Time Delay	tD	RL = 200Ω	9	+25°C	25	-	ns
Propogation Delay Times: Address Inputs to I/O Channel Times	tA	RL = 10MΩ	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	1000	ns
Enable to I/O	tON(EN)	RL = 200Ω	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	1000	ns
	tOFF(EN)	RL = 200Ω	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	1000	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device tested at +VSUPPLY = +15V, -VSUPPLY = -15V, VEN = 2.4V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS		NOTE	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance: Address Input	CA	V+ = V- = 0V f = 1MHz		1	+25°C	-	12	pF
Capacitance: Output Switch	COS	V+ = V- = 0V f = 1MHz	HS-0506RH	1	+25°C	-	90	pF
			HS-0507RH	1	+25°C	-	50	pF
Capacitance: Input Switch	CIS	V+ = V- = 0V f = 1MHz		1	+25°C	-	12	pF
Charge Transfer Error	VCTE	VS = GND VGEN = 0V to 5V		1	+25°C	-	10	mV
Off Isolation	VISO	VEN = 0.8V,RL = 1kΩ , CL = 15pF,VS = 7 VRMS f = 100kHz		1, 2	+25°C	-50	-	dB

NOTES:

1. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Worst case isolation occurs on channel 8B due to proximity of the output pins.

TABLE 4A. POST 10K RAD DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device tested at +VSUPPLY = +15V. -VSUPPLY = -15V, VEN = 2.4V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS		TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	IIH	Measure Inputs Sequentially GND All Unused Inputs		+25°C	-1.0	1.0	µA
	IIL			+25°C	-1.0	1.0	µA
Leakage Current into the Source Terminal of an "OFF" Switch	+IS(OFF)	VS = +10V, VD = -10V, VEN = 0.8V All Unused Inputs = -10V		+25°C	-50	+50	nA
	-IS(OFF)	VS = -10V, VD = +10V, VEN = 0.8V All Unused Inputs = +10V		+25°C	-50	+50	nA
Leakage Current into the Drain Terminal of an "OFF" Switch	+ID(OFF)	VD = +10V, VEN = 0.8V All Unused Inputs = -10V	HS-0506RH	+25°C	-300	+300	nA
			HS-0507RH	+25°C	-200	+200	nA
	-ID(OFF)	VD = -10V, VEN = 0.8V All Unused Inputs = +10V	HS-0506RH	+25°C	-300	+300	nA
			HS-0507RH	+25°C	-200	+200	nA
Leakage Current from an "ON" Driver into the Switch (Drain)	+ID(ON)	VS = VD = +10V All Unused Inputs = -10V	HS-0506RH	+25°C	-300	+300	nA
			HS-0507RH	+25°C	-200	+200	nA
	-ID(ON)	VS = VD = -10V All Unused Inputs = +10V	HS-0506RH	+25°C	-300	+300	nA
			HS-0507RH	+25°C	-200	+200	nA
Positive Supply Current	I(+)	VA = 0V, VEN = 2.4V		+25°C	-	3.0	mA

TABLE 4A. POST 10K RAD DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device tested at +VSUPPLY = +15V. -VSUPPLY = -15V, VEN = 2.4V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Negative Supply Current	I(-)	VA = 0V, VEN = 2.4V	+25°C	-1.0	-	mA
Standby Positive Supply Current	+ISBY	VA = 0V, VEN = 0V	+25°C	-	3.0	mA
Standby Negative Supply Current	-ISBY	VA = 0V, VEN = 0V	+25°C	-1.0	-	mA
Switch "ON" Resistance	+RDS1	VS = +10V, ID = +1mA	+25°C	-	400	Ω
	-RDS1	VS = -10V, ID = -1mA	+25°C	-	400	Ω
Logic Level Voltage	VAL	Note 1	+25°C	-	0.8	V
	VAH	Note 1	+25°C	2.4	-	V

NOTE:

1. Use for forcing conditions for all DC tests unless otherwise specified.

TABLE 4B. POST 10K RAD AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device tested at +VSUPPLY = +15V. -VSUPPLY = -15V, VEN = 2.4V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Propagation Delay Times: Address Inputs to I/O Channel Times	tA	RL = 10MΩ	+25°C	-	1000	ns
Enable to I/O	tON(EN)	RL = 200Ω	+25°C	-	1000	ns
	tOFF(EN)	RL = 200Ω	+25°C	-	1000	ns

TABLE 5. BURN-IN DELTA PARAMETERS (T_A = +25°C)

Device tested Per Table 1.

PARAMETERS	SYMBOL	DELTA LIMITS
Input Leakage Current	IIH, IIL	±100nA
Leakage Current into the Source Terminal of an "OFF" Switch	+IS(OFF)	±10nA
	-IS(OFF)	±10nA
Leakage Current into the Drain Terminal of an "OFF" Switch	+ID(OFF)	±10nA
	-ID(OFF)	±10nA
Leakage Current from an "ON" Driver into the Switch (Drain)	+ID(ON)	±10nA
	-ID(ON)	±10nA
Switch On Resistance	R(DS)	±50Ω
	R(DS)	±50Ω
Positive Supply Current	I(+)	±300µA
Negative Supply Current	I(-)	±100µA
Positive Standby Supply Current	+ISBY	±300µA
Negative Standby Supply Current	-ISBY	±100µA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	MIL-STD-883 METHOD	GROUP A SUBGROUPS	
		TESTED FOR -Q	RECORDED FOR -Q
Initial Test	100% 5004	1, 9	1 (Note 2)
Interim Test	100% 5004	1, 9, Δ	1, Δ (Note 2)
PDA	100% 5004	1, Δ	–
Final Test	100% 5004	2, 3, 10, 11	-
Group A (Note 1)	Sample 5005	1, 2, 3, 9, 10, 11	-
Subgroup B5	Sample 5005	1, 2, 3, Δ	1, 2, 3, Δ (Note 2)
Subgroup B6	Sample 5005	1	-
Group D	Sample 5005	1	-
Group E, Subgroup 2	Sample 5005	1	-

NOTES:

1. Alternate Group A testing in accordance with MIL-STD-883 Method 5005 may be exercised.
2. Table 5 parameters only.

Intersil Space Level Product Flow -Q

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM) (Note 1)

GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In, Condition A or B, 72 hrs. min., +125^{o}C min., Method 1015

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% PDA 1, Method 5004 (Note 2)

100% Dynamic Burn-In, Condition D, 240 hrs., +125^{o}C or Equivalent, Method 1015

100% Interim Electrical Test 2 (T2)

100% Delta Calculation (T0-T2)

100% PDA 2, Method 5004 (Note 2)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic (X-Ray), Method 2012 (Note 3)

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 4)

Sample - Group B, Method 5005 (Note 5)

Sample - Group D, Method 5005 (Notes 5 and 6)

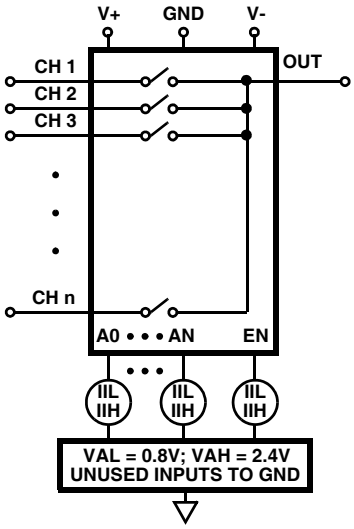
100% Data Package Generation (Note 7)

NOTES:

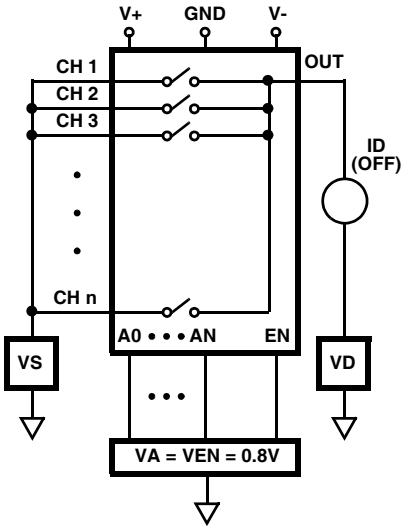
1. Modified SEM Inspection, not compliant to MIL-STD-883, Method 2018. This device does not meet the Class S minimum metal step coverage of 50%. The metal does meet the current density requirement of <2 E^5 A/cm^2. Data provided upon request.
2. Failures from subgroup 1 and deltas are used for calculating PDA. The maximum allowable PDA = 5%.
3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
5. Group B and D inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for Group B test, Group B samples, Group D test and Group D samples.
6. Group D Generic Data, as defined by MIL-I-38535, is optional and will not be supplied unless required by the P.O. When required, the P.O. should include a separate line item for Group D generic data. Generic data is not guaranteed to be available and is therefore not available in all cases.
7. Data Package Contents:
   - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).
   - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Intersil.
   - X-Ray report and film. Includes penetrometer measurements.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Lot Serial Number Sheet (Good units serial number and lot number).
   - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
   - Group B and D attributes and/or Generic data is included when required by the P.O.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

Test Circuits

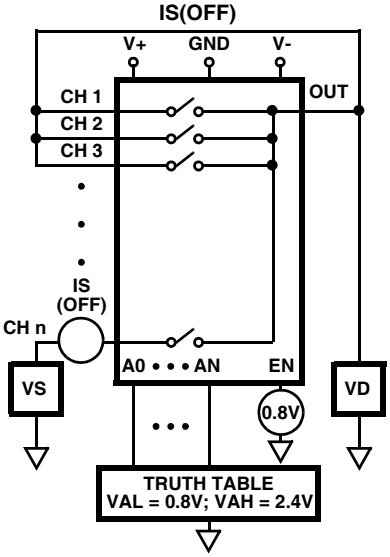
INPUT LEAKAGE CURRENT



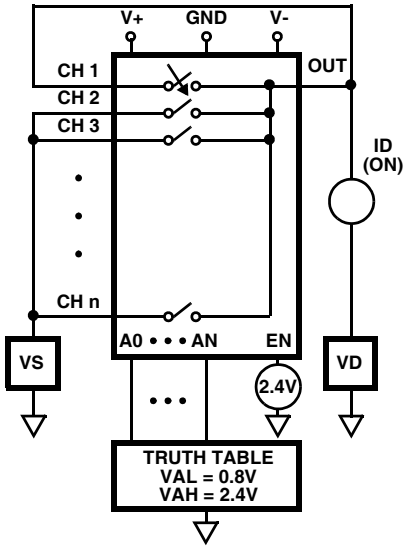
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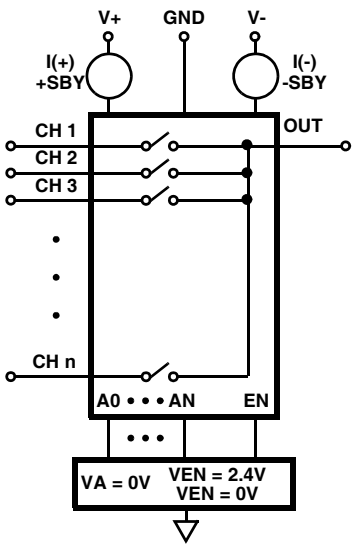
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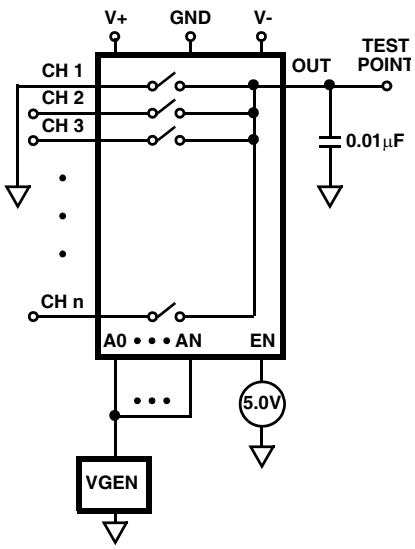
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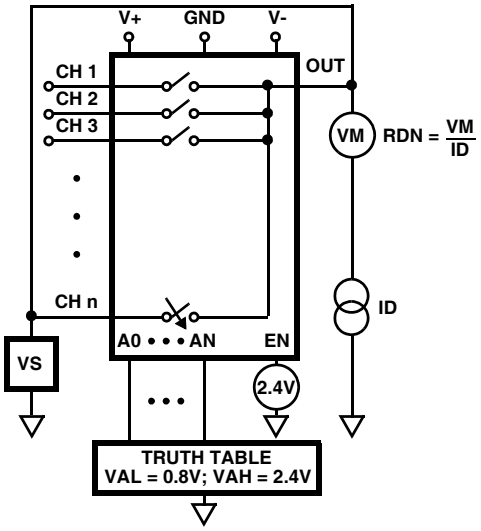
SUPPLY CURRENTS



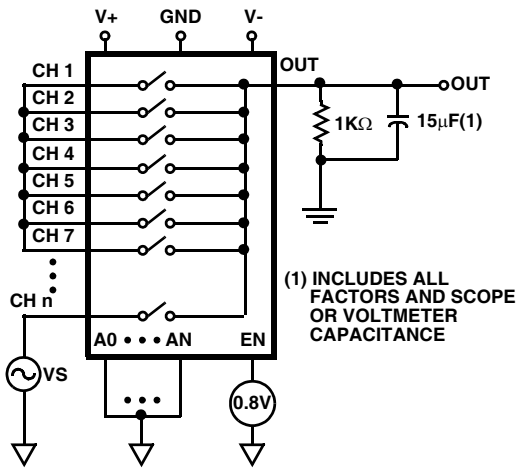
CHARGE TRANSFER ERROR



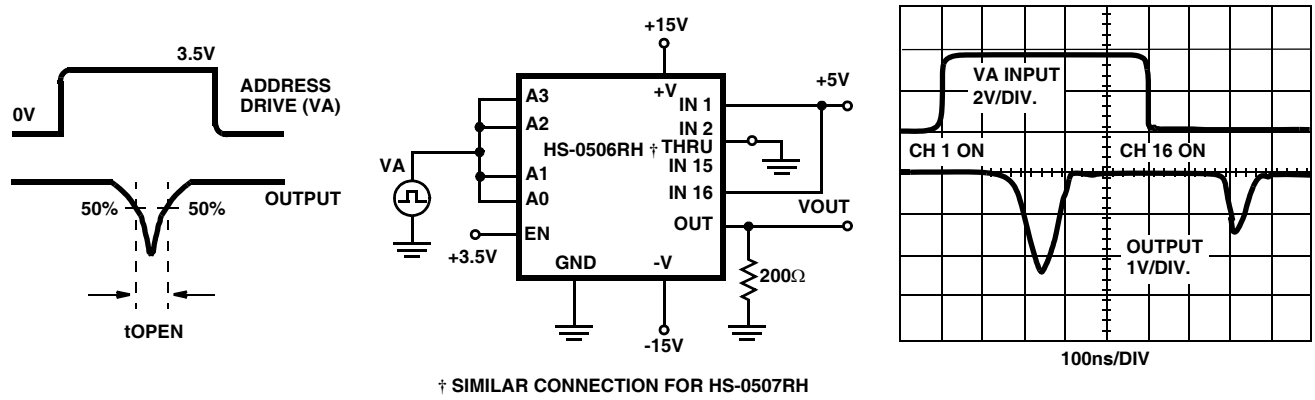
RDS



OFF CHANNEL ISOLATION

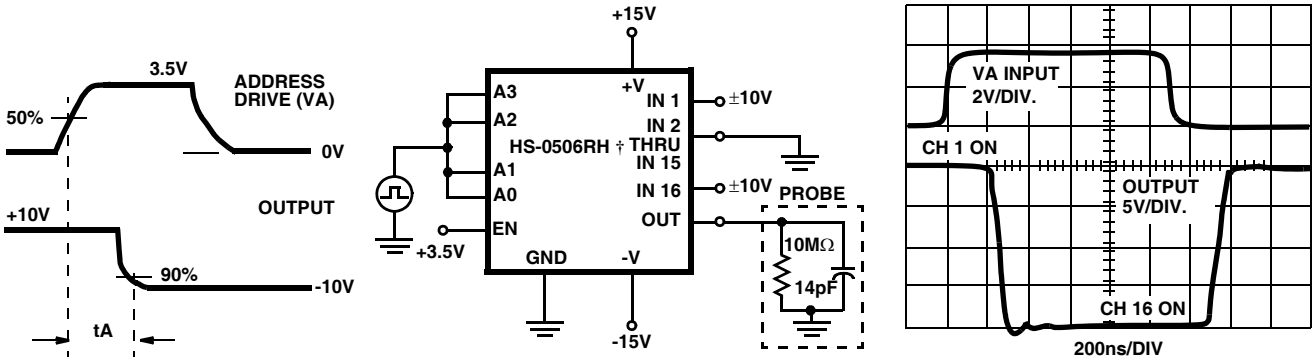


Switching Waveforms



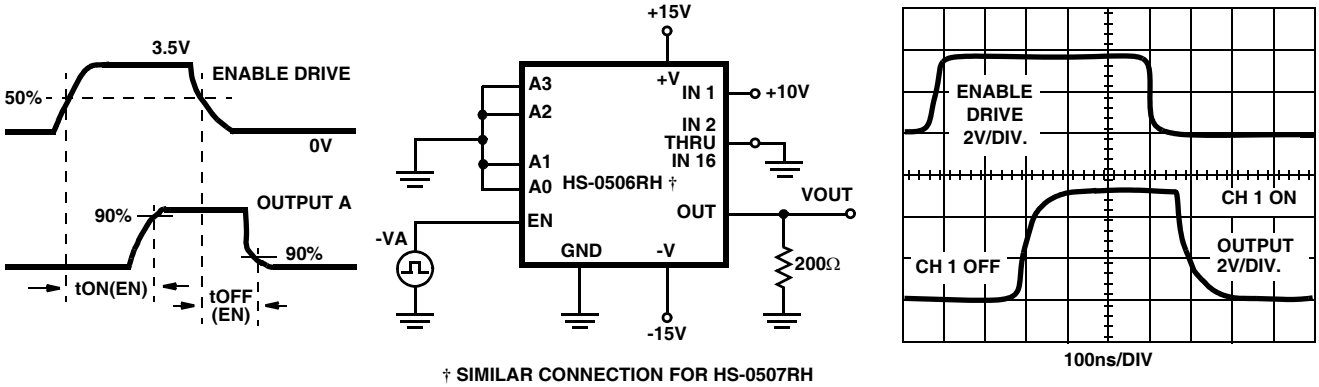
† SIMILAR CONNECTION FOR HS-0507RH

FIGURE 1. BREAK-BEFORE-MAKE DELAY (tOPEN)



† SIMILAR CONNECTION FOR HS-0507RH

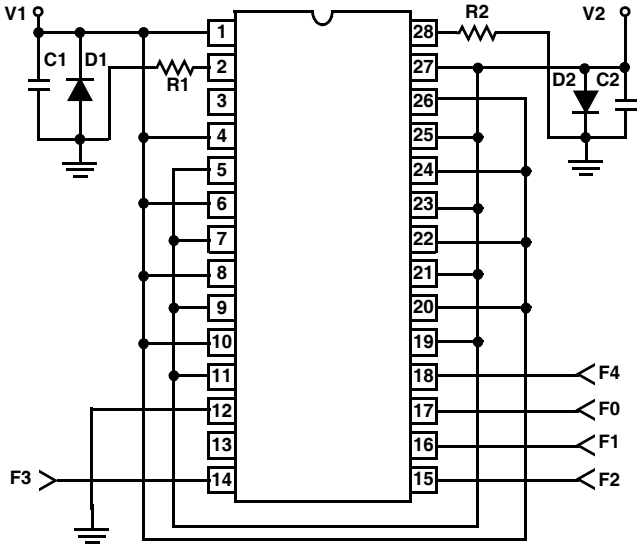
FIGURE 2. ACCESS TIME vs LOGIC LEVEL (HIGH)



† SIMILAR CONNECTION FOR HS-0507RH

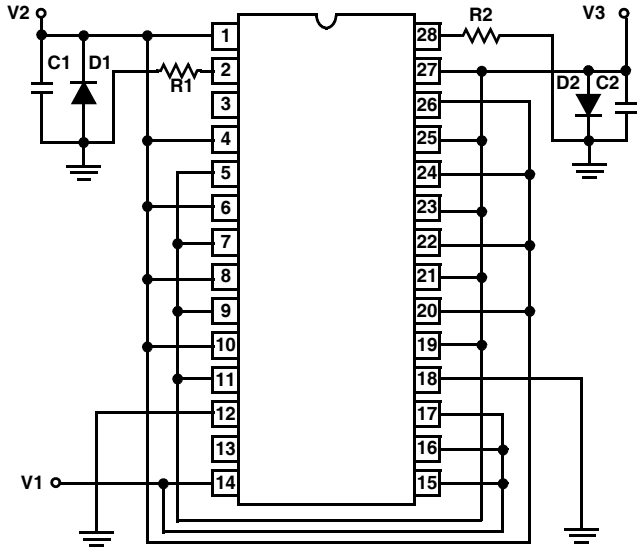
FIGURE 3. ENABLE DELAY tON(EN), tOFF 9EN)

Burn-Circuits



DYNAMIC

V1 = +15V minimum, +16V maximum
V2 = -15V maximum, -16V minimum
R1, R2 = 10kΩ, ± 5%, 1/4 or 1/2W (per socket)
C1, C2 = 0.01μF minimum (per socket) or 0.1μF minimum (per row)
D1, D2 = 1N4002 or equivalent (per board)
F0 = 100kHz, 10%; F1 = F0/2; F2 = F1/2; F3 = F2/2; F4 = F3/2
40% - 60% duty cycle; VIL = 0.8V maximum;
VIH = 4.0V minimum



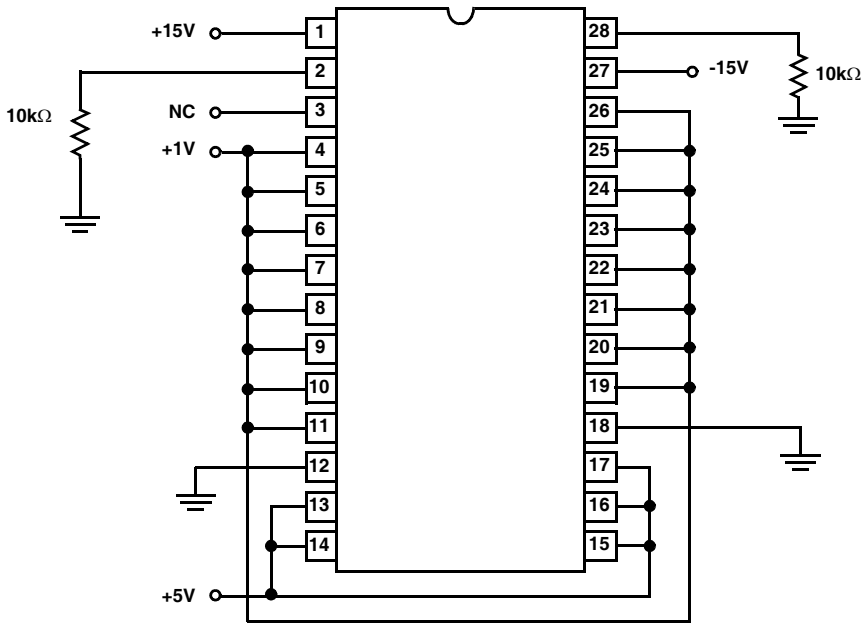
STATIC

V1 = +5V minimum, +6V maximum
V2 = +15V minimum, +16V maximum
V3 = -15V maximum, -16V minimum
R1, R2 = 10kΩ, ±5%, 1/4 or 1/2W (per socket)
C1, C2 =0.01μF minimum (per socket) or 0.1μF minimum (per row)
D1, D2 = 1N4002 or equivalent (per board)

NOTES:

1. The above test circuits are utilized for all package types.
2. The dynamic test circuit is utilized for all life testing.

Irradiation Circuit



Schematic Diagrams

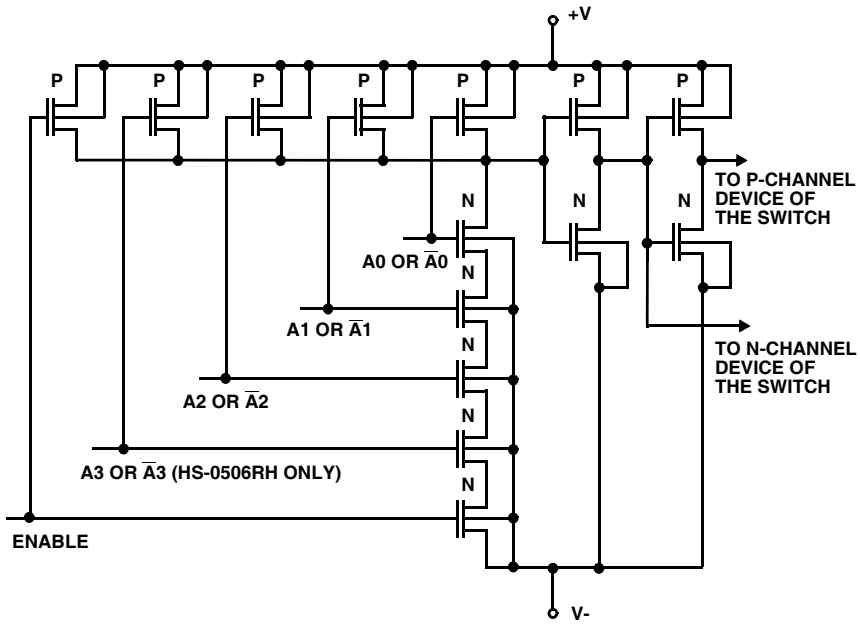


FIGURE 4. ADDRESS DECODER

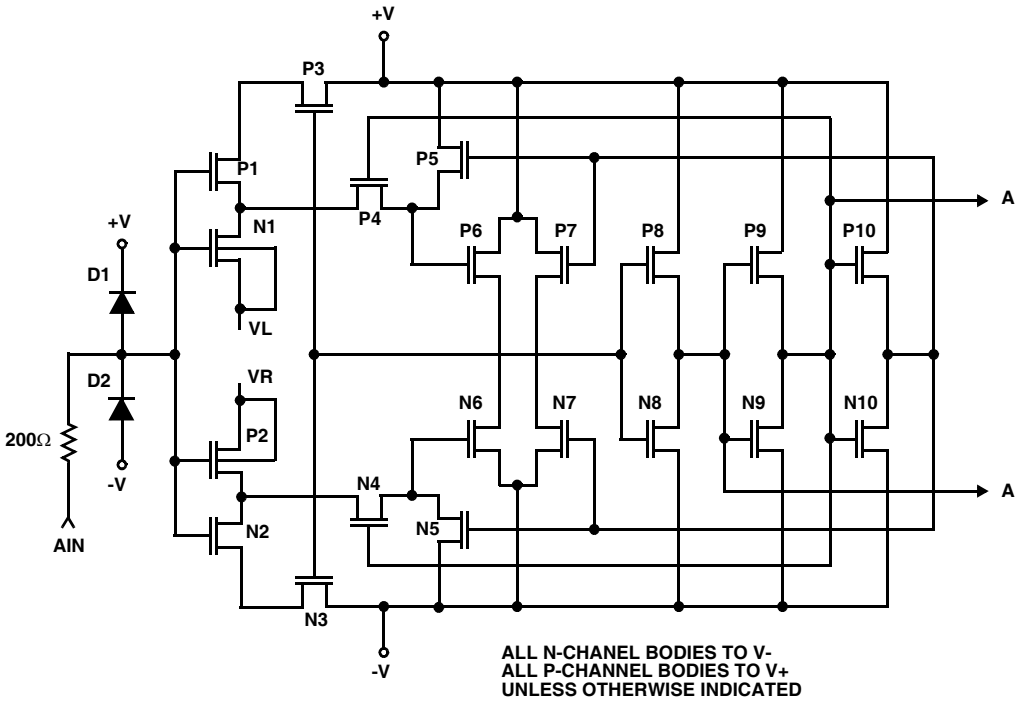


FIGURE 5. ADDRESS INPUT BUFFER LEVER SHIFTER

Schematic Diagrams (Continued)

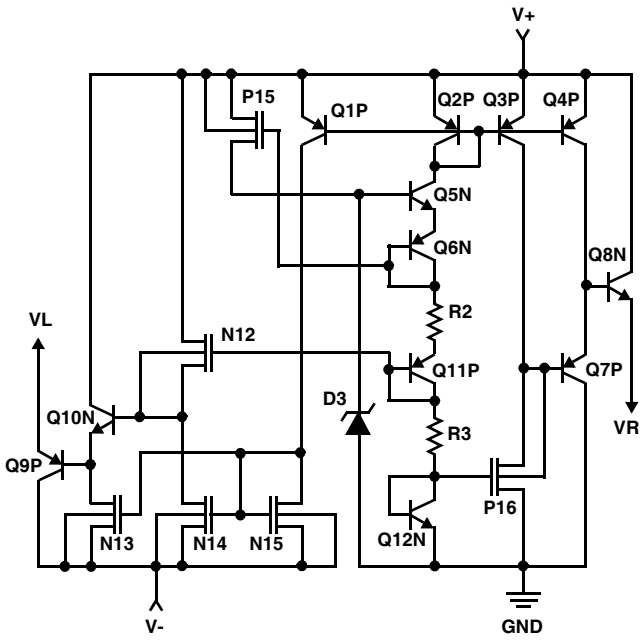


FIGURE 6. TTL REFERENCE CIRCUIT

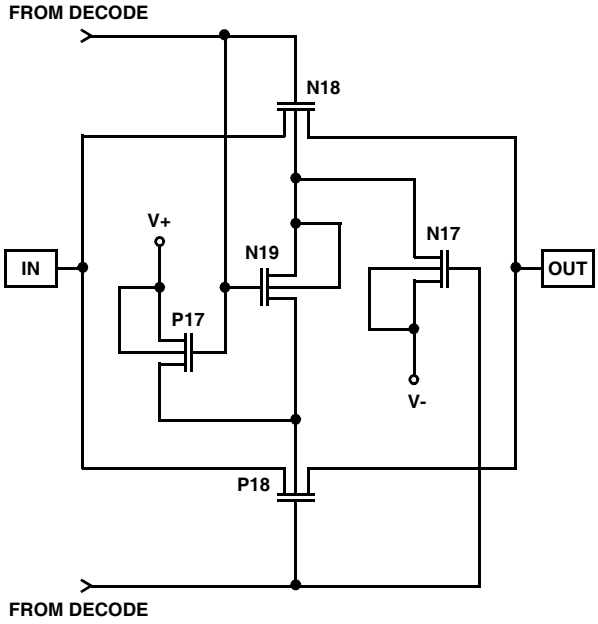


FIGURE 7. MULTIPLEX SWITCH

Metallization Topology

DIE DIMENSIONS:
82 x 129 x 19 mils

METALLIZATION:
Type: Al
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

WORST CASE CURRENT DENSITY:
$< 2.0 \times 10^5$ A/cm^2

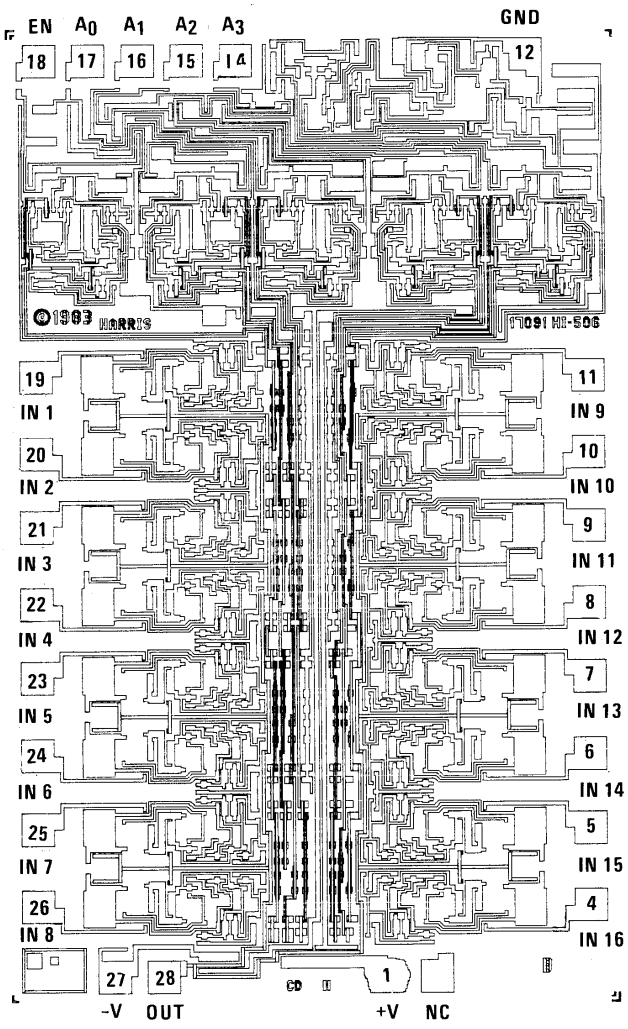
TRANSISTOR COUNT:

HS-0506RH	421
HS-0507RH	421

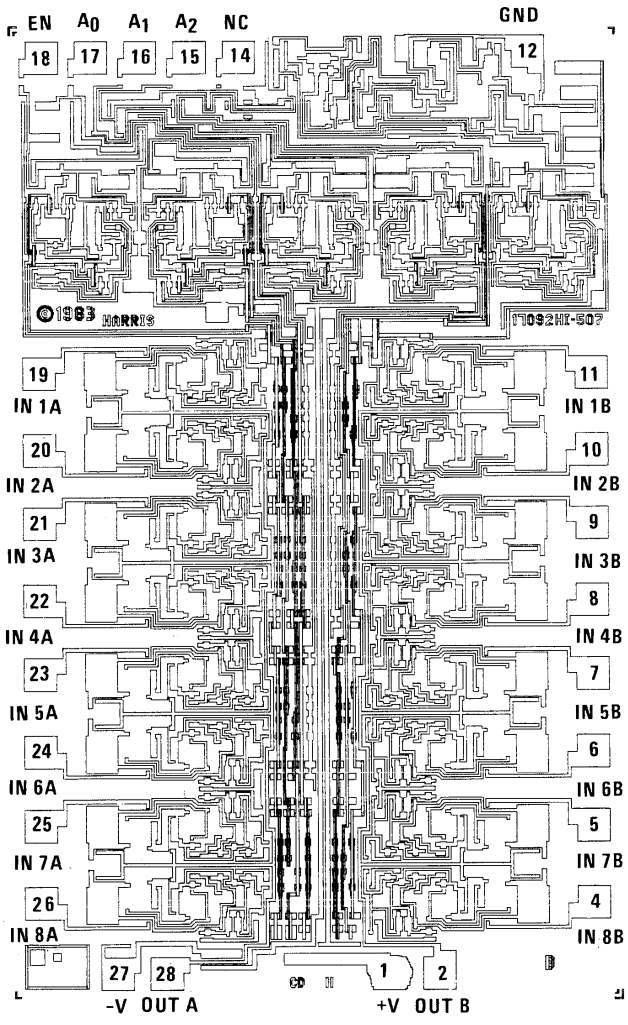
PROCESS: CMOS-DI

Metallization Mask Layout

HS-0506RH



HS-0507RH



NOTE: Pad numbers correspond to DIP pin numbers only.