HPM10

Power Management IC for Hearing Aids

Introduction

HPM10 is a Power Management IC (PMIC) that provides a high−performance solution for rechargeable batteries in hearing aids and hearing implant devices. Responsible for generating the voltage needed by the hearing aid, it manages the charging algorithms such that the battery autonomy and the number of charging cycles are optimized. The rechargeable chemistries supported include silver−zinc (AgZn), and lithium−ion (Li−Ion). HPM10 also detects zinc−air (Zn−Air) and nickel−metal hydride (Ni−MH) batteries but doesn't charge them.

HPM10 includes a Charger Communication Interface (CCIF) to inform the hearing aid charger about the charging progress. Other battery information such as voltage levels, current levels, temperature, and different types of battery failures can also be communicated.

HPM10 has the flexibility that allows easy integration into various types of hearing aids. It can be used without any connection to the main hearing aid digital signal processing (DSP), and manage the switch on and off operation, as well as the battery EOL control by−itself. Closer integration and communication with the main hearing aid DSP can also be obtained.

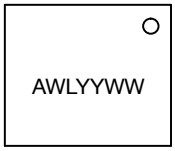
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WLCSP29
CASE 567MK

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
HPM10−W29A100G	WLCSP29 (Pb−Free)	5,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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KEY FEATURES

Supports Multiple Battery Types: Can charge and manage the power of multiple battery chemistries, including rechargeable Li−ion and AgZn batteries. Ni−MH batteries and disposable Zn−Air batteries can be detected as well. An automatic chemistry detection system recognizes the battery type.

Flexibility to Support Multiple Battery Sizes: The charging parameters should be updated depending on the battery size. Parameters corresponding to one battery size can be stored in an One−Time Programmable (OTP) memory at customer site.

Power Supply: Provides a clean supply to the hearing aid DSP. When a Li−ion battery is used, a step−down capacitive divider or Charge Pump is used, providing a voltage between ~1.4 V and ~0.95 V. When a AgZn battery is used, a linear regulator can be used, providing a 1.5 V max. HPM10 can also directly provide the battery voltage to the hearing aid DSP. Eg., when a Zn−Air battery is used or if the DSP can handle the voltage of a AgZn battery.

Charger Communication Interface: Communicates the status of the charging process and battery voltage to the hearing aid charger and allows user interaction with HPM10.

Information sent in this mode includes:

- Battery voltage level and charge current
- Charge Mode phase
- Battery chemistry type
- Fault conditions

Battery Life Optimization: High−precision current and voltage sources are used to manage the battery charge curves with the precision required to optimize battery life duration.

Battery Supervision: Ensures that the battery doesn't fall below critical levels. This helps to maximize battery life.

Non−Volatile Memory (OTP): Stores charging parameters, trim codes, and general product specific settings.

Power On and Off Management: Based on a smart method between HPM10 and the hearing aid DSP.

SPECIFICATION

Table 1. ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Min	Max	Unit
VDDP	DC Supply Voltage for charging	−0.5	5.7	V
VDDIO	Digital I/O supply	−0.5	5.5	V
VDD_OTP	OTP Supply	−0.5	6.0	V
DVREG	Regulated supply for HPM10	−0.5	2.0	V
VBAT	DC supply voltage, battery connection	−0.5	5.5	V
VSSA	Analog ground	−0.5		V
VSS	Digital Ground	−0.5		V
VDDIO I/O pins	SCL, SDA, CCIF	−0.5	VDDIO+0.3	V
VBAT I/O pins	SWIN, CP1A, CP1B, CP2A, CP2B	−0.5	VBAT+0.3	V
VHA I/O pins	VHA, SWOUT, DS_EN, EXT_CLK, CLKDIV[2:0], AGZN_REG_EN, WARN	−0.5	2.0 (Note 1)	V
I_{REG}	Max DVREG Load Current		20	mA
I_{VDDP}	Max VDDP Source Current		30	mA
Temp	Storage temperature	−50	85	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Max value should not exceed VBAT +0.3 V

Table 2. ELECTRICAL OVERSTRESS IMMUNITY

Test	Reference	Test Conditions
ELECTROSTATIC DISCHARGE ON COMPONENT LEVEL:		
ESD − HBM	JESD22 − A114	2 kV (Note 2)
ESD − MM	JESD22 − A115	200 V
ESD − CDM	ESD−STM 5−3−1−1999	500 V all pins
Latch−up	JESD78	100 mA @ 25°C

2. All pins at room temperature

ELECTRICAL PERFORMANCE SPECIFICATIONS

Table 3. ELECTRICAL SPECIFICATIONS

Description	Symbol	Conditions	Min	Typ	Max	Units	Screened
OVERALL OPERATING CONDITIONS							
Analog DC supply	VDDP	DC Supply from charger	4.8	–	5.2 (Note 3)	V	✓
Digital IO supply	VDDIO		DVREG	–	VDDP	V	
OTP supply for Burning	VDD_OTP	During burn	5.5	–	6.0	V	✓
Supply voltage	VBAT	Li−Ion battery	2.7	–	4.3	V	✓
		AgZn battery	1.2	–	2.0	V	✓
		ZnAir battery	1.00	–	1.65	V	✓
Analog ground	VSSA			0		V	
Digital Ground	VSS			0		V	
Input clock frequency	EXT_CLK		0.125	–	32	MHz	
Operating temperature	Top		0	–	50	°C	
Extended Operating temperature	Top ext	(Note 4)	−20	–	70	°C	
Deep sleep current	Isleep	VBAT=3.8 V, T=25°C	–	15	150	nA	✓
CHARGE VOLTAGE AND CURRENT SOURCE							
Charge current range	Ichg		0	–	23	mA	✓
Charge current granularity	Ichg LSB		–	30	–	μA	
Current ripple	Ichg Ripple	Ichg=10 mA	–	15	150	μA	
Charge voltage precision		VBAT=3.8 V, Ichg= 0 mA			20	mV	✓
Charge current precision		VBAT=3.8 V, Ichg= 5 mA			200	uA	✓
CHARGER COMMUNICATION INTERFACE							
Transmit pull down resistor	TX Rdown	VDDP = 5 V	2.6	3.3	4.0	kOhm	✓
Transmit data rate	TX DR	VDDP = 5 V	1.9	2	2.1	kHz	✓
Transmit current modulation	TX Imod	Includes Rdown and switch impedance	1	1.5	2	mA	✓
Receive data rate	RX DR		1.9	2	2.1	kHz	
Receive voltage level for input high	RX Vih		VDDP+ 0.15	VDDP+ 0.2	VDDP+ 0.25	V	
Receive voltage level for input low	RX Vil		VDDP− 0.05	VDDP	VDDP+ 0.05	V	
Allowable Rise/Fall Time for VDDP Supply		Voltage modulation = 200 mV			100	μs	
STEP DOWN CHARGE PUMP (DIV3)							
Supply from battery (Li−Ion)	Vbat Li−Ion	When active	3.1	3.6	4.3	V	
Supply to hearing aid	VHA	Relative to VBAT. Iload = 1 mA	0.326	0.331	0.336	VBAT	✓
Switching frequency using EXT_CLK or a division of EXT_CLK	Freq		62	90	125	kHz	✓
Output impedance	Rout		–	6	10	Ohm	✓
Power efficiency	Eff	Iload = 1 mA (Efficiency calculation includes the HA_Current_Li_Ion)	80	See Table 4	–	%	✓
Ripple		Iload = 1 mA	–	–	50	mV	✓
Load current	Iload	For functional operation, VBAT = 3.6 V	–	–	15	mA	✓

Table 3. ELECTRICAL SPECIFICATIONS

Description	Symbol	Conditions	Min	Typ	Max	Units	Screened
HEARING AID MODE OSCILLATOR							
Clock frequency	HA_Fclk	T = 25°C, Vbat = 1.3 V	66	95	124	kHz	✓
Clock frequency temperature deviation		T = 0°C to 50°C	−10	−1	10	%fclk	
Clock frequency supply deviation		Vbat = 1 V to 4.3 V	−10	0.2	10	%fclk	
CRADLE MODE OSCILLATOR							
Clock frequency	Fclk	T = 25°C	250.88	256	261.12	kHz	✓
Clock frequency temperature deviation		T = 0°C to 50°C	−2	–	2	%fclk	
Clock frequency supply deviation		VDDP = 5.0 to 5.2 V	−1	–	1	%fclk	
DVREG Linear Regulator for the Digital Blocks							
Linear Regulator	DVREG		1.71	1.8	1.89	V	✓
Regulator PSRR	$DVREG_{PSRR}$	I_{LOAD}=200 μA		30		dB	✓
Load Current	I_{LOAD}				200	μA	✓
Load Regulation	$LOAD_{REG}$	Absolute change for 0−200 μA, VDDP=4.8 V			15	mV	✓
Equivalent series resistance	ESR			10		Ω	
BATTERY DETECTION (Hearing Aid Mode)							
Turn−On threshold		AgZn and ZnAir	1.045	1.1	1.155	V	✓
Turn−off hysteresis		AgZn and ZnAir		10		%	
Startup Delay		VBAT = 3 V, from SWIN step input to VHA turn−on		20		ms	
AgZn battery detection upper threshold		AgZn	2.09	2.2	2.31	V	✓
Li−Ion battery detection turn−on threshold		Lithium−Ion	2.85	3	3.15	V	✓
Li-Ion turn−off hysteresis		Lithium−Ion		5		%	
VOLTAGE SWITCH CONTROLLER							
Switch resistance (On)	Rsw			6	10	Ohm	✓
Switch off current	Isw_off	T = 25°C		10	100	nA	✓
AgZn REGULATOR							
Battery voltage	Vbat	For AgZn.	1.5	–	2	V	✓
AgZn regulator	Vagzn	Limiting regulator for AgZn > 1.5 V	1.4	1.5	1.58	V	✓
Regulator impedance	Ragzn	Load = 1 mA, Vbat = 1.8 V		5	10	Ohm	✓
Max load current	Imax	For functional operation, VBAT > 1.15 V	15			mA	✓
ANALOG−TO−DIGITAL CONVERTER (ADC)							
Sampling frequency per input channel	fs_CH	4 MUX inputs		0.20		KHz	
Input voltage range	I_ADC range	Referred to bandgap	0		VREF	V	
LSB resolution	ADCres	VREF = 900 mV		0.879		mV	
TEMPERATURE SENSOR							
Temperature Measurement Range	Trange		0		50	°C	
Temperature Precision		Over Trange	−5		5	°C	

Table 3. ELECTRICAL SPECIFICATIONS

Description	Symbol	Conditions	Min	Typ	Max	Units	Screened
DIGITAL INPUT THRESHOLDS							
EXT_CLK	HA_logic_th	Hearing Aid Mode, VBAT=3.8 V		VHA/2		V	
DS_EN, CLKDIV[2:0], AGZN_REG_EN	agzn_en_th	Hearing AidMode, VBAT=3.8 V		0.6		V	
SWIN	swin_th	Hearing Aid Mode		VBAT/2		V	
DS_EN Minimum Triggerable Pulse Width	ds_pw_min	Hearing Aid Mode, VBAT = 3.8 V		20	100 (Note 5)	μs	
SCL,SDA, ATST_EN	logic_th	CM mode		VDDIO/2		V	
HEARING AID MODE CURRENT							
HA_Current_Li_Ion	I_HA_Li	Hearing Aid Mode, VBAT=3.8 V		68		μA	✓
HA_Current_AgZn	I_HA_AgZn	Hearing Aid Mode, VBAT=1.8 V		30		μA	✓

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. During OTP programming, the maximum VDDP value is 5.7 V. This allows VDDP to be tied to VDD_OTP.
4. HPM10 is functional in this range, but is not supposed to meet specification in terms of voltages, currents, thresholds and precision.
5. We ensure that all parts will go into Deep Sleep Mode with a duration of the DS_EN signal longer than 100 us. However, 20 μs is the typical minimum duration value, which means a typical part will trigger with a 20 us duration of DS_EN.

Table 4. EFFICIENCY OF THE STEP DOWN CHARGE PUMP (DIV3) VS LOAD, AT 25°C, V_{in} = 3.6 V

Load (mA)	Efficiency (%)
0.5	75.5
1	86
2	89.6
3	93.5
5	94.3
7	94
9	93.3

HPM10 INTERNAL ARCHITECTURE

The architecture of the HPM10 chip is shown in Figure 1.

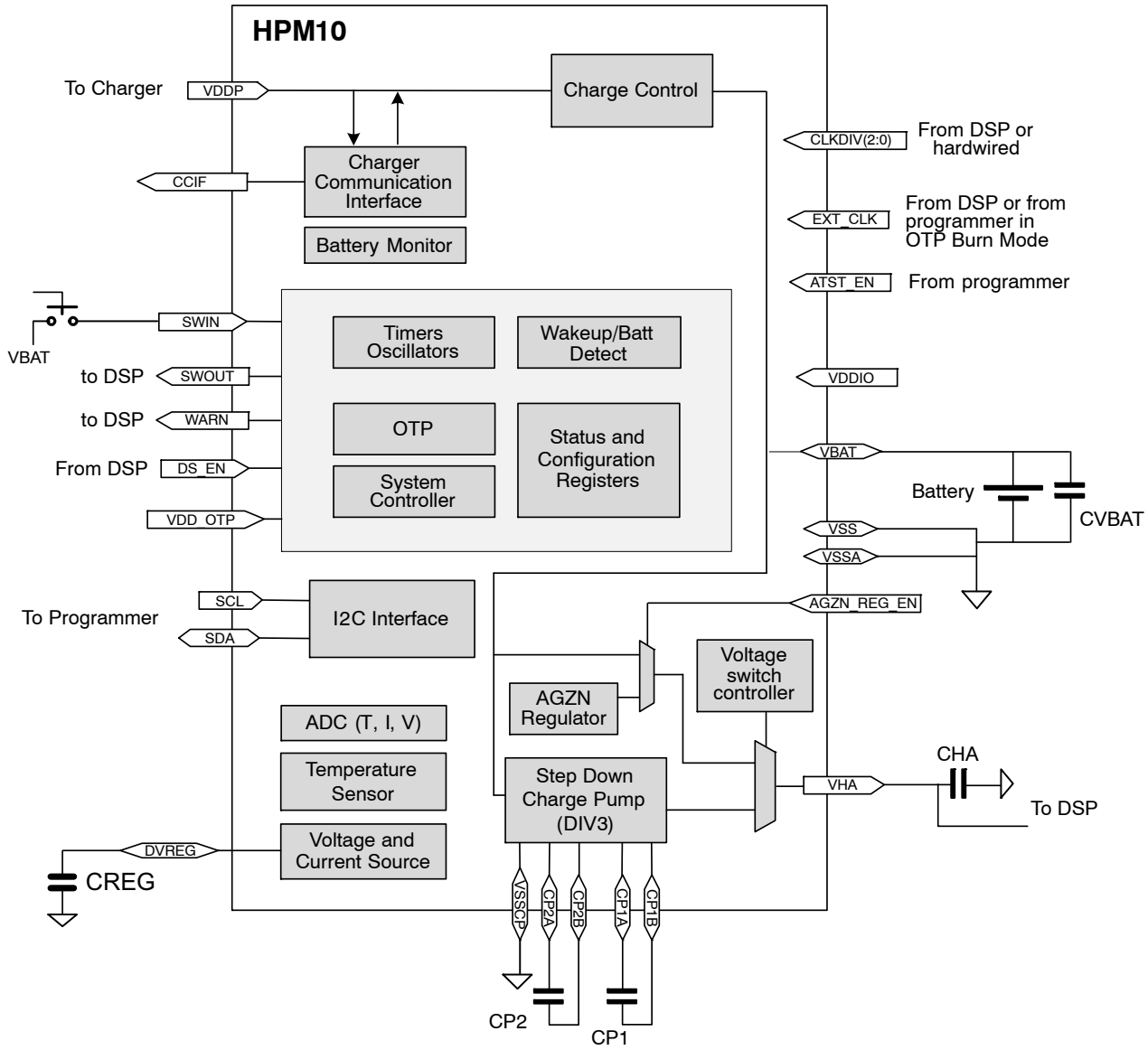


Figure 1. HPM10 Architecture

EXTERNAL COMPONENTS

HPM10 requires six external components listed in Table 4. Depending which type of rechargeable battery is used, some of the decoupling caps are not needed.

Table 5. EXTERNAL COMPONENTS

Component	Function	Typ. Value	Tol.	Units	Notes
Cp1	Capacitor 1 for charge pump	2.2	20%	μF	Required for Lithium−Ion For other batteries, CP1A and CP1B pins can be floating
Cp2	Capacitor 2 for charge pump	2.2	20%	μF	Required for Lithium−Ion For other batteries, CP2A and CP2B pins can be floating
Cha	VHA decoupling capacitor	0.1	20%	μF	
Cvbat	Battery decoupling cap	1	20%	μF	Cvbat should always be 5*Cha to ensure reliable startup
Creg	Voltage and current ref decoupling cap	6.8	20%	μF	
button	Button to interact with the system	–		–	Intermittent

CHIP INTERFACE SPECIFICATIONS

HPM10 has a total of 29 pads. Descriptions of these pads are given in Table 6.

Table 6. PAD DESCRIPTIONS

Pin Number	Pad Name	Description	Power Domain	I/O	A/D	Pull
E2	CLKDIV[0]	EXT_CLK divider ratio	VHA	I	D	Dw
D3	CLKDIV[1]	EXT_CLK divider ratio	VHA	I	D	Dw
C3	CLKDIV[2]	EXT_CLK divider ratio	VHA	I	D	Dw
A3	VDDIO	Supply for digital I/O, Should most commonly be connected to DVREG.		I	P	
B1	SCL	I^2C serial clock pad	VDDIO	I/O	D	U
A1	SDA	I^2C serial data line	VDDIO	I/O	D	U
A2	RESERVED	Do not connect				
B2	RESERVED	Do not connect				
A4	CCIF	Digital CCIF signal or tri−state Charge status	VDDIO	O	D	
C4	ATST_EN	OTP Burn: Connect to VDDIO during OTP burning. Leave floating or grounded for normal operation.	VDDIO	I	D	Ds
B3	DS_EN	Deep sleep enable input	VHA	I	D	Ds
D5	AGZN_REG_EN	Enable use of regulator when VBAT>1.5 V	VHA	I	D	Uw
D1	EXT_CLK	External clock input Also used to output oscillator clock to the system for test. Should be connected to programmer in OTP Burn Mode	VHA	I	D	Dw
D2	SWOUT	Level shifted version of SWIN input	VHA	O	D	
B4	VSS	Ground for digital circuits		I	P	
C5	WARN	Shutdown warning	VHA	O	D	
A5	VDDP	VDDP primary charger input		I	P	
B5	DVREG	Linear regulator for digital core		O	P	
D4	RESERVED	Do not connect				
F2	VSSCP	Ground for charge pump		O	P	
E3	CP2B	Charge pump cap 2 terminal B		O	A	
F3	CP2A	Charge pump cap 2 terminal A		O	A	
E5	CP1B	Charge pump cap 1 terminal B		O	A	
F5	CP1A	Charge pump cap 1 terminal A		O	A	
F1	VHA	Hearing aid DSP voltage connection		O	A	
F4	VBAT	Connection to battery		I	P	
E4	SWIN	Input for external button	VBAT	I	A	Dw2
C2	VDD_OTP	HV pad normally connected to VDDP used for OTP programming supply		I	P	
E1	VSSA	Ground for analog circuitry and OTP		I	P	

Legend:
Type: A = analog; D = digital; I = input; O = output; P = power
Dw = Internal Weak 1 MΩ pull−down
Uw = Internal Weak 1 MΩ pull−up
Dw2 = Internal Weak 2 MΩ pull−down
Ds = Internal 100 KΩ pull−down
U = Internal 20 kΩ pull−up: I^2C lines can have external pull up for extra drive, value defined by I^2C Standard, but not to be less than 1 kΩ

HPM10 USAGE IN A HEARING AID

HPM10 has the built−in flexibility to allow integration within various sorts of hearing instruments. The battery door can be sealed or unsealed. The hearing aid may have a pushbutton or may not. HPM10 can be integrated with the hearing aid DSP though dedicated communication lines, or it can work independently from the hearing aid DSP. The following list gives a few possible scenarios of integration:

Hearing Aid with a Push Button and Sealed Battery Door:

Cradle Charging

- When the hearing aid is inserted to the cradle, it will charge. While charging, the hearing aid will turn off.
- When the hearing aid is taken out from the cradle, it will go into Deep Sleep Mode (HPM10 in Deep Sleep Mode).

Power On/Off

- To turn on the hearing aid, use the pushbutton.
  - Logic high at SWIN signal is detected and turns on HPM10
  - HPM10 supplies the main DSP with VHA
- To turn off the hearing aid, use the pushbutton.
  - Logic high at SWOUT sent to main DSP
  - Main DSP to send DS_EN to HPM10 to turn VHA off

Store Shelf Mode

- To put the hearing aid in Store Shelf Mode, the same operation as turning the hearing aid off applies.

Battery

- When battery goes EOL: the hearing aid will automatically turn off (HPM10 in Deep Sleep Mode) through two possible mechanisms:
  - HPM10 goes into Deep Sleep Mode to protect the battery from over discharge
  - DSP detects low battery voltage and puts HPM10 into Deep Sleep Mode through the DS_EN pin

Hearing Aid with a Push Button and Unsealed Battery Door:

Cradle Charging

- When the hearing aid is inserted to the cradle, it will charge. While charging, the hearing aid will turn off.
- When the hearing aid is taken out from the cradle, it will go into Deep Sleep Mode (HPM10 in Deep Sleep Mode).

Power On/Off

- When the battery is removed, the hearing aid will shut down
- When the battery is inserted, the hearing aid will go into Deep Sleep Mode (HPM10 in Deep Sleep Mode).
- To turn on the hearing aid, use the pushbutton.
  - Logic high at SWIN signal is detected and turns on HPM10
  - HPM10 supplies the main DSP with VHA
- To turn off the hearing aid, use the pushbutton.
  - Logic high at SWOUT sent to main DSP
  - Main DSP to send DS_EN to HPM10 to turn VHA off

Battery

- When battery goes EOL, the hearing aid will automatically turn off (HPM10 in Deep Sleep Mode) through two possible mechanisms:
  - HPM10 goes into Deep Sleep Mode to protect the battery from over discharge
  - DSP detects low battery voltage and puts HPM10 in Deep Sleep Mode through the DS_EN pin.

Hearing Aid without Push Button and Sealed Battery Door

In this mode, it is possible that there won't be any communication lines between the DSP and HPM10.

Cradle Charging and Power On/Off

- When the hearing aid is inserted into the cradle, it will charge. While charging, hearing aid will turn off.
- When the hearing aid is taken out from the cradle, it will turn on.

Store Shelf Mode

- To put the hearing aid in Store Shelf Mode
  - Trigger DS_EN on HPM10 interface either over DSP or by bringing out the DS_EN pin in PCB. This would put HPM10 into deep sleep mode resulting in extended battery shelf life for the hearing aid.

Battery

- When battery goes EOL, the hearing aid will automatically turn off (HPM10 in Deep Sleep Mode) through two possible mechanisms:
  - HPM10 goes into Deep Sleep Mode to protect the battery from over discharge
  - DSP detects low battery voltage and puts HPM10 in Deep Sleep Mode through the DS_EN pin

Hearing Aid without a Push button and an Unsealed Battery

In this mode, it is possible that there won't be any communication lines between the DSP and HPM10.

Cradle Charging

- When the hearing aid is inserted to the cradle, it will charge. While charging, the hearing aid will turn off.
- When the hearing aid is taken out from the cradle, it will turn on.

Power On/Off

- When the battery is removed, the hearing aid will shut down
- When the battery is inserted, the hearing aid will turn on

Battery

- When the battery goes EOL, the hearing aid will automatically turn off (HPM10 in Deep Sleep Mode) through two possible mechanisms:
  - HPM10 goes into Deep Sleep Mode to protect the battery from over discharge
  - DSP detects low battery voltage and puts HPM10 in Deep Sleep Mode through the DS_EN pin

In all modes, when the device is removed from the cradle, it will either immediately turn on or wait until the pushbutton is pushed. This means that for the first and second use cases (Hearing Aid with a Pushbutton and Sealed Battery Door and Hearing Aid with a Pushbutton and Unsealed Battery Door), the hearing aid manufacturer will be able to configure HPM10 to directly switch on or wait for the pushbutton.

In case the hearing aid doesn't have a pushbutton, once the battery is fully charged and the hearing aid remains on the cradle, HPM10 includes a system that compensates the current drawn by its components detecting the cradle mode exit. In this case, the hearing aid can be left on the charger for an extended amount of time without any drain or extra charge on the battery.

Wakeup on SWIN Pushbutton: In a hearing aid that contains pushbuttons, HPM10 will wake up the entire system (VHA active) from Deep Sleep Mode when SWIN is closed to VBAT for 20 ms minimum.

Wakeup also requires a battery voltage appropriate for a healthy battery.

- For ZnAir or AgZn: VBAT > 1.1 V and VBAT < 2.2 V
- For Li−Ion: VBAT > 3.0 V

Wakeup on Battery Insertion: Waking up HPM10 on battery insertion requires an external capacitor from VBAT to SWIN. The SWIN pull down is a large 2 MΩ resistor. The time constant needs to be >200 ms (Cswin = 0.1 μF, R = 2 Meg).

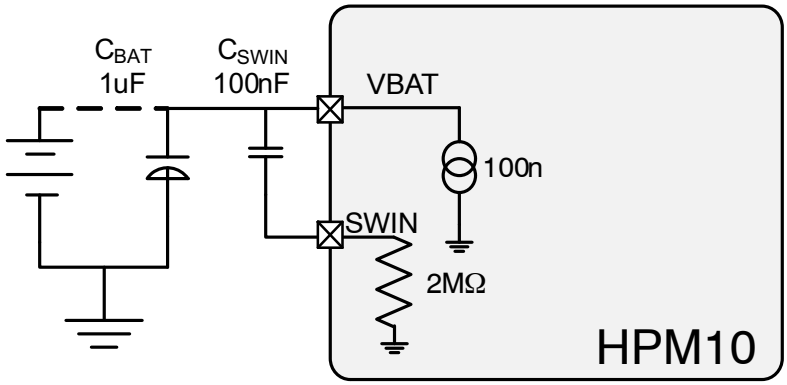


Figure 2. External Connection Required for a Proper Wakeup at Battery Insertion

This RC network effectively provide a high pulse of long enough duration for the wakeup block on HPM10 to latch ON and enable the DSP. Since the HPM10 latch on delay is about 20 ms, a pulse of about 200 ms provides a large margin to ensure that HPM10 reliably turns on.

During Hearing Aid Mode, if the battery discharges to its end−of−life then the DSP or HPM10 can trigger the Deep Sleep. Once in Deep Sleep the only way to wake up (in case there is no button) is to place in the charger.

Wakeup on Removal from Cradle: Waking up HPM10 when the hearing aid is removed from the charger requires OTP bit "no_button' to be set high. In this case, VHA will be turned on.

If the OTP bit "no_button' is set low, HPM10 will go in Deep Sleep Mode, and VHA will not be activated.

Shutdown Warning: When the hearing aid is placed in the Cradle, the output pad WARN signals the DSP that the power will soon shutdown. This signal is a level−shifted copy of the analog signal 'CH_CONN' (see Figure 3).

The time duration between the moment the WARN signal is raised to logic "1", and VHA being switched off, will allow the hearing aid DSP to get ready for shut down. This period of time will typically allow the hearing aid DSP to manage datalogging or mute the audio without glitches. This time period can be configured in the OTP with a resolution of 0.5 seconds, with a min value of 0.5 seconds and a max value of 127.5 seconds.

HPM10 WORKING MODES

HPM10 has three working modes represented in the state machine below.

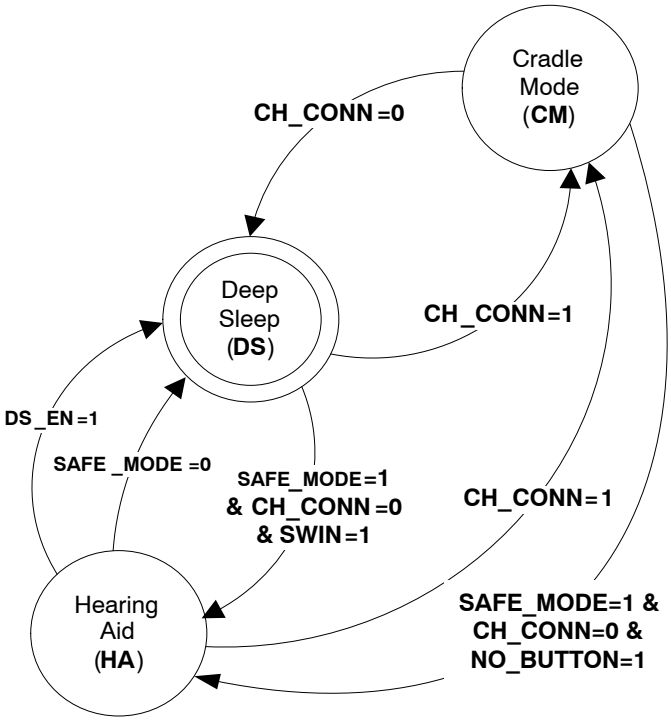


Figure 3. HPM10 State Machine

Deep Sleep Mode: A low power mode with all blocks turned off. HPM10 can enter Deep Sleep Mode in one of three ways:

- From Hearing Aid Mode when the host DSP toggles the DS_EN pin high. An example use−case for this transition is when a program is running on the host DSP, that determines that the hearing aid is not being worn or the measured battery voltage is below a specified value and puts the system into Deep Sleep Mode to save power.
- From Hearing Aid Mode when the battery voltage drops below the EOL set point (**VEOL** level), for the battery chemistry actively being used to avoid irreversible battery damage. This is when VBAT<1.0 V (for AgZN) or 2.2 V<VBAT<3.0 V (for Lithium−Ion). This will draw the *SAFE_MODE* status bit to 0.
- From Cradle Mode when the hearing aid charger is removed, in case the OTP bit “no_button” is not set.

Cradle Mode: The hearing aid will enter in Cradle Mode when the hearing Aid is physically connected to Cradle (*CH_CONN*=1). In this mode, the hearing aid battery is being charged.

Once in this state, the following sequence of processes will occur:

- The OTP is enabled and its contents are copied to internal latches.
- After the OTP contents have been read, a Cyclic Redundancy Check (CRC) is made by the controller. If it fails, the system transitions to completion phase in Cradle Mode and an error flag is set.
- If the CRC passes, the controller starts the charging process.

The charging process is controlled by a controller and firmware in ROM.

Hearing Aid Mode: The hearing aid DSP power is supplied by HPM10 and there is no digital logic running on HPM10. In this mode, the hearing aid is in normal operation mode and receives its supply voltage from HPM10. HPM10 can enter Hearing Aid Mode in two ways:

- From Deep Sleep after SWIN goes high from a button press. The battery voltage must be in a valid range.
- From Cradle Mode after removed from Cradle with OTP bit NO_BUTTON=1. The battery voltage must be in a valid range.HPM10 is either clocked with the Hearing Aid Mode Oscillator, or with the divided EXT_CLK.

The recommended tasks for the host DSP in Hearing Aid Mode are as follows:

- Set the external clock division ratio (if desired) by driving the 3 CLKDIV pins (*)
- Apply a valid clock to EXT_CLK pin

- Periodically monitor pin VHA using its on−board ADC
- Monitor SWOUT to determine button press events
- Monitor the WARN to determine if the hearing aid has been placed in cradle, in which case the DSP should shut itself down gracefully before HPM10 cuts the power to VHA.
- Toggle pin DS_EN to logical high (VHA level), if it needs to put HPM10 into Deep Sleep Mode

(*): CLKDIV can be configured by the DSP (through GPIO for example) or through physical connection.

In Hearing Aid Mode, voltage monitoring is used to prevent turn−on if battery voltage is not acceptable, and to control the output mode of the VHA supply.

The voltage levels and modes are as follows:

- 1.0 V to 1.5 V The battery type could be AgZn, Zn−Air, or NiMH. A low impedance switch connects VBAT to VHA to power the DSP.
- 1.5 to 2.2 V The battery type is likely AgZn. If pin AGZN_REG_EN=floating, then the VHA voltage is powered by a 1.5 V regulator. This is to protect those DSPs that are not able to handle the unregulated AgZn voltage. For those DSP that can handle maximum AgZn battery voltages, the pin AGZN_REG_EN=0V will enable the low impedance switch between VBAT and VHA.
- 3.0 V and above. The battery type is Li_Ion. VHA is powered by a divide by 3 step down converter.

VBAT voltages outside of these ranges will not enable the VHA, and the DSP will not be powered. Note that each of these thresholds have hysteresis to ensure stable operation.

The following figure indicates how HPM10 monitors voltage in Hearing Aid Mode.

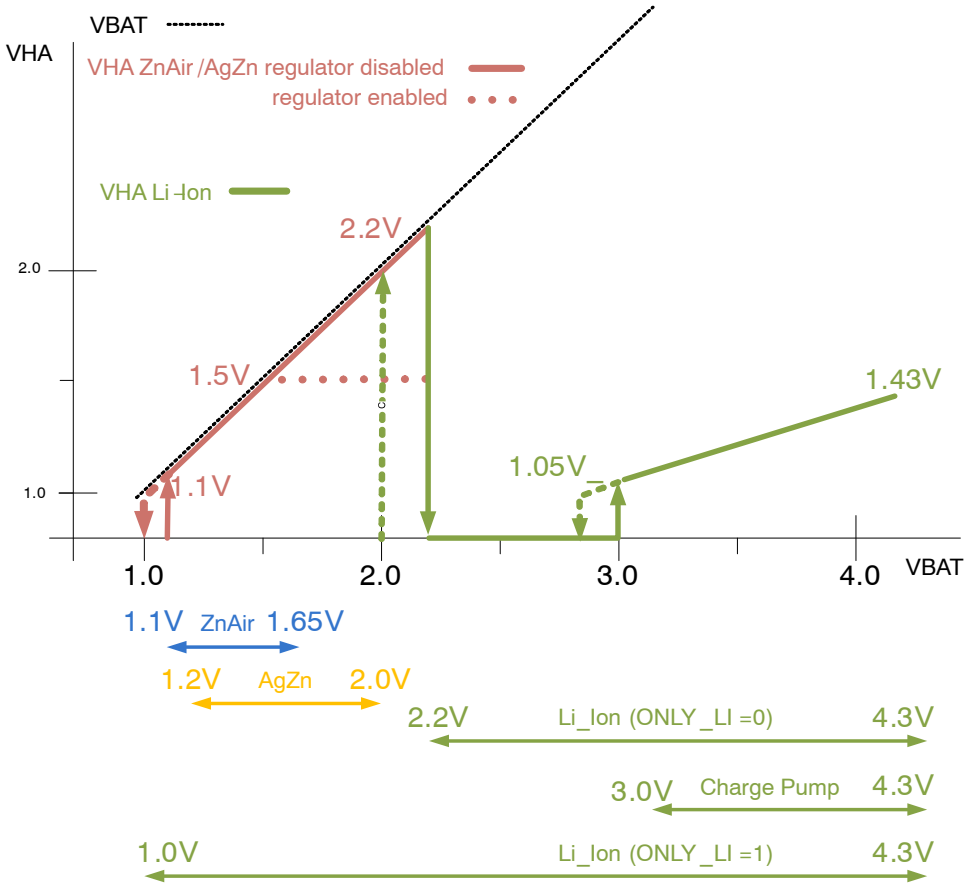


Figure 4. Hearing Aid Mode: Voltage Monitoring

Interfaces to Host DSP

In Hearing Aid Mode, the SWOUT pin provides a level shifted version of the SWIN pin. The SWOUT pin would typically be connected to the host DSP's GPIO pin so that the button on the hearing aid connected to SWIN can also be used for other functions such as memory select or volume control.

The DS_EN input pin is provided for the DSP to trigger Deep Sleep Mode:

- It is active in Hearing Aid Mode only, it is ignored in Cradle Mode
- It is protected from glitches with a 100 μsec de−glitch circuit
- The host DSP will need to hold the pin high for greater than 100 usec to put HPM10 into Deep Sleep Mode
- It has a 100 kOhm pull down
- During power−up it will be held low as it will be connected to the host DSP's GPIO pin with the following assumptions:
  - The GPIO is by default in input mode during power up
  - The resistance used for pull−up is greater than 250 KOhm
  - After boot−up, the host DSP configures the GPIO pin as an output in a low state
- If the GPIO pull−up resistance is less than 250 kOhm, it is necessary to add an external resistor to VSS such that the ratio of pull−up to pull−down resistance is more than 2.5

DIV3 (Step Down Charge Pump)

In Hearing Aid Mode, the DIV3 step−down charge pump (CP) is used when Li−Ion batteries are used. The DIV3 CP uses 2 external capacitors plus 1 decoupling capacitor to divide the VBAT by a factor of 3. The output impedance of the charge pump is fixed, and the VHA will track variation in VBAT.

If VBAT is insufficient to power DIV3 CP, the DIV3 CP will be shut off. Based on the Li_Ion discharge curve, the battery is nearly discharged when VBAT<3.1V, and so a threshold around 3.1 V would be acceptable for the DSP to use as a turn off threshold. This is equivalent to 3.1/3=1.03 V on VHA. The HPM10 turn off threshold is much lower (typically 2.8 V) as a fail−safe in case the DSP is unable to turn off HPM10.

The DIV3 CP can only be activated when in Hearing Aid Mode.

The input clock to DIV3 CP comes initially from the hearing aid oscillator, which also is only active in HA mode. After the DIV3 starts up and the DSP turns on, if there is detected a clock signal on the EXT_CLK pad, it will be used as the master clock in Hearing Aid Mode. When using the *EXT_CLK*, the range of frequency can be as much as −2%/+95% due to the limited division steps.

AgZn Regulator

In Hearing Aid Mode, the AgZn regulator can be used to limit voltage below 1.5 V when the voltage is above 1.5 V (first discharge plateau). This regulator will be used in case the hearing aid DSP input voltage range is limited to 1.5 V. Disabling this regulator is done by tying the AGZN_REG_EN pin to ground.

Note that if Zinc−Air or AgZn battery are used and VBAT < 1.5 V, the AgZn regulator will not be used and the VBAT will be shorted to the *VHA*. If VBAT > 1.45 V, the AgZn regulator is enabled. Hysteresis has been added to all these thresholds.

If Li−Ion battery is installed, the AgZn Regulator is disabled and the DIV3 is enabled.

Slave I^2C

In Cradle Mode or during debug: HPM10 has a slave I^2C port to allow an external host device to access all the HPM10 internal registers when in Cradle Mode. It is also used for OTP burning, standalone test, and debug. When in Hearing Aid Mode, the I^2C is off.

Charger Communication Interface (CCIF)

This is a bi−directional interface that will communicate the status of the charging process in Cradle Mode to the hearing aid charger and allow user interaction with HPM10. Normally, once the hearing aid is assembled and the battery attached, this interface is the only means to monitor the battery health. The CCIF will communicate with the hearing aid charger using a superset of the 'Qi' (inductive power standard) based communications protocol using an UART type encoding. This protocol has been developed for wireless charging systems. Although this version of HPM10 is only supporting wired charging, this protocol will be used to facilitate an easier migration to a wireless charging mode. The data rate is fixed to 2 kHz.

Some of the information sent in this mode is:

- Battery voltage
- Current levels
- Ambient temperature
- Accumulated charge
- Charge mode phase
- Battery chemistry type
- Fault conditions

This communication supports data transfer between the HPM10 and the Primary Charger. This physical link is the VDDP power connection. Bidirectional communication (half−duplex) is supported. The communication from the HPM10 to Primary is using "load modulation", where the VDDP is loaded with a low valued resistor to represent a "0". The communication from Primary to HPM10 uses VDDP voltage modulation.

HPM10 to Primary Charger (Transmit): The CCIF digital signal (UART type) is converted into a modulated

load on the VDDP wired supply. This current modulation is superimposed on the existing current that is used to charge the battery. State transitions will cause short current transient steps that need to be ignored by the Primary Charger data detector. To support the HPM10 usage in a wireless recharging device, an alternate interface has been provided. It is composed of pad “CCIF” that is a digital output duplicating the raw UART signal (i.e. not the differential encoded data).

The CCIF pin can be configured in the OTP to provide a static signal that can be used by the system to provide information on the battery charge as follow:

CCIF Pin State	Corresponding Information
HI	Charge Complete
LO	Fault
HI−Z	Neither

In OTP Burn mode (ATST_EN=HIGH), the CCIF pin is used as an external reset input active LOW. This reset is necessary during the OTP READ procedure and it is to ensure that digital is in a known good state and the OTP contents have been loaded before doing the read. The CCIF pin, when in input mode, does not have a pull−up or pull−down resistor so it should not be left floating.

Primary Charger to HPM10 (Receive): The Primary Charger can use voltage modulation of VDDP to transmit data to the HPM10. HPM10 uses edge detection and AC coupling to extract the data easily without a precise amplitude requirement. This helps relax the requirements on the drive signal and the loading of the VDDP line by the Charge Control block. For robust pulse detection, the rise/fall time of the 200 mV modulation should be less than 100 μs.

Battery Monitoring

HPM10 employs two methods of battery monitoring:

1. In Cradle Mode, the high−precision 10 bit ADC continuously measures voltage and current to the battery.
2. In Hearing Aid Mode, the system uses instantaneous voltage to analog comparators to perform simple detection of battery chemistry. Refer to the Hearing Aid Mode section on page 19 for more information.

Figure 5 illustrates how the battery monitoring is done in a hearing aid system using HPM10.

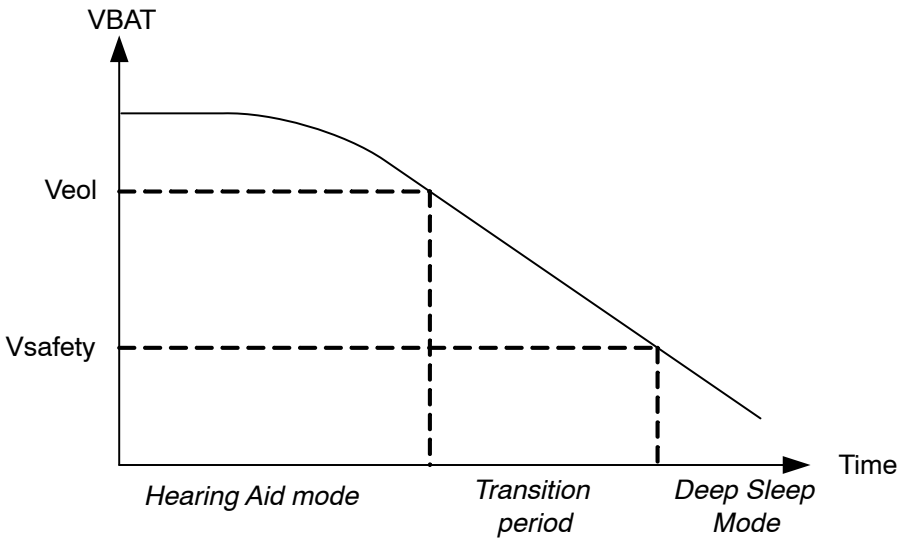


Figure 5. Battery Monitoring for Battery End of Life (EOL)

The hearing aid DSP will have to determine its Veol threshold, and detect when the VBAT reaches this level. From this point, the hearing aid DSP will have to manage its battery EOL procedure (playing a beep users hear, managing datalogging, etc.) before its toggles the DS_EN pin.

If the DS_EN pin hasn’t been toggled by the hearing aid DSP and if the hearing aid DSP keeps on drawing power from the battery, HPM10 will preserve the rechargeable battery from over−discharging by forcing Deep Sleep Mode when VBAT reaches Vsafety. In this mode, the VHA supply is stopped (*SAFE_MODE* status bit = 0). Vsafety is 2.8 V for Li−Ion and 1.0 V for AgZn.

Battery Charging Control

While in Cradle Mode, HPM10 controls the charging of the attached battery. The charging cycle is different for each battery type, with the charging phase transition points for each chemistry (voltage, current temperature and time) stored in OTP and available to the micro−controller in Cradle mode.

The chemistries that are supported by HPM10 are Silver−Zinc (AgZn) and Lithium−Ion (Li−ion). While Zinc−Air (ZnAir) and Nickel−Metal Hydride (Ni−MH) batteries are detected, they are not charged.

As shown in Figure 6, a charger state machine operates in five phases to manage the charging process:

- Start−up (**SU**):
  - Battery type detection
  - OTP boot and CRC checking
- Initialization (**INIT**):
  - Li−ion pre−charge (trickle)
  - Li−ion advanced charging algorithms
  - Over−discharge recovery for AgZn.
- Phase 1 (**PH1**):
  - Li−Ion: Maintain a constant current and monitor the voltage.
  - AgZn: Lower plateau (Ag_2O) and transition zone charging region
  - Exit if the voltage set point has been reached or time−out has occurred.
- Phase 2 (**PH2**):
  - Li−Ion: Maintain a constant voltage and monitor the current.
  - AgZn: Upper plateau (AgO) charging region
  - Exit if the current set point has been reached or time−out has occurred.
- Completion (**CMPLT**): Battery charging process is stopped. Any faults that occurred are stored and communicated to the external charger.

If ZnAir or Ni−MH is detected, then the state machine moves to completion phase.

The control loop for controlling the current and voltage for the charging process consists of monitoring both current and voltage with the ADC and controlling the current supplied with a 10−bit current DAC.

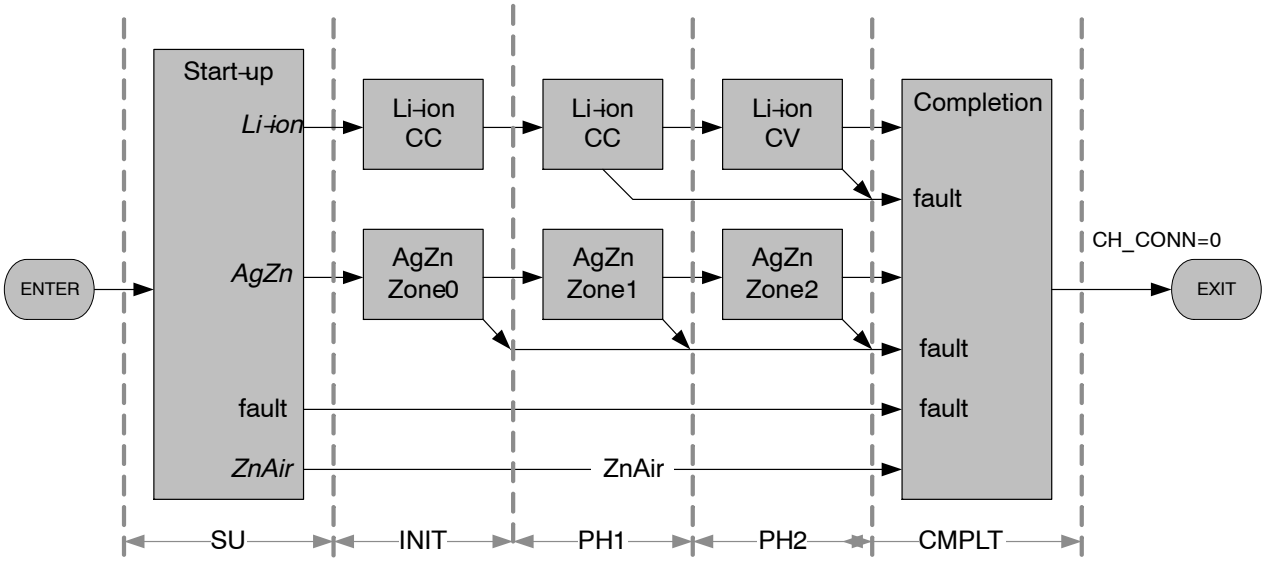


Figure 6. Charging Algorithm Diagram Flow

Clocking

HPM10 has two clock sources:

- In Cradle Mode, the CM_CLK clock is coming from an internal RC oscillator. This clock controls the charging process (timing and state machine), since an accurate time reference is required during this state. This clock is used only in Cradle Mode.
- In Hearing Aid Mode, the HA_CLK is either selected from either an internal RC oscillator or a divided down version of an external clock signal, EXT_CLK. The external clock selection is automatic. If a clock is detected on EXT_CLK it will override the internal oscillator. The motivation for this selection is to have a single clock in the combined system, to avoid pollution on the supplies that will feed into the audio path. When the external clock is used, it must be divided down so the resultant frequency is in the same frequency range as the internal clock (i.e. 64 kHz −2/+95%. The division ratios that are possible are divided by 2, 4, 8, 16, 32, 64, 128 and 256 (3 bits). The hearing aid manufacturer is responsible for setting the appropriate ratio using the CLKDIV[2:0] pins in order to use an external clock pin. This can be done from the DSP or can be connected on the printed circuit board. This clock is used only in Hearing Aid Mode, and in OTP burn mode (ATST_EN=VDDIO).

There is no clock active during the Deep Sleep Mode.

Supply Management

There are several forms of supply management on HPM10:

- **Battery Charge Control:** This block provides either a constant current or constant voltage to the attached battery. Both the current and voltage levels are programmable when in their respective phases.

- **Step−Down Charge Pump:** A high efficiency charge pump, generating a voltage equal to 1/3 of the battery voltage is used for Li−Ion batteries. It supplies directly to the hearing aid chip as the main power supply. The output impedance of the charge pump is low (less than 10 ohms).
- **Digital Voltage Regulator:** This block provides the supply voltage to the digital logic, low voltage band−gaps, oscillator, I/V sense, and ADC when in Charge Mode
- **Hearing Aid Mode Voltage Regulator:** This block provides the supply voltage to all the analog blocks when in Hearing Aid Mode.
- **Digital Interfaces**
  - The digital inputs and outputs SDA, SCL and CCIF are powered from the VDDIO supply pin, which can be connected to DVREG or another available supply. VDDIO is not used in Hearing Aid mode. When the I^2C interface is used for debugging, it is preferable that VDDIO is powered externally to minimize measurement errors.
  - The digital inputs and outputs SWOUT, DS_EN, EXT_CLK, CLKDIV[2:0], AGZN_REG_EN and WARN are powered from the VHA.
- **Voltage References:** There are two bandgap voltage references on the chip. One is a precision bandgap used to generate the high−precision voltage references needed for charging. It also generates other references for the ADC, OSC, and current reference. A 1 V low resolution bandgap is used in Hearing Aid Mode for wakeup and Veol comparators.

General Purpose Analog−to−Digital Converter (ADC)

The general purpose ADC with input mux will allow the state machine to properly manage the charging algorithm based on analog measurements.

The signals being monitored include:

- Battery voltage (VBAT)
- Charge current
- Internal temperature
- Charger input voltage (VDDP)
- VREF (from BandGap, used to calibrate ADC offset)

Power Domains

The input/output is divided into several independent power domains, each with their own ESD clamping structures to allow flexibility in the allowed voltages that can be present on the pins, shown in Table 7.

Table 7. POWER DOMAIN DESCRIPTIONS

Power Domain	Pins	Description
VDDP	DVREG	Full voltage range
VDDIO	SCL, SDA, CCIF, ATST_EN	All digital input/output used in Cradle Mode
VHA	SWOUT, WARN, DS_EN, EXT_CLK, CLKDIV[2:0], AGZN_REG_EN	All digital input/output used in Hearing Aid mode
VBAT	SWIN, VHA, CP1A, CP1B, Cp2A, CP2B	All voltages derived from VBAT
VDD_OTP		Supports overvoltage for OTP burning
VSS	VSS, VSSA, VSSCP	All grounds are shorted together < 2 ohms

Development Tools

A full suite of comprehensive tools is available to assist developers from the initial concept and technology assessment through to prototyping and product launch.

An Evaluation Board and a Charger Board are available for customers to demonstrate, evaluate, and develop products based on HPM10.

HPM10 Programming Interface: This application is primarily used on the production line. It allows a technician to program HPM10's OTP predetermined register values. A user's manual will describe the product application features.

The communication between the PC and HPM10 will be supported by either the Promira Serial Platform from TotalPhase, Inc. or the Communication Accelerator Adaptor (CAA) from ON Semiconductor. On the PC, the communication box will use a USB interface. On HPM10, the I^2C interface of HPM10 will be used.

Company or Product Inquiries

For more information about ON Semiconductor products or services visit our Web site at http://onsemi.com.

Table 8. HPM10 Pin Arrangement

	1	2	3	4	5
A	SDA	RESERVED	VDDIO	CCIF	VDDP
B	SCL	RESERVED	DS_EN	VSS	DVREG
C		VDD_OTP	CLKDIV[2]	ATST_EN	WARN
D	EXT_CLK	SWOUT	CLKDIV[1]	RESERVED	AGZN_REG_EN
E	VSSA	CLKDIV[0]	CP2B	SWIN	CP1B
F	VHA	VSSCP	CP2A	VBAT	CP1A

Table 9. MISC DIE SPECIFICATION

Subject	Specification
Bump metallization	Lead Free (Sn/Ag/Cu)
Backside coating specification	Adwill LC2850
Backside coating thickness	40 μm ± 3 μm

LQFP 32 Pin List

The HPM10 version used on development boards is packaged in a LQFP package of 32 pins. The following table shows the allocation of the IOs:

Table 10. LQFP PIN LIST

Pin #	Pin Name	I/O	Pin #	Pin Name	I/O
1	SDA	I/O	17	CP1A	O
2	RESERVED	I	18	CP1B	O
3	CCIF	I/O	19	VBAT	Power
4	––		20	CP2A	O
5	ATST_EN	I	21	CP2B	O
6	VSS	Gnd	22	VSSCP	Gnd
7	––		23	VHA	O
8	RESERVED	I/O	24	VSSA	Gnd
9	VDDP	Power	25	EXT_CLK	I
10	DVREG	O	26	CLKDIV[0]	I
11	WARN	O	27	CLKDIV[1]	I
12	AGZN_REG_EN	I	28	CLKDIV[2]	I
13	SWIN	I	29	VDD_OTP	Power
14	DS_EN	I	30	VDDIO	Power
15	SWOUT	O	31	RESERVED	I/O
16	––		32	SCL	I/O

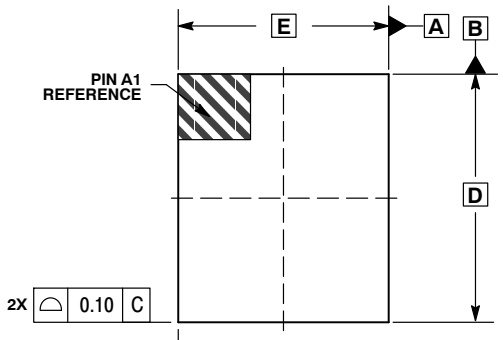
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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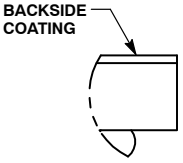
WLCSP29 2.05x1.74
CASE 567MK
ISSUE O

SCALE 4:1

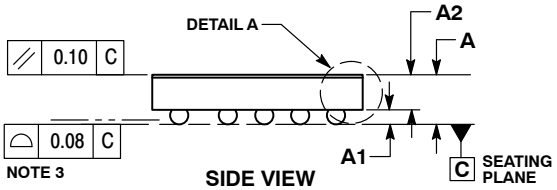
DATE 09 OCT 2015



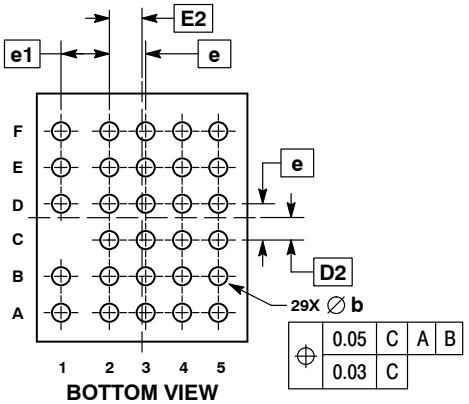
TOP VIEW



DETAIL A



SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.
4. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.46
A1	0.09	0.15
A2	0.29 REF	
b	0.12	0.18
D	2.05 BSC	
D2	0.185 BSC	
E	1.74 BSC	
E2	0.27 BSC	
e	0.30 BSC	
e1	0.40 BSC	

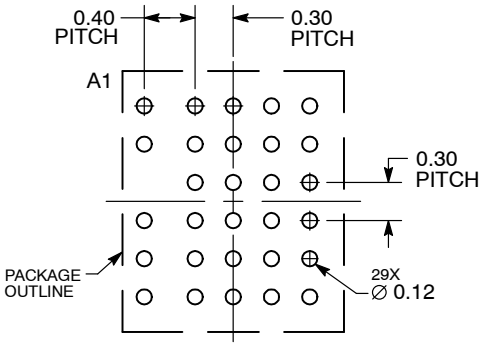
GENERIC MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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