HMP8115

April 1998

NTSC/PAL Video Decoder

Features

- **(M) NTSC and (B, D, G, H, I, M, N, N_C) PAL Operation**
  - **Optional Auto Detect of Video Standard**
  - **ITU-R BT.601 (CCIR601) and Square Pixel Operation**
- **Digital Output Formats**
  - **VMI Compatible**
    - **8-Bit, 16-Bit 4:2:2 YCbCr**
    - **15-Bit (5,5,5), 16-Bit (5,6,5) RGB**
      - **Linear or Gamma-Corrected**
  - **8-Bit BT.656**
- **Analog Input Formats**
  - **Three Analog Composite Inputs**
  - **Analog Y/C (S-Video) Input**
- **"Sliced" VBI Data Capture Capabilities**
  - **Closed Captioning**
  - **Widescreen Signalling (WSS)**
  - **BT.653 System B, C and D Teletext**
    - **NABTS (North American Broadcast Teletext)**
    - **WST (World System Teletext)**
- **2-Line (1H) Comb Filter Y/C Separator**
- **Fast I^2C Interface**
- **Two 8-Bit ADCs**

Applications

- **Multimedia PCs**
- **Video Conferencing**
- **Video Compression Systems**
- **Video Security Systems**
- **LCD Projectors and Overhead Panels**
- **Related Products**
  - **NTSC/PAL Encoders: HMP815x, HMP817x**
  - **NTSC/PAL Decoders: HMP8112A**
- **Related Literature**
  - **AN9644: Composite Video Separation Techniques**
  - **AN9716: Widescreen Signalling**
  - **AN9717: YCbCr to RGB Considerations**
  - **AN9728: BT.656 Video Interface for ICs**
  - **AN9738: VMI Video Interface for ICs**

Description

The HMP8115 is a high quality NTSC and PAL decoder with internal A/D converters. It is compatible with NTSC M, PAL B, D, G, H, I, M, N, and combination N (N_C) video standards.

Both composite and S-video (Y/C) input formats are supported. A 2-line comb filter plus a user-selectable chrominance trap filter provide high quality Y/C separation. User adjustments include brightness, contrast, saturation, hue, and sharpness.

Data during the vertical blanking interval (VBI), such as closed captioning, widescreen signalling and teletext, may be captured and output as BT.656 ancillary data. Closed captioning and widescreen signalling information may also be read out via the I^2C interface.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HMP8115CN	0 to 70	80 Ld PQFP	Q80.14x20
HMPVIDEVAL/ISA	Evaluation Board: ISA Frame Grabber		

NOTES:

1. PQFP is also known as QFP and MQFP.
2. Evaluation Board and Reference Design descriptions are in the Applications section.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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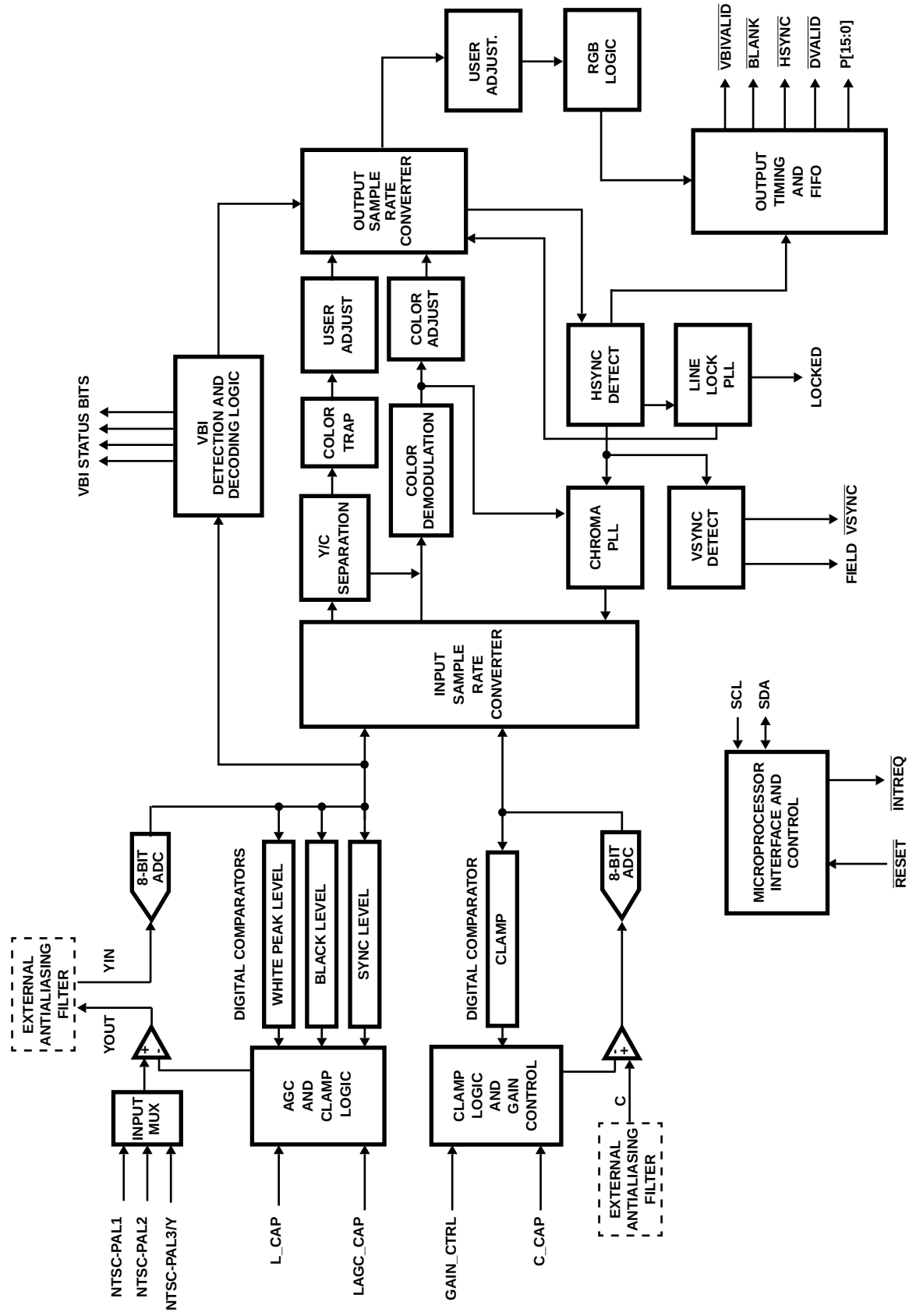
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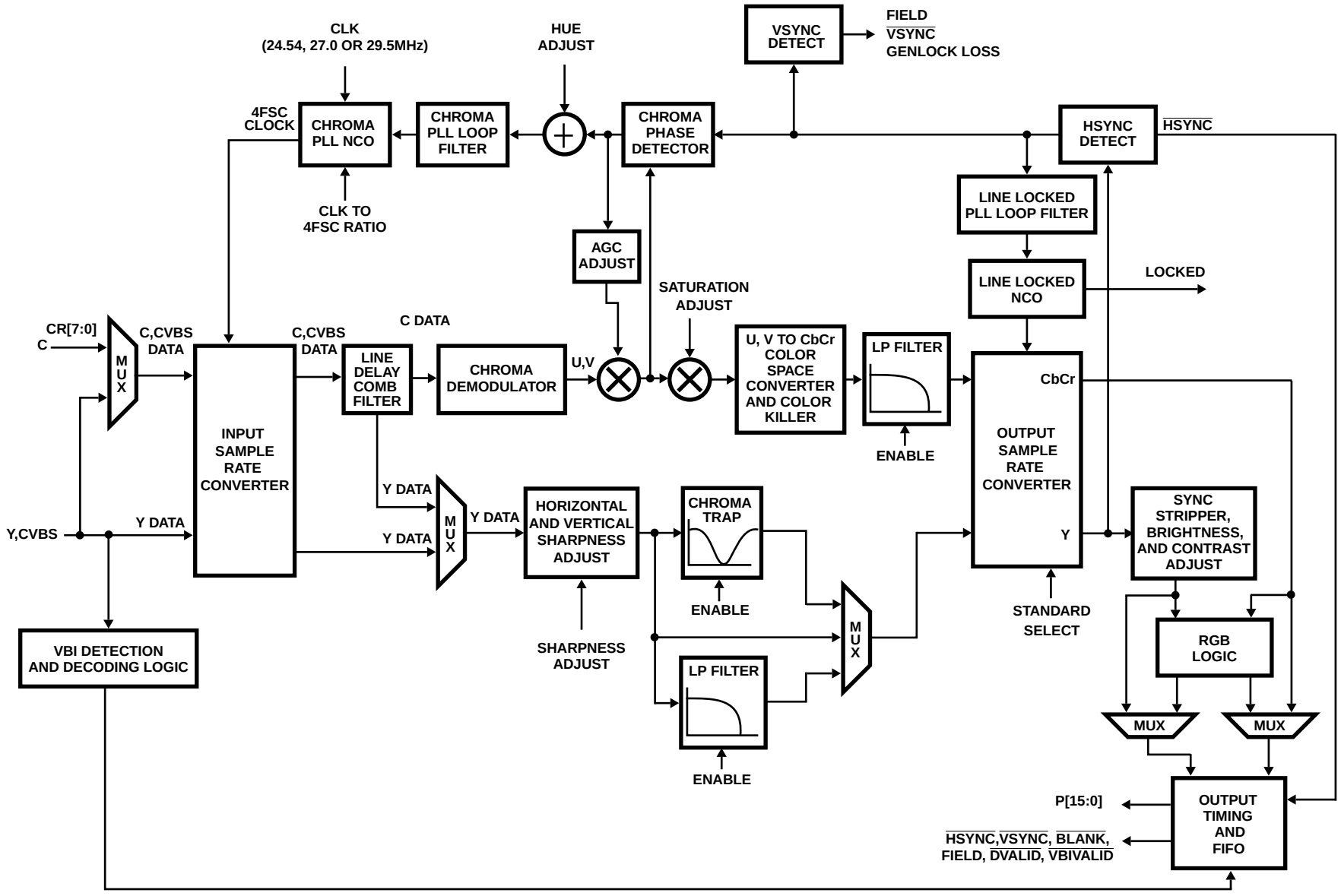
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Functional Block Diagram (Continued)



Introduction

The HMP8115 is designed to decode baseband composite or S-video NTSC and PAL signals, and convert them to either digital YCbCr or RGB data. In addition to performing the basic decoding operations, the HMP8115 includes hardware to decode different types of VBI data and to generate digital video patterns for a blue screen, black screen and full screen color bars.

The digital PLLs are designed to synchronize to all NTSC and PAL standards. A chroma PLL is used to maintain chroma lock for demodulation of the color information; a line-locked PLL is used to maintain vertical spatial alignment. The PLLs are designed to maintain lock even in the event of VCR headswitches and multipath noise.

The HMP8115 contains two 8-bit A/D converters and an I^2C interface for programming internal registers.

External Video Processing

Before a video signal can be digitized the decoder has some external processing considerations that need to be addressed. This section discusses those external aspects of the HMP8115.

ANALOG VIDEO INPUTS

The HMP8115 supports either three composite or two composite and one S-video input.

Three analog video inputs (NTSC/PAL 1-3) are used to select which one of three composite video sources are to be decoded. To support S-video applications, the Y channel drives the NTSC/PAL 3 analog input, and the C channel drives the C analog input.

The analog inputs must be AC-coupled to the video signals, as shown in the Applications section.

ANTI-ALIASING FILTERS

An external anti-alias filter is required to achieve optimum performance and prevent high frequency components from being aliased back into the video image.

For the NTSC/PAL 1-3 inputs, a single filter is connected between the YOUT and YIN pins. For the C input, the anti-aliasing filter should be connected before the C input. A recommended filter is shown in Figure 1.

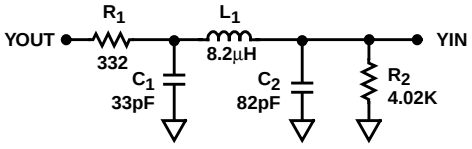


FIGURE 1. RECOMMENDED ANTI-ALIASING FILTER

S-VIDEO CHROMA GAIN CONTROL

The Chroma portion of S-video is AC coupled through an anti-aliasing filter as shown in the applications section. Unlike the composite/luma inputs, the Automatic Gain Control (AGC) for the chroma portion of S-video is done digitally inside the decoder as determined by bits 7 and 6 of the COLOR PROCESSING register 06_H. In addition to the internal AGC, the designer can also apply some gain to the chroma before it reaches the internal AGC logic. This gain is controlled by pin 28. The voltage at this pin determines the gain of the chroma before it gets digitized by the chroma A/D with a typical gain performance as shown in Figure 2.

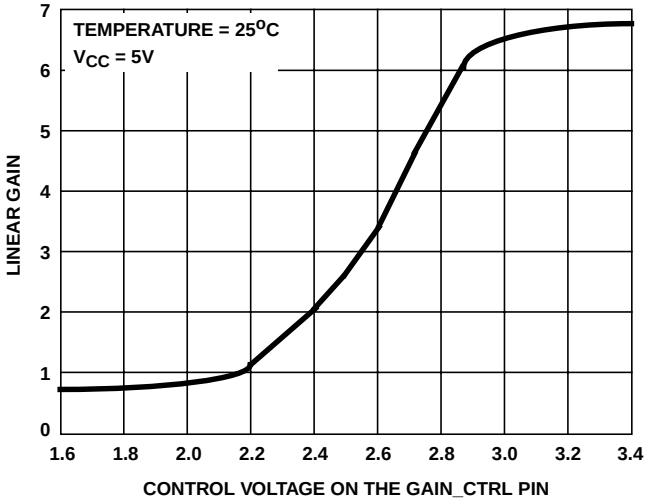


FIGURE 2. CHROMINANCE AMPLIFIER GAIN

Digitization of Video

Prior to A/D conversion, the video signal is DC restored and gained to generate known video levels into the digital processing logic. This process is addressed in the “AGC and DC Restoration” section. After digitization, sample rate converters and a comb filter are used to perform color separation and demodulation.

A/D CONVERSION

Video data is sampled at the CLK2 frequency then processed by the input sample rate converter. The output levels of the ADC after AGC processing are:

	(M) NTSC (M, N) PAL	(B, D, G, H, I, N_C) PAL
white	224	213
black	76	64
blank	64	64
sync	0	0

AGC AND DC RESTORATION

The AGC amplifier attenuates or amplifies the analog video signal to ensure that the sync tip level generates code 0. The difference from the ideal sync tip level of 0 is used to control the amount of attenuation or gain of the analog video signal. The capacitor on the LAGC_CAP pin is used to store the voltage which sets the gain level of the input video amplifier.

DC restoration positions the video signal such that the DC level of the back porch generates an average code 64. The back porch is sampled to determine the average value. The capacitor on the L_CAP pin is used to store the voltage

which sets the DC offset level into the input video amplifier. During the S-video mode of operation the capacitor on the C_CAP pin performs the same function as the L_CAP capacitor, except the chroma video amplifier's DC offset is set so that the chroma A/D generates a code of 128 during the back porch. The internal timing windows for AGC and DC Restoration are show in Figure 3.

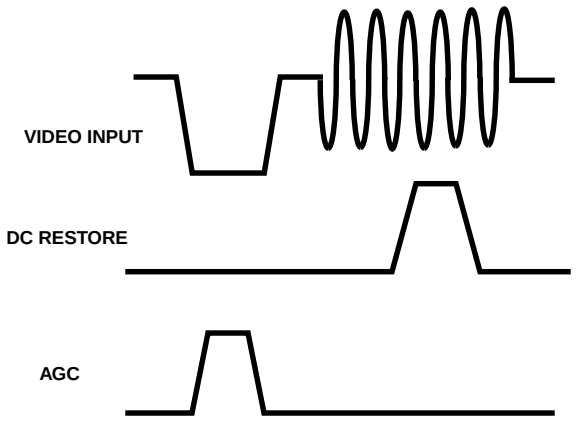


FIGURE 3. AGC AND DC RESTORE INTERNAL TIMING

INPUT SIGNAL DETECTION

It is assumed there is no video input if a horizontal sync is not detected for 16 consecutive lines. When no video has been detected, nominal video timing is generated for the previously detected or programmed standard. A maskable interrupt is included to flag when no video has been detected (bit 6 of the INTERRUPT MASK register $0F_H$) allowing for blue/black/color bar output modes to be enabled if desired. The vertical sync interrupt can be used in determining when a video signal is present at the currently selected video mux input. Bit 0 of register $0F_H$ is used to enable vertical sync interrupts.

VERTICAL SYNC AND FIELD DETECTION

The vertical sync and field detect circuit uses a low time counter to detect the vertical sync sequence in the video data stream. The low time counter accumulates the low time encountered during any sync pulse, including serration and equalization pulses. When the low time count exceeds the vertical sync detect threshold, $\overline{VSYNC}$ is asserted immediately. FIELD is asserted at the same time that $\overline{VSYNC}$ is asserted. FIELD is asserted low for odd fields and high for even fields. Field is determined from the location in the video line where VSYNC is detected. If VSYNC is detected in the first half of the line, the field is odd. If VSYNC is detected in the second half of a line, the field is even.

In the case of lost vertical sync or excessive noise that would prevent the detection of vertical sync, the FIELD output will continue to toggle. Lost vertical sync is declared if after 337 lines, a vertical sync period was not detected for 1 or 3 (selectable) successive fields as specified by bit 2 of the GENLOCK CONTROL register 04_H. When this occurs, the PLLs are initialized to the acquisition state.

Y/C SEPARATION

A composite video signal has the luma (Y) and chroma (C) information mixed in the same video signal. The Y/C separation process is responsible for separating the composite video signal into these two components. The HMP8115 utilizes a comb filter to minimize the artifacts that are associated with the Y/C separation process.

INPUT SAMPLE RATE CONVERTER

The input sample rate converter is used to convert video data sampled at the CLK2 rate to a virtual $4xf_{SC}$ sample rate for comb filtering and color demodulation. An interpolating filter is used to generate the $4xf_{SC}$ samples as illustrated in Figure 4.

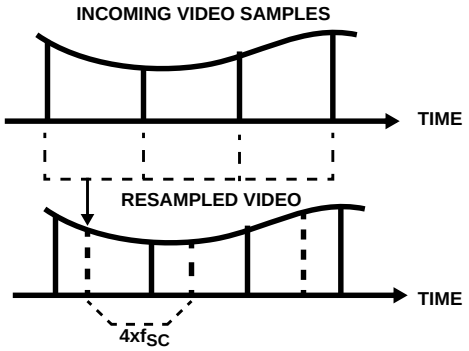


FIGURE 4. SAMPLE RATE CONVERSION

COMB FILTER

A 2-line comb filter, using a single line delay, is used to perform part of the Y/C separation process. During S-video operation, the Y signal bypasses the comb filter; the C signal is processed by the comb filter since it is an integral part of the chroma demodulator. During PAL operation, the chroma trap filter should also be enabled for improved performance.

Since a single line store is used, the chroma will normally have a half-line vertical offset from the luma data. This may be eliminated, vertically aligning the chroma and luma samples, at the expense of vertical resolution of the luma. Bit 0 of the OUTPUT FORMAT register 02_H controls this option.

CHROMA DEMODULATION

The output of the comb filter is further processed using a patented frequency domain transform to complete the Y/C separation and demodulate the chromanance.

Demodulation is done at a virtual $4xf_{SC}$ sample rate using the interpolated data samples to generate U and V data. The demodulation process decimates by 2 the U/V sample rate.

OUTPUT SAMPLE RATE CONVERTER

The output sample rate converter converts the Y, U and V data from a virtual $4xf_{SC}$ sample rate to the desired output sample rate (i.e., 13.5MHz). It also vertically aligns the samples based on the horizontal sync information embedded in the digital video data stream. The output sample rate is determined by the selected video standard and whether

square or rectangular pixels are output. The output format is 4:2:2 for all modes except the RGB modes which use a 4:4:4 output format.

CLK2 INPUT

Note that the color subcarrier is derived from CLK2. Any jitter on CLK2 will be transferred to the color subcarrier, resulting in color changes. Thus, CLK2 should be derived from a stable clock source, such as a crystal. The use of a PLL to generate CLK2 is not recommended. CLK2 must have a 50ppm accuracy and at least a 60/40% duty cycle to ensure proper operation.

The CLK2 clock rate must be one of the following frequencies:

24.54MHz
27.00MHz
29.50MHz

The frequency of CLK2 must be 2x the desired output sample rate. The values in Table 1 below indicate the CLK2 clock rate based on the video standard and pixel mode. The output sample rate for the given video standard and pixel mode is half the CLK2 clock rate.

TABLE 1. VIDEO STANDARD CLOCK RATE SELECTION SUMMARY

VIDEO FORMAT	ALLOWABLE CLK2 FREQUENCIES (MHz)	
	RECTANGULAR PIXEL MODE	SQUARE PIXEL MODE
(M) NTSC	27.00	24.54
(B, D, G, H, I, N) PAL	27.00	29.50
(M) PAL	27.00	24.54
(N_C) PAL	27.00	29.50

Digital Processing of Video

Once the luma and chroma have been separated the HMP8115 then performs programmable modifications (i.e. contrast, coring, color space conversions, color AGC, etc.) to the decoded video signal.

UV TO CbCr CONVERSION

The baseband U and V signals are scaled and offset to generate a nominal range of 16-240 for both the Cb and Cr data.

DIGITAL COLOR GAIN CONTROL

There are four types of color gain control modes available: no gain control, automatic gain control, fixed gain control, and freeze automatic gain control.

If “no gain control” is selected, the amplitude of the color difference signals (CbCr) is not modified, regardless of variations in the color burst amplitude. Thus, a gain of 1x is always used for Cb and Cr.

If “automatic gain control” is selected, the amplitude of the color difference signals (CbCr) is compensated for variations in the color burst amplitude. The burst amplitude is averaged with the two previous lines having a color burst to limit line-to-line variations. A gain of 0.5x to 4x is used for Cb and Cr.

If “fixed gain control” is selected, the amplitude of the color difference signals (CbCr) is multiplied by a constant, regardless of variations in the color burst amplitude. The constant gain value is specified by the COLOR GAIN register $1C_H$. A gain of 0.5x to 4x is used for Cb and Cr. Limiting the gain to 4x limits the amount of amplified noise.

If “freeze automatic gain control” is selected, the amplitude of the color difference signals (CbCr) is multiplied by a constant. This constant is the value the AGC circuitry generated when the “freeze automatic gain” command was selected.

COLOR KILLER

If “enable color killer” is selected, the color output is turned off when the running average of the color burst amplitude is below approximately 25% of nominal for four consecutive fields. When the running average of the color burst amplitude is above approximately 25% of nominal for four consecutive fields, the color output is turned on. The color output is also turned off when excessive phase error of the chroma PLL is present.

If “force color off” is selected, color information is never present on the outputs.

If “force color on” is selected, color information is present on the outputs regardless of the color burst amplitude or chroma PLL phase error.

Y PROCESSING

The black level is subtracted from the luminance data to remove sync and any blanking pedestal information. Negative values of Y are supported at this point to allow proper decoding of “below black” luminance levels.

Scaling is done to position black at 8-bit code 0 and white at 8-bit code 219.

A chroma trap filter may be used to remove any residual color subcarrier from the luminance data. The center frequency of the chroma trap is automatically determined from the video standard being decoded. The chroma trap should be disabled during S-video operation to maintain maximum luminance bandwidth. Alternately, a 3MHz lowpass filter may be used to remove high-frequency Y data. This may make a noisy image more pleasing to the user, although softer.

Coring of the high-frequency Y data may be done to reduce low-level high frequency noise.

Coring of the Y data may also be done to reduce low-level noise around black. This forces Y data with the following values to a value of 0:

coring = 1: $\pm$ 1
coring = 2: $\pm$ 1, $\pm$ 2
coring = 3: $\pm$ 1, $\pm$ 2. $\pm$ 3

High-frequency components of the luminance signal may be “peaked” to control the sharpness of the image. Maximum gain may be selected to occur at either 2.6MHz or the color

subcarrier frequency. This may be used to make the displayed image more pleasing to the user. It should not be used if the output video will be compressed, as the circuit introduces high-frequency components that will reduce the compression ratio.

The brightness control adds or subtracts a user-specified DC offset to the Y data. The contrast control multiplies the Y data by a user-specified amount. These may be used to make the displayed image more pleasing to the user.

Finally, a value of 16 is added to generate a nominal range of 16 (black) to 235 (white).

CbCr PROCESSING

The CbCr data is lowpass filtered to either 0.85 or 1.5MHz.

Coring of the CbCr data may be done to reduce low-level noise around zero. This forces CbCr data with the following values to a value of 128.

coring = 1: 127, 129
coring = 2: 126, 127, 129, 130
coring = 3: 125, 126, 127, 129, 130, 131

The saturation control multiplies the CbCr data by a user-specified amount. This may be used to make the displayed image more pleasing to the user. The CbCr data may also be optionally multiplied by the contrast value to avoid color shifts when changing contrast.

The hue control provides a user-specified phase offset to the color subcarrier during decoding. This may be used to correct slight hue errors due to transmission.

YCbCr OUTPUT FORMAT PROCESSING

Y has a nominal range of 16 to 235. Cb and Cr have a nominal range of 16 to 240, with 128 corresponding to zero. Values less than 1 are made 1 and values greater than 254 are made 254.

While $\overline{\text{BLANK}}$ is asserted, Y is forced to have a value of 16, with Cb and Cr forced to have a value of 128, unless VBI data is present.

RGB OUTPUT FORMAT PROCESSING

The 4:2:2 YCbCr data is converted to 4:4:4 YCbCr data and then converted to either 15-bit or 16-bit gamma-corrected RGB (R′G′B′) data. While $\overline{\text{BLANK}}$ is asserted, RGB data is forced to a value of 0.

15-Bit R′G′B′

The following YCbCr to R′G′B′ equations are used to maintain the proper black and white levels:

R′ = 0.142(Y - 16) + 0.194(Cr - 128)
G′ = 0.142(Y - 16) - 0.099(Cr - 128) - 0.048(Cb - 128)
B′ = 0.142(Y - 16) + 0.245(Cb - 128)

The resulting 15-bit R′G′B′ data has a range of 0 to 31. Values less than 0 are made 0 and values greater than 31 are made 31.

The 15-bit R′G′B′ data may be converted to 15-bit linear RGB, using the following equations. Although the PAL specifications specify a gamma of 2.8, a gamma of 2.2 is normally used. The HMP8115 allows the selection of the gamma to be either 2.2 or 2.8, independent of the video standard.

for gamma = 2.2:

for R′G′B′ < 0.0812*31

$R = (31)((R'/31)/4.5)$
$G = (31)((G'/31)/4.5)$
$B = (31)((B'/31)/4.5)$

for R′G′B′ >= 0.0812*31

$R = (31)(((R'/31) + 0.099)/1.099)^{2.2}$
$G = (31)(((G'/31) + 0.099)/1.099)^{2.2}$
$B = (31)(((B'/31) + 0.099)/1.099)^{2.2}$

for gamma = 2.8:

$R = (31)(R'/31)^{2.8}$
$G = (31)(G'/31)^{2.8}$
$B = (31)(B'/31)^{2.8}$

16-Bit R′G′B′

The following YCbCr to R′G′B′ equations are used to maintain the proper black and white levels:

R′ = 0.142(Y - 16) + 0.194(Cr - 128)
G′ = 0.288(Y - 16) - 0.201(Cr - 128) - 0.097(Cb - 128)
B′ = 0.142(Y - 16) + 0.245(Cb - 128)

The resulting 16-bit R′G′B′ data has a range of 0 to 31 for R′ and B′, and a range of 0 to 63 for G′. Values less than 0 are made 0; R′ and B′ values greater than 31 are made 31, G′ values greater than 63 are made 63.

The 16-bit R′G′B′ data may be converted to 16-bit linear RGB, using the following equations. Although the PAL specifications specify a gamma of 2.8, a gamma of 2.2 is normally used. The HMP8115 allows the selection of the gamma to be either 2.2 or 2.8, independent of the video standard.

for gamma = 2.2:

for R′B′ < 0.0812*31, G′ < 0.0812*63

$R = (31)((R'/31)/4.5)$
$G = (63)((G'/63)/4.5)$
$B = (31)((B'/31)/4.5)$

for R′B′ >= 0.0812*31, G′ >= 0.0812*63

$R = (31)(((R'/31) + 0.099)/1.099)^{2.2}$
$G = (63)(((G'/63) + 0.099)/1.099)^{2.2}$
$B = (31)(((B'/31) + 0.099)/1.099)^{2.2}$

for gamma = 2.8:

$R = (31)(R'/31)^{2.8}$
$G = (63)(G'/63)^{2.8}$
$B = (31)(B'/31)^{2.8}$

BUILT-IN VIDEO GENERATION

When the blue screen, black screen or color bar output is selected, a full-screen of blue, black or 75% colorbar output is generated using the currently selected output format. The type of screen to be generated is determined by bits 2 and 1 of the OUTPUT FORMAT register 02_H. When built-in video generation is not desired, the bits need to be set for normal operation to pass decoded video.

If a video source is input, it will be used to provide the video timing. If an input video source is not detected, internally-generated video timing will be used.

Pixel Port Timing

The the timing and format of the output data and control signals is presented in the following sections.

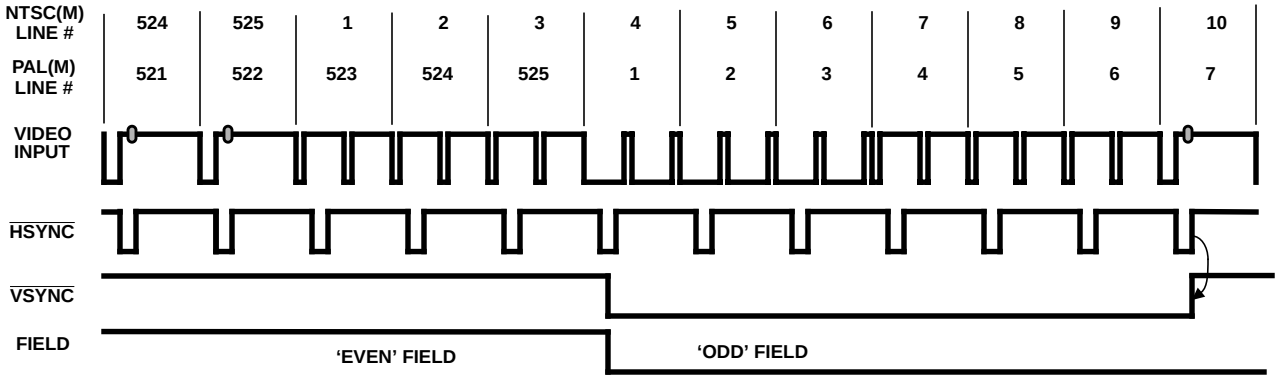
$\overline{\text{HSYNC}}$ AND $\overline{\text{VSYNC}}$ TIMING

The $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ output timing is VMI v1.4 compatible. Figures 5-8 illustrate the video timing. The leading edge of HSYNC is synchronous to the video input signal and has a fixed latency due to internal pipeline processing. The pulse width of the $\overline{\text{HSYNC}}$ is defined by the END HSYNC register 36H, where the trailing edge of $\overline{\text{HSYNC}}$ has a programmable delay of 0-510 CLK2 cycles from the leading edge.

The leading edge of $\overline{\text{VSYNC}}$ is asserted approximately half way through the first serration pulse of each field. For an odd field, the trailing edge of $\overline{\text{VSYNC}}$ is 5±1 CLK2 cycles after the trailing edge of the $\overline{\text{HSYNC}}$ that follows the last equalization pulse. Refer to Figures 5 and 7. For an even field, the trailing edge of $\overline{\text{VSYNC}}$ is 5±1 CLK2 cycles leading the leading edge of the $\overline{\text{HSYNC}}$ that follows the last equalization pulse. Refer to Figures 6 and 8.

FIELD TIMING

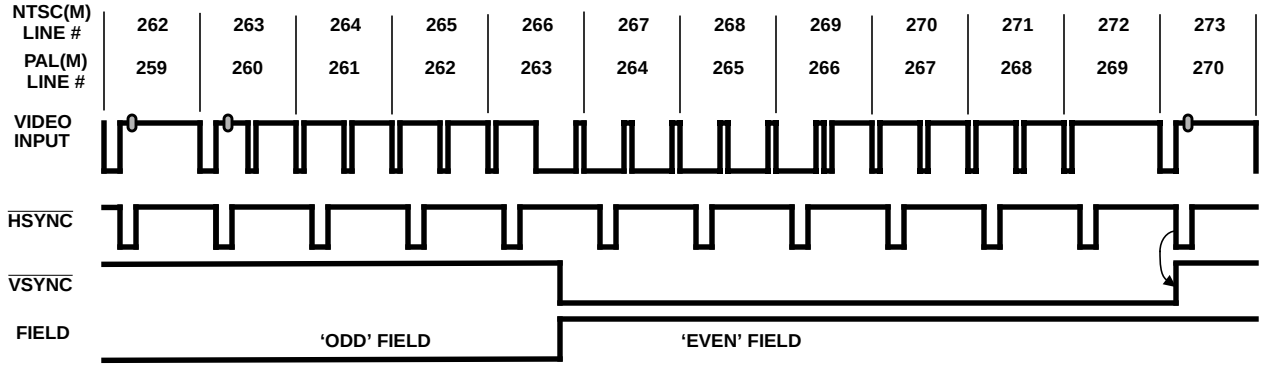
When field information can be determined from the input video source, the FIELD output pin reflects the video source field state. When field information cannot be determined from the input video source, the FIELD output pin alternates its state at the beginning of each field. FIELD changes state 5±1 CLK2 cycles before the leading edge of $\overline{\text{VSYNC}}$.



NOTE:

3. The trailing edge of $\overline{\text{VSYNC}}$ is 5±1 clocks after the trailing edge of $\overline{\text{HSYNC}}$ to be VMI compatible and to indicate a transition to an odd field.

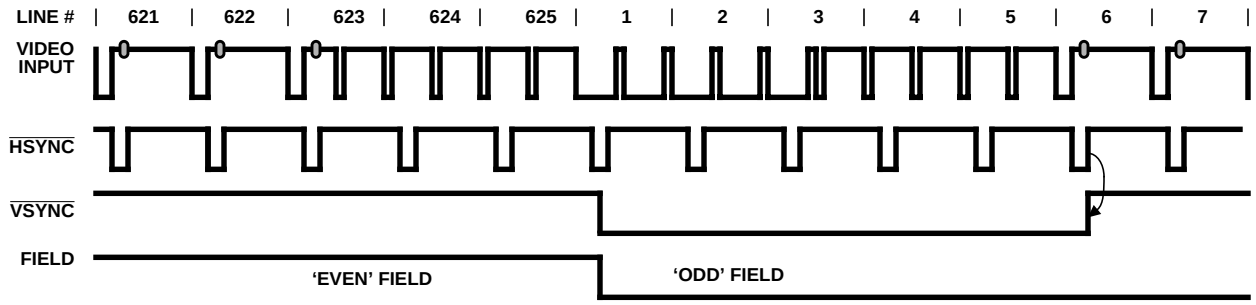
FIGURE 5. NTSC(M) AND PAL(M) $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ AND FIELD TIMING DURING AN EVEN TO ODD FIELD TRANSITION



NOTE:

4. The trailing edge of $\overline{\text{VSYNC}}$ is 5±1 clocks after the leading edge of $\overline{\text{HSYNC}}$ to be VMI compatible and to indicate a transition to an even field.

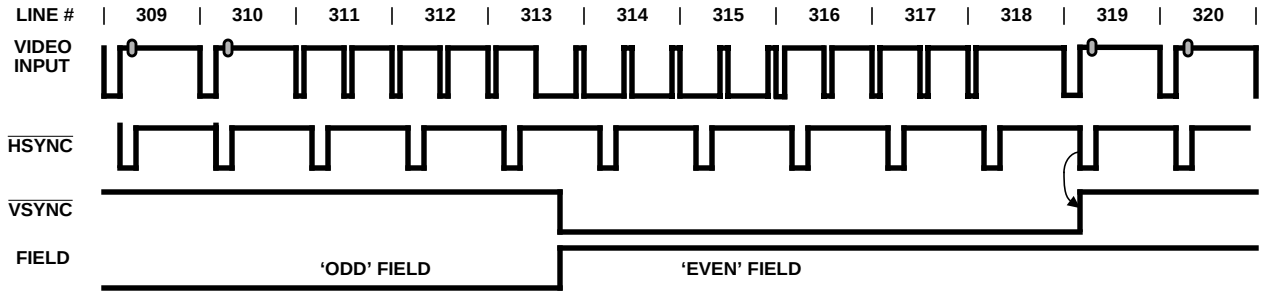
FIGURE 6. NTSC(M) AND PAL(M) $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ AND FIELD TIMING DURING AN ODD TO EVEN FIELD TRANSITION



NOTE:

5. The trailing edge of $\overline{\text{VSYNC}}$ is 5±1 clocks after the trailing edge of $\overline{\text{HSYNC}}$ is to be VMI compatible and to indicate a transition to an odd field.

FIGURE 7. PAL(B,D,G,H,I,N,N_C) HSYNC, VSYNC AND FIELD TIMING DURING AN EVEN TO ODD FIELD TRANSITION



NOTE:

6. The trailing edge of $\overline{\text{VSYNC}}$ is 5±1 clocks after the leading edge of $\overline{\text{HSYNC}}$ to be VMI compatible and to indicate a transition to an even field.

FIGURE 8. PAL(B,D,G,H,I,N,N_C) HSYNC, VSYNC AND FIELD TIMING DURING AN ODD TO EVEN FIELD TRANSITION

$\overline{\text{BLANK}}$ AND $\overline{\text{DVALID}}$ TIMING

$\overline{\text{DVALID}}$ is asserted when P15-P0 contain valid data. The timing and behavior of $\overline{\text{DVALID}}$ is dependent on the output video format and the programmed values for bit 4 (DVLD_DCYC) and bit 5 (DVLD_LTC) of the GENLOCK CONTROL register 04_H. Refer to the specific output video format sections that follow for the specific behavior for $\overline{\text{DVALID}}$.

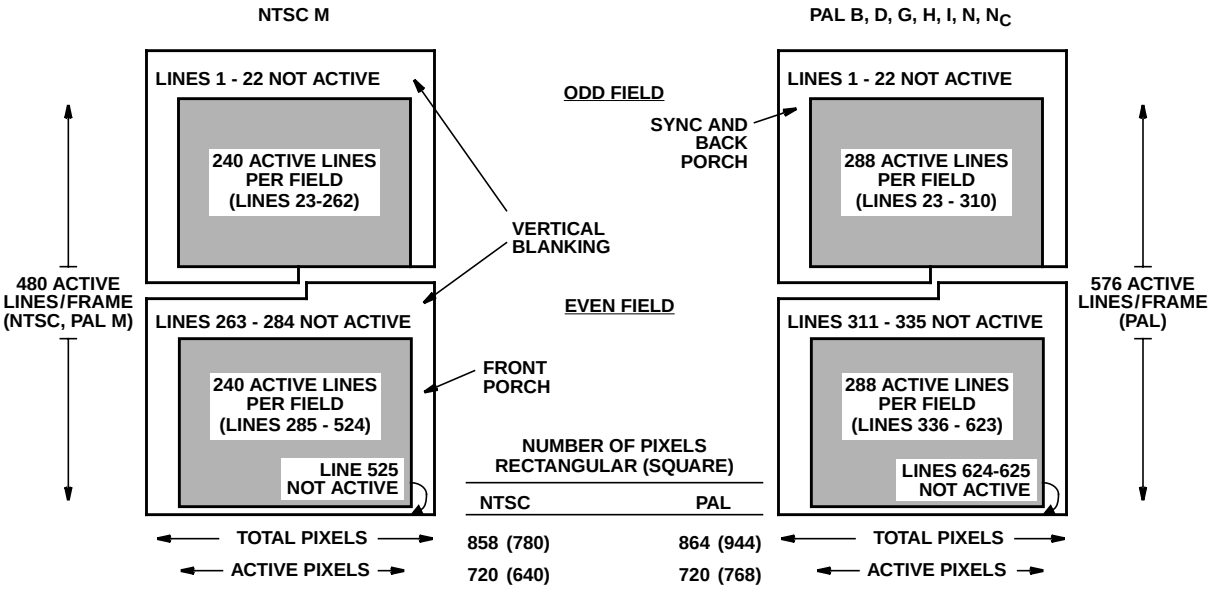
$\overline{\text{BLANK}}$ is used to determine if the HMP8115 is generating active video data. $\overline{\text{BLANK}}$ should be used in conjunction with $\overline{\text{DVALID}}$ to capture digital data from the decoder. $\overline{\text{BLANK}}$, $\overline{\text{DVALID}}$ and the video data are output after the internal pipeline latency and synchronous with the rising edge of CLK2.

During active scan lines $\overline{\text{BLANK}}$ is negated when the horizontal pixel count matches the value in the END H_BLANK register 32_H. A count of 00_H corresponds to the 50% point of the leading edge of the sync tip after leaving the part. $\overline{\text{BLANK}}$ is asserted when the horizontal pixel count matches the value in the START H_BLANK register $31_H/30_H$. Note that horizontally, $\overline{\text{BLANK}}$ is programmable with two pixel resolution.

START V_BLANK register $34_H/33_H$ and END V_BLANK register 35_H determine which scan lines are blanked for each field. During inactive scan lines, $\overline{\text{BLANK}}$ is asserted during the entire scan line. Half-line blanking of the output video cannot be done. Reference Figure 9 for active video timing and use Table 2 for typical blanking programming values.

TABLE 2. TYPICAL VALUES FOR HBLANK AND VBLANK REGISTERS

VIDEO STANDARD (MSB/LSB)	ACTIVE PIXELS/ LINE	TOTAL PIXELS/ LINE	LAST PIXEL COUNT	START H_BLANK (31H/30H)	END H_BLANK (32H)	START V_BLANK (34H/33H)	END V_BLANK (35H)
RECTANGULAR PIXELS							
NTSC (M), PAL (M)	720	858	857 (0359_H)	842 ($034A_H$)	122 ($7A_H$)	259 (0103_H)	19 (13_H)
PAL (B, D, G, H, I,N, N_C)	720	864	863 ($035F_H$)	852 (0354_H)	132 (84_H)	310 (0136_H)	22 (16_H)
SQUARE PIXELS							
NTSC (M), PAL (M)	640	780	779 ($030B_H$)	758 ($02F6_H$)	118 (76_H)	259 (0103_H)	19 (13_H)
PAL (B, D, G, H, I,N, N_C)	768	944	943 ($03AF_H$)	922 ($039A_H$)	154 ($9A_H$)	310 (0136_H)	22 (16_H)



NOTE:

7. The line numbering for PAL (M) followings NTSC (M) line count minus 3 per the video standards.

FIGURE 9. TYPICAL ACTIVE VIDEO REGIONS

TABLE 3. PIXEL OUTPUT FORMATS

PIN NAME	8-BIT, 4:2:2, YCbCr	16-BIT, 4:2:2, YCbCr	15-BIT, RGB, (5,5,5)	16-BIT, RGB, (5,6,5)	BT.656
P0	0	Cb0, Cr0	B0	B0	0
P1	0	Cb1, Cr1	B1	B1	0
P2	0	Cb2, Cr2	B2	B2	0
P3	0	Cb3, Cr3	B3	B3	0
P4	0	Cb4, Cr4	B4	B4	0
P5	0	Cb5, Cr5	G0	G0	0
P6	0	Cb6, Cr6	G1	G1	0
P7	0	Cb7, Cr7	G2	G2	0
P8	Y0, Cb0, Cr0	Y0	G3	G3	YCbCr Data, Ancillary Data, SAV and EAV Sequences
P9	Y1, Cb1, Cr1	Y1	G4	G4	
P10	Y2, Cb2, Cr2	Y2	R0	G5	
P11	Y3, Cb3, Cr3	Y3	R1	R0	
P12	Y4, Cb4, Cr4	Y4	R2	R1	
P13	Y5, Cb5, Cr5	Y5	R3	R2	
P14	Y6, Cb6, Cr6	Y6	R4	R3	
P15	Y7, Cb7, Cr7	Y7	0	R4	

PIXEL OUTPUT PORT

Pixel data is output via the P0-P15 pins. Refer to Table 3 for the output pin definition as a function of the output mode.

8-BIT YCbCr OUTPUT

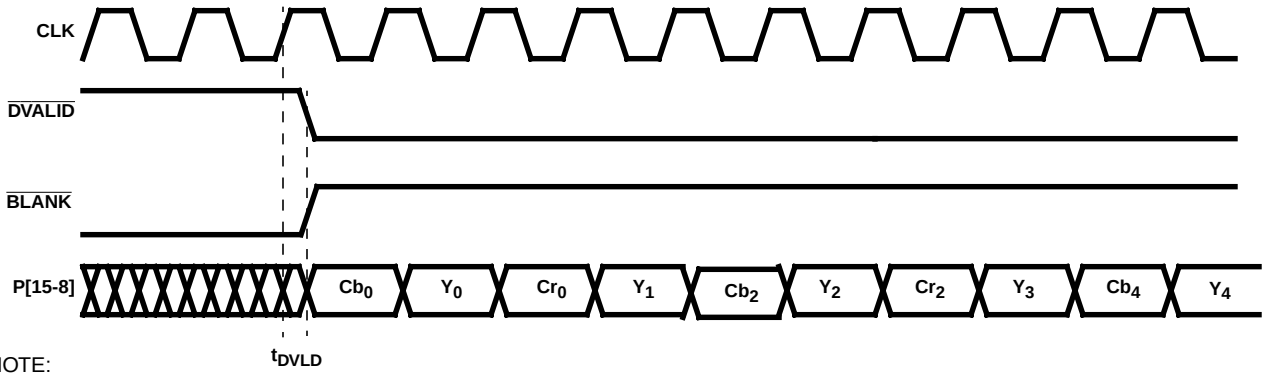
The $\overline{\text{DVALID}}$ output pin may be configured to operate in one of two ways. The configuration is determined by the DVLD_LTC bit (bit 4) of the GENLOCK CONTROL register 04_H.

If DVLD_LTC=0, the $\overline{\text{DVALID}}$ output is continuously asserted during the entire active video time on active scan lines if CLK2 is exactly 2x the desired output sample rate. $\overline{\text{DVALID}}$ being asserted indicates valid pixel data is present on the P15-P8 pixel outputs. $\overline{\text{DVALID}}$ is never asserted during the blanking intervals. Refer to Figure 10.

If DLVD_LTC=1, $\overline{\text{DVALID}}$ has the same internal timing as the first mode, but is ANDed with the CLK2 signal, and the result is output onto the $\overline{\text{DVALID}}$ pin. This results in a gated CLK2 signal being output during the active video time on active scan lines. Refer to Figure 11.

If 8-bit YCbCr data is generated, it is output following each rising edge of CLK2. The YCbCr data is multiplexed as [Cb Y Cr Y′ Cb Y Cr Y′...], with the first active data each scan line containing Cb data. The pixel output timing is shown in Figures 10 and 11.

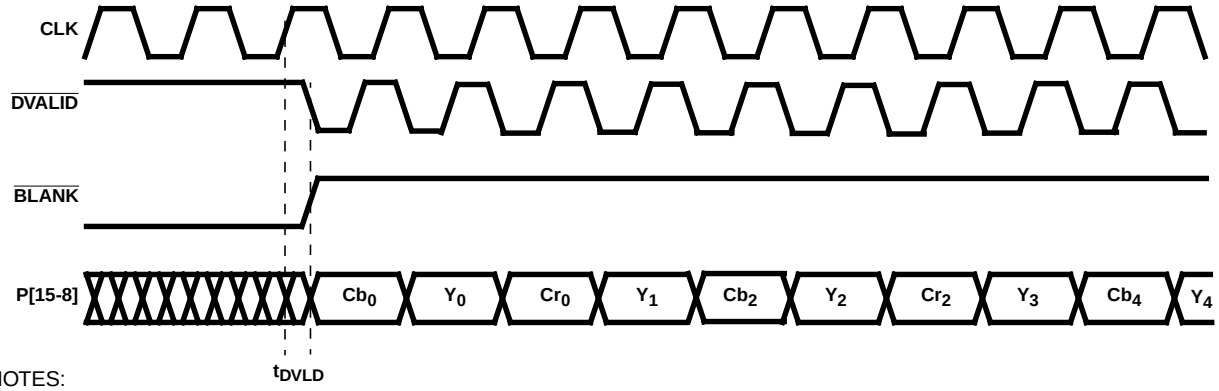
$\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{DVALID}}$, $\overline{\text{VBIVALID}}$, and FIELD are output following the rising edge of CLK2. When $\overline{\text{BLANK}}$ is asserted and $\overline{\text{VBIVALID}}$ is deasserted, the YCbCr outputs have a value of 16 for Y and 128 for Cb and Cr.



NOTE:

8. Y_0 is the first active luminance pixel data of a line. Cb_0 and Cr_0 are first active chrominance pixel data in a line. Cb and Cr will alternate every cycle due to the 4:2:2 subsampling. Pixel data is not output during the blanking period, but the values on the ports are forced to blanking levels.

FIGURE 10. OUTPUT TIMING FOR 8-BIT YCbCr MODE (DVLD_LTC = 0)



NOTES:

9. Y_0 is the first active luminance pixel data of a line. Cb_0 and Cr_0 are first active chrominance pixel data in a line. Cb and Cr will alternate every cycle due to the 4:2:2 subsampling. Pixel data is not output during the blanking period, but the values on the ports are forced to blanking levels.
10. When DVLD_LTC is set to 1, the polarity of $\overline{\text{DVALID}}$ needs to be set to active low, otherwise $\overline{\text{DVALID}}$ will stay low during active video and be gated with the clock only during the blanking interval.

FIGURE 11. OUTPUT TIMING FOR 8-BIT YCbCr MODE (DVLD_LTC = 1)

16-BIT YCbCr, 15-BIT RGB, OR 16-RGB OUTPUT

In these output modes, $\overline{\text{DVALID}}$ may be configured to operate in one of four modes as controlled by the DVLD_LTC and DVLD_DCYC bits of the GENLOCK CONTROL register (04_H). Bit 4 is the DVLD_LTC bit and bit 5 is the DVLD_DCYC bit.

If DVLD_LTC=0 and DVLD_DCYC=0, $\overline{\text{DVALID}}$ is present only during the active video time on active scan lines. Thus, $\overline{\text{DVALID}}$ being asserted indicates valid pixel data is present on the P0-P15 pixel outputs. $\overline{\text{DVALID}}$ is never asserted during the blanking intervals. In this mode $\overline{\text{DVALID}}$ will have a 50% duty cycle only during the active video times. The timing diagrams for this mode can be found in Figures 12 and 13.

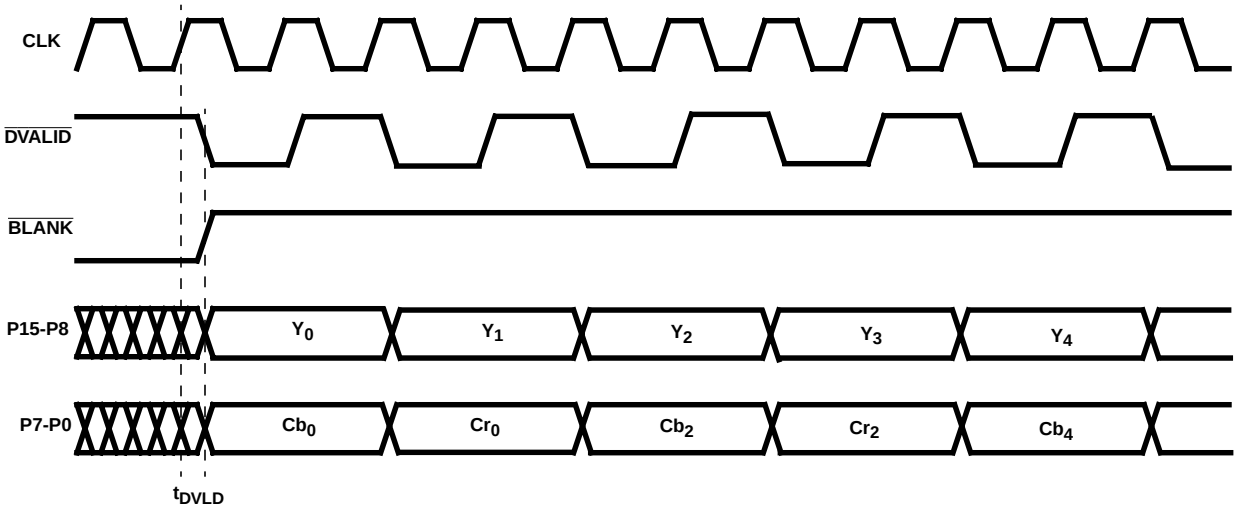
If DVLD_LTC=0 and DVLD_DCYC=1, $\overline{\text{DVALID}}$ behaves the same as the first mode, with the exception that $\overline{\text{DVALID}}$ does not have a 50% duty cycle. This mode is intended for backward compatibility with HMP8112(A) timing dependencies in which $\overline{\text{DVALID}}$ did not have a 50% duty cycle timing and other timing variations. The timing diagrams for this mode can be found in Figures 14 and 15.

If DVLD_LTC=1 and DVLD_DCYC=0, $\overline{\text{DVALID}}$ is present the entire line time on all scan lines. $\overline{\text{DVALID}}$ may occasionally be negated for two consecutive CLK2 cycles just prior to active video. In this mode $\overline{\text{DVALID}}$ is guaranteed have a 50% duty cycle only during the active video times. The timing for this mode differs from the timing shown in Figures 12 and 13 only in that $\overline{\text{DVALID}}$ will also be asserted during the blanking portion of the video line time as described above.

If DVLD_LTC=1 and DVLD_DCYC=1, $\overline{\text{DVALID}}$ is present during the entire line time on all scan lines. $\overline{\text{DVALID}}$ is asserted during the blanking intervals as needed to ensure a constant number of total samples per line. The timing for this mode differs from the timing shown in Figures 14 and 15 only in that $\overline{\text{DVALID}}$ will also be asserted during the blanking portion of the video line time as described above.

If 16-bit YCbCr, 15-bit RGB data, or 16-bit RGB data is generated, it is output following the rising edge of CLK2 while $\overline{\text{DVALID}}$ is asserted. Either linear or gamma-corrected RGB data may be output. The pixel output timing is shown in Figures 12 to 15.

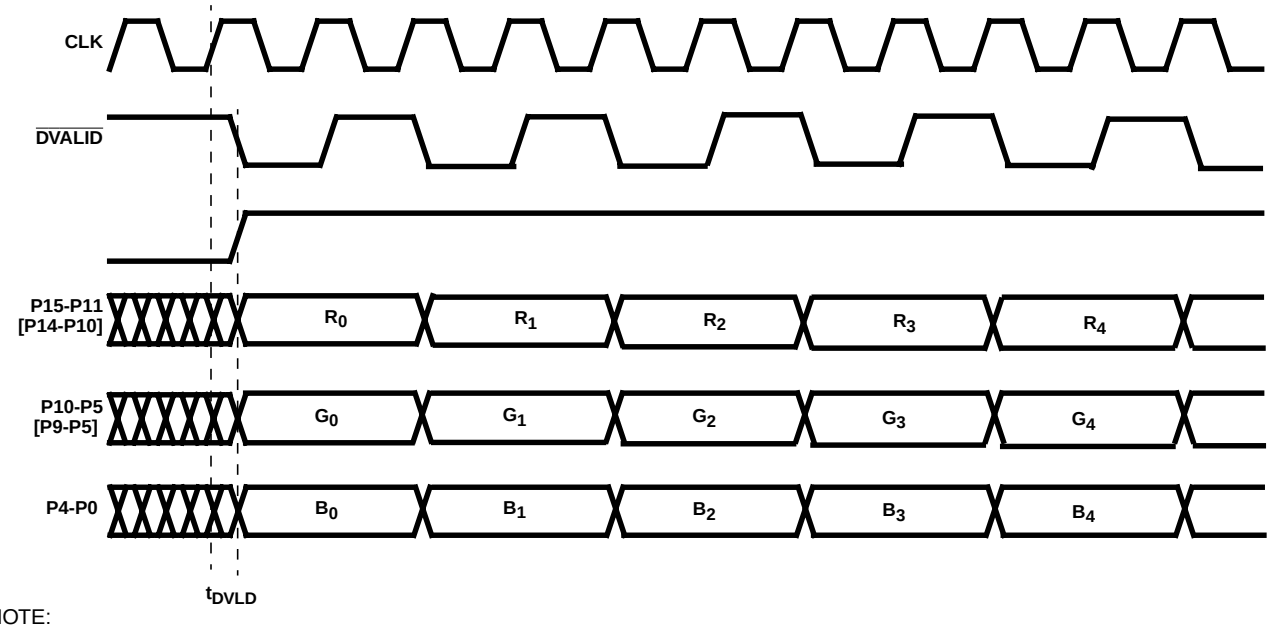
$\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{DVALID}}$, $\overline{\text{VBIVALID}}$, and FIELD are output following the rising edge of CLK2. When $\overline{\text{BLANK}}$ is asserted and $\overline{\text{VBIVALID}}$ is deasserted, the YCbCr outputs have a value of 16 for Y and 128 for Cb and Cr; the RGB outputs have a value of 0.



NOTES:

11. Y_0 is the first active luminance pixel data of a line. Cb_0 and Cr_0 are first active chrominance pixel data in a line. Cb and Cr will alternate every cycle due to the 4:2:2 subsampling.
12. $\overline{\text{BLANK}}$ is asserted per Figure 9.

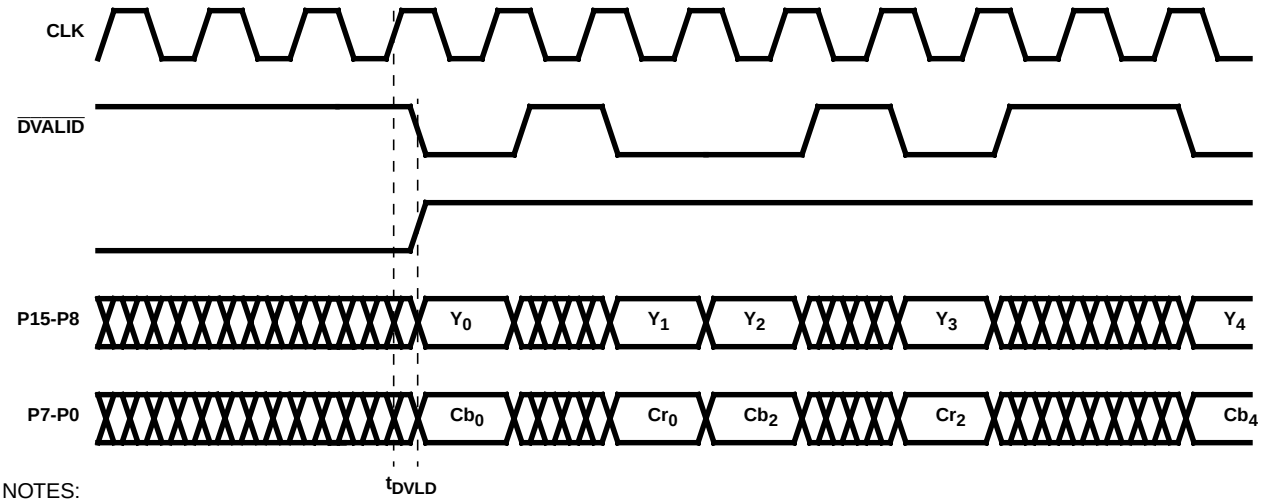
FIGURE 12. OUTPUT TIMING FOR 16-BIT YCbCr MODE (DVLD_LTC = 0, DVLD_DCYC = 0)



NOTE:

13. $\overline{\text{BLANK}}$ is asserted per Figure 9.

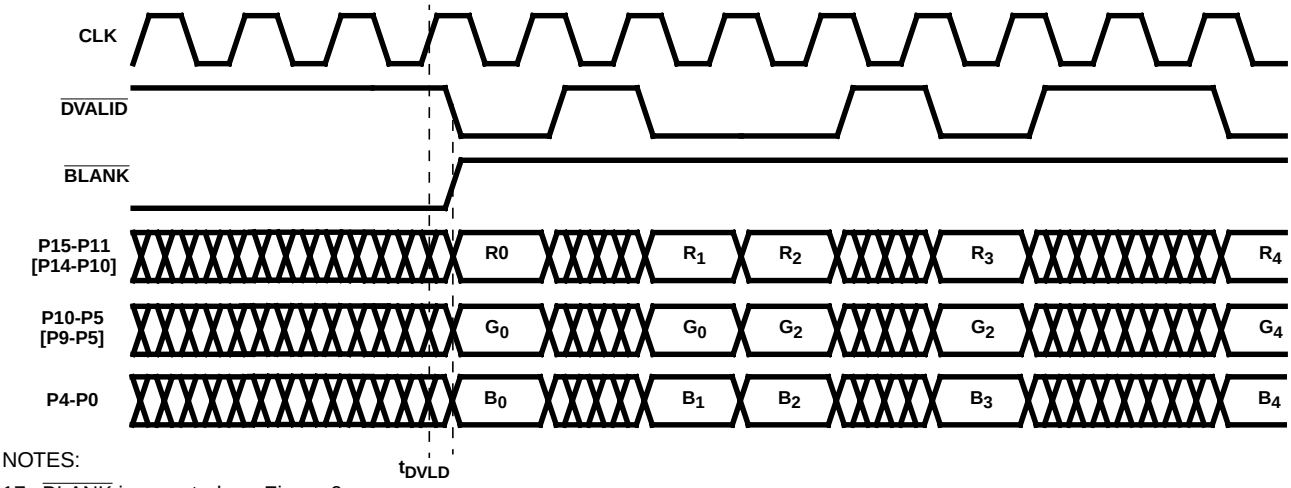
FIGURE 13. OUTPUT TIMING FOR 16-BIT [15-BIT] RGB MODE (DVLD_LTC = 0, DVLD_DCYC = 0)



NOTES:

14. Y_0 is the first active luminance pixel of a line. Cb_0 and Cr_0 are first active chrominance pixels in a line. Cb and Cr will alternate every cycle due to the 4:2:2 subsampling.
15. $\overline{\text{BLANK}}$ is asserted per Figure 9.
16. $\overline{\text{DVALID}}$ is asserted for every valid pixel during both active and blanking regions. $\overline{\text{DVALID}}$ is not a 50% duty cycle synchronous output and will appear to jitter as the Output Sample Rate converter adjusts the output timing for various data rates and clock frequency inputs.

FIGURE 14. OUTPUT TIMING FOR 16-BIT YCbCr MODE (DVLD_LTC = 0, DVLD_DCYC = 1)



NOTES:

17. $\overline{\text{BLANK}}$ is asserted per Figure 9.
18. $\overline{\text{DAVLID}}$ is asserted for every valid pixel during both active and blanking regions. $\overline{\text{DVALID}}$ is not a 50% duty cycle synchronous output and will appear to jitter as the Output Sample Rate converter adjusts the output timing for various data rates and clock frequency inputs.

FIGURE 15. OUTPUT TIMING FOR 16-BIT [15-BIT] RGB MODE (DVLD_LTC = 0, DVLD_DCYC = 1)

8-BIT BT.656 OUTPUT

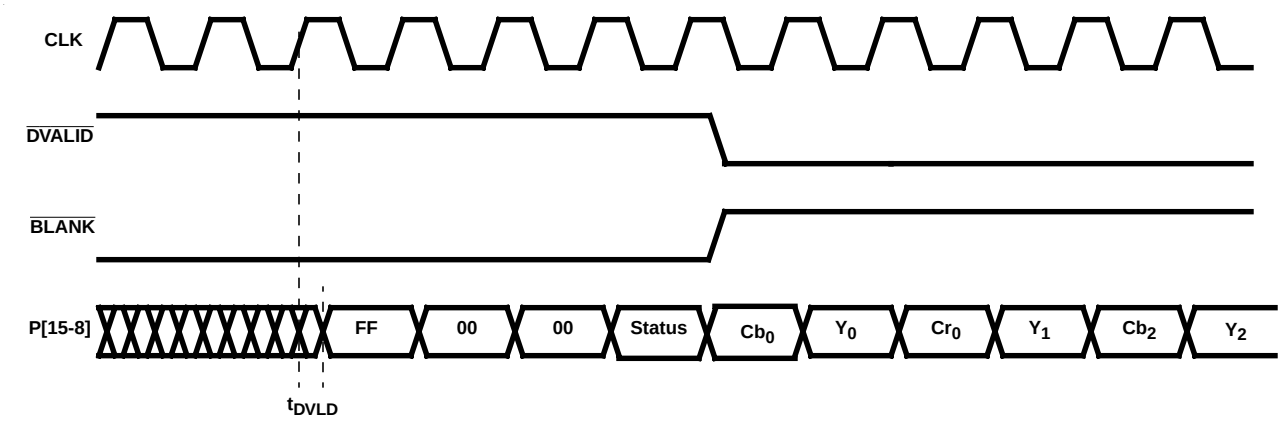
If BT.656 data is generated, it is output following each rising edge of CLK2. The BT.656 EAV and SAV formats are shown in Table 4 and the pixel output timing is shown in Figure 16. The EAV and SAV timing is determined by the programmed horizontal and vertical blank timing

$\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{DVALID}}$, $\overline{\text{VBIVALID}}$, and FIELD are output following the rising edge of CLK2.

For proper operation, CLK2 must be exactly 2x the desired output sample rate. The $\overline{\text{DVALID}}$ output is continuously asserted during the entire active video time.

During the blanking intervals, the YCbCr outputs have a value of 16 for Y and 128 for Cb and Cr, unless ancillary data is present.

Due to the use of digital PLLs and source video timing the total # of samples per line may not equal exactly 1716 (NTSC) or 1728 (PAL). The active video portion of the BT.656 data stream is always exactly 1440 continuous samples. Any line-to-line timing difference from nominal # of samples per line, plus or minus, is accommodated in the horizontal blanking interval.



NOTES:

19. Y_0 is the first active luminance pixel data of a line. Cb_0 and Cr_0 are first active chrominance pixel data in a line. Cb and Cr will alternate every cycle due to the 4:2:2 subsampling. Pixel data is not output during the blanking period.
20. Notice that $\overline{\text{DVALID}}$ is not asserted during the preamble and that $\overline{\text{BLANK}}$ is still asserted.
21. See Table 4 for Status bit definitions.

FIGURE 16. OUTPUT TIMING FOR 8-BIT BT.656 MODE

TABLE 4. BT.656 EAV AND SAV SEQUENCES

PIXEL INPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0
Status Word	1	F	V	H	P3	P2	P1	P0

NOTES:

22. P3 = V xor H; P2 = F xor H; P1 = F xor V; P0 = F xor V xor H
23. F: “0” = field 1; “1” = field 2
24. V: “1” during vertical blanking
25. H: “0” at SAV (start of active video); “1” at EAV (end of active video)

Advanced Features

In addition to digitizing an analog video signal the HMP8115 has hardware to process different types of Vertical Blanking Interval (VBI) data as described in the following sections.

“SLICED” VBI DATA CAPTURE

The HMP8115 implements “sliced” data capture of select types of VBI data. The VBI decoders incorporate detection hysteresis to prevent them from rapidly turning on and off due to noise and transmission errors. In order to handle real-world signals, the VBI decoders also compensate for DC offsets and amplitude variations.

CLOSED CAPTIONING

During closed captioning capture, the scan lines containing captioning information are monitored. If closed captioning is enabled and captioning data is present, the caption data is loaded into the caption data registers.

Detection of Closed Captioning

The closed caption decoder monitors the appropriate scan lines looking for the clock run-in and start bits used by captioning. If found, it locks to the clock run-in, the caption data is sampled and loaded into shift registers, and the data is then transferred to the caption data registers.

If the clock run-in and start bits are not found, it is assumed the scan line contains video data unless other VBI information is detected, such as teletext.

Once the clock run-in and start bits are found on the appropriate scan line for four consecutive odd fields, the Closed Captioning odd field Detect status bit is set to “1”. It is reset to “0” when the clock run-in and start bits are not found on the appropriate scan lines for four consecutive odd fields.

Once the clock run-in and start bits are found on the appropriate scan line for four consecutive even fields, the Closed Captioning even field Detect status bit is set to “1”. It is reset to “0” when the clock run-in and start bits are not found on the appropriate scan lines for four consecutive even fields.

Reading the Caption Data

The caption data registers may be accessed in two ways: via the I^2C interface or as BT.656 ancillary data.

Captioning Disabled on Both Lines

In this case, any caption data present is ignored.

The Caption odd field Read status bit and the Caption even field Read status bit are always a “0”.

Odd Field Captioning

In this case, any caption data present on line 284 (or line 281 or 335 in the PAL modes) is ignored. Caption data present on line 21 (or line 18 or 22 in the PAL modes) is captured into a shift register then transferred to CLOSED CAPTION_ODD_A register 20_H and CLOSED CAPTION_ODD_B register 21_H.

The Caption even field Read status bit is always a “0”. The Caption odd field Read status bit is set to “1” after data has been transferred from the shift register to the CLOSED CAPTION_ODD_A and CLOSED CAPTION_ODD_B registers. It is set to “0” after the data has been read out.

Even Field Captioning

In this case, any caption data present on line 21 (or line 18 or 22 in the PAL modes) is ignored. Caption data present on line 284 (or line 281 or 335 in the PAL modes) is captured into a shift register then transferred to CLOSED CAPTION_EVEN_A register 22_H and CLOSED CAPTION_EVEN_B register 23_H.

The Caption odd field Read status bit is always a “0”. The Caption even field Read status bit is set to “1” after data has been transferred from the shift register to the CLOSED CAPTION_EVEN_A and CLOSED CAPTION_EVEN_B registers. It is set to “0” after the data has been read out.

Odd and Even Field Captioning

Caption data present on line 21 (or line 18 or 22 in the PAL modes) is captured into a shift register then transferred to the CLOSED CAPTION_ODD_A and CLOSED CAPTION_ODD_B registers. Caption data present on line 284 (or line 281 or 335 in the PAL modes) is captured into a shift register then transferred to the CLOSED CAPTION_EVEN_A and CLOSED CAPTION_EVEN_B registers.

The Caption odd field Read status bit is set to “1” after data has been transferred from the shift register to the CLOSED CAPTION_ODD_A and CLOSED CAPTION_ODD_B registers. It is set to “0” after the data has been read out.

The Caption even field Read status bit is set to “1” after data has been transferred from the shift register to the CLOSED CAPTION_EVEN_A and CLOSED CAPTION_EVEN_B registers. It is set to “0” after the data has been read out.

WIDESCREEN SIGNALLING (WSS)

During WSS capture (ITU-R BT.1119 and EIAJ CPX-1204), the scan lines containing WSS information are monitored. If WSS is enabled and WSS data is present, the WSS data is loaded into the WSS data registers.

Detection of WSS

The WSS decoder monitors the appropriate scan lines looking for the run-in and start codes used by WSS. If found, it locks to the run-in code, the WSS data is sampled and loaded into shift registers, and the data is then transferred to the WSS data registers.

If the run-in and start codes are not found, it is assumed the scan line contains video data unless other VBI information is detected, such as teletext.

Once the run-in and start codes are found on the appropriate scan line for four consecutive odd fields, the WSS Line 20 Detect status bit is set to “1”. It is reset to “0” when the run-in and start codes are not found on the appropriate scan lines for four consecutive odd fields.

Once the run-in and start codes are found on the appropriate scan line for four consecutive even fields, the WSS Line 283 Detect status bit is set to “1”. It is reset to “0” when the clock run-in and start bits are not found on the appropriate scan lines for four consecutive even fields.

Reading the WSS Data

The WSS data registers may be accessed in two ways: via the I^2C interface or as BT.656 ancillary data.

WSS Disabled on Both Lines

In this case, any WSS data present is ignored.

The WSS odd field Read status bit and the WSS even field Read status bit are always a “0”.

Odd Field WSS

In this case, any WSS data present on line 283 (or line 280 or 336 in the PAL modes) is ignored. WSS data present on line 20 (or line 17 or 23 in the PAL modes) is captured into a shift register then transferred to the WSS_ODD_A and WSS_ODD_B data registers.

The WSS even field Read status bit is always a “0”. The WSS odd field Read status bit is set to “1” after data has been

transferred from the shift register to the WSS_ODD_A and WSS_ODD_B registers. It is set to “0” after the data has been read out.

Even Field WSS

In this case, any WSS data present on line 20 (or line 17 or 23 in the PAL modes) is ignored. WSS data present on line 283 (or line 280 or 336 in the PAL modes) is captured into a shift register then transferred to the WSS_EVEN_A and WSS_EVEN_B data registers.

The WSS odd field Read status bit is always a “0”. The WSS even field Read status bit is set to “1” after data has been transferred from the shift register to the WSS_EVEN_A and WSS_EVEN_B registers. It is set to “0” after the data has been read out.

Odd and Even WSS

WSS data present on line 20 (or line 17 or 23 in the PAL modes) is captured into a shift register then transferred to the WSS_ODD_A and WSS_ODD_B registers. WSS data present on line 283 (or line 280 or 336 in the PAL modes) is captured into a shift register then transferred to the WSS_EVEN_A and WSS_EVEN_B registers.

The WSS odd field Read status bit is set to “1” after data has been transferred from the shift register to the WSS_ODD_A and WSS_ODD_B registers. It is set to “0” after the data has been read out.

The WSS even field Read status bit is set to “1” after data has been transferred from the shift register to the WSS_EVEN_A and WSS_EVEN_B registers. It is set to “0” after the data has been read out.

BT.656 ANCILLARY DATA

Through the BT.656 interface the HMP8115 can generate non-active video data which contains CC, WSS, teletext or Real-Time Control Interface (RTCI) information. Teletext and RTCI data is only available as BT.656 ancillary data.

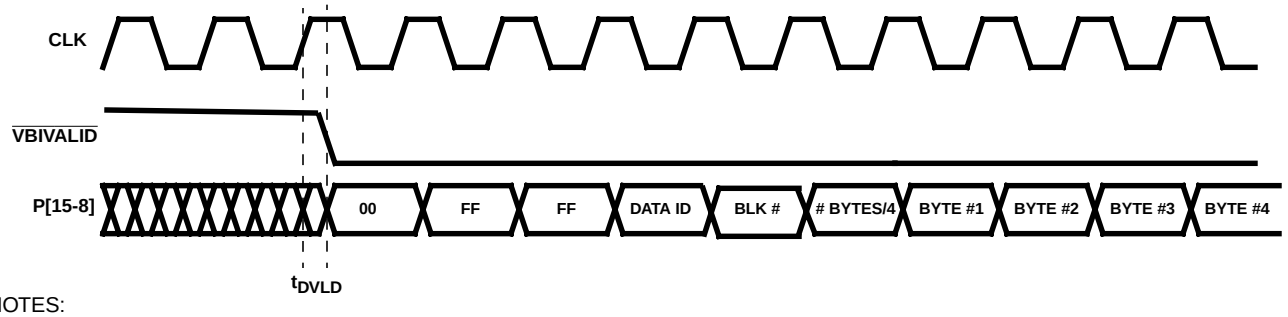
$\overline{\text{VBIVALID}}$ OUTPUT TIMING

The $\overline{\text{VBIVALID}}$ output is asserted when outputting closed captioning, widescreen signalling, teletext or RTCI data as BT.656 ancillary data. It is asserted during the entire BT.656 ancillary data packet time, including the preamble.

BT.656 CLOSED CAPTIONING AND WIDE SCREEN SIGNALLING

Table 5 illustrates the format when outputting the caption data registers as BT.656 ancillary data. The ancillary data is present during the horizontal blanking interval after the line containing the captioning information.

Table 6 illustrates the format when outputting the WSS data registers as BT.656 ancillary data. The ancillary data is present during the horizontal blanking interval after the line containing the WSS information.



NOTES:

26. BT.656 VBI ancillary starts with a 00H, FFH and FFH sequence which is opposite to the SAV/EAV sequence of FFH, 00H and 00H.

27. During active VBI data intervals, $\overline{\text{DVALID}}$ is deasserted and $\overline{\text{BLANK}}$ is asserted.

FIGURE 17. OUTPUT TIMING FOR BT.656 VBI DATA TRANSFERS (CC, WSS, TELETEXT, RTCI)

TABLE 5. READING THE CLOSED CAPTION DATA AS BT.656 ANCILLARY DATA

PIXEL OUTPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1
Data ID	$\overline{\text{P14}}$	ep	1	1	0	0	0	0 = odd field data 1 = even field data
Data Block Number	$\overline{\text{P14}}$	ep	0	0	0	0	0	1
Data Word Count	$\overline{\text{P14}}$	ep	0	0	0	0	0	1
Caption Data	$\overline{\text{P14}}$	ep	0	0	bit 15	bit 14	bit 13	bit 12
	$\overline{\text{P14}}$	ep	0	0	bit 11	bit 10	bit 9	bit 8
	$\overline{\text{P14}}$	ep	0	0	bit 7	bit 6	bit 5	bit 4
	$\overline{\text{P14}}$	ep	0	0	bit 3	bit 2	bit 1	bit 0
CRC	$\overline{\text{P14}}$	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

NOTES:

28. ep = even parity for P8-P13.

29. CRC = Sum of P8-P14 of Data ID through last user data word. Preset to all zeros, carry is ignored.

TABLE 6. OUTPUTTING THE SLICED WSS DATA AS BT.656 ANCILLARY DATA

PIXEL OUTPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1
Data ID	$\overline{P14}$	ep	1	1	0	0	1	0 =odd field data 1 =even field data
Data Block Number	$\overline{P14}$	ep	0	0	0	0	0	1
Data Word Count	$\overline{P14}$	ep	0	0	0	0	1	0
WSS Data	$\overline{P14}$	ep	0	0	0	0	bit 13	bit 12
	$\overline{P14}$	ep	0	0	bit 11	bit 10	bit 9	bit 8
	$\overline{P14}$	ep	0	0	bit 7	bit 6	bit 5	bit 4
	$\overline{P14}$	ep	0	0	bit 3	bit 2	bit 1	bit 0
WSS CRC Data	$\overline{P14}$	ep	0	0	0	0	bit 5	bit 4
	$\overline{P14}$	ep	0	0	bit 3	bit 2	bit 1	bit 0
	$\overline{P14}$	ep	0	0	0	0	0	0
	$\overline{P14}$	ep	0	0	0	0	0	0
CRC	$\overline{P14}$	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

NOTES:

30. ep = even parity for P8-P13.

31. WSS CRC data = “00 0000” during PAL operation.

32. CRC = Sum of P8-P14 of Data ID through last user data word. Preset to all zeros, carry is ignored.

TELETEXT

The HMP8115 supports ITU-R BT.653 625-line and 525-line teletext system B, C and D capture. NABTS (North American Broadcast Teletext Specification) is the same as BT.653 525-line system C, which is also used to transmit Intel Intercast™ information. WST (World System Teletext) is the same as BT.653 system B. Figure 18 shows the basic structure of a video signal that contains teletext data.

The scan lines containing teletext information are monitored. If teletext is enabled and teletext data is present, the teletext data is output as BT.656 ancillary data.

Detection of Teletext

The teletext decoder monitors the scan lines, looking for the 16-bit clock run-in (sometimes referred to as the clock synchronization code) used by teletext. If found, it locks to the clock run-in, the teletext data is sampled and loaded into shift registers, and the data is then transferred to internal holding registers.

If the clock run-in is not found, it is assumed the scan line contains video data unless other VBI information is detected, such as WSS.

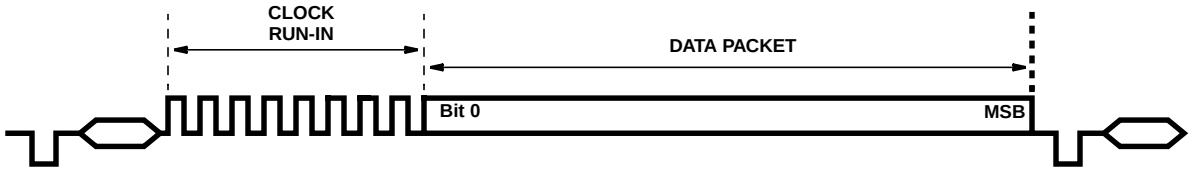
If a teletext clock run-in is found before line 23 or line 289 for NTSC and (M) PAL, or line 336 for (B, D, G, H, I, N, N_C) PAL, the VBI Teletext Detect status bit is immediately set to “1”. If not found by these lines, the status bit is immediately reset to “0”.

Accessing the Teletext Data

The teletext data must be output as BT.656 ancillary data. The I^2C interface does not have the bandwidth to output teletext information when needed.

Table 7 illustrates the teletext BT.656 ancillary data format and Figure 17 depicts the portion of the incoming teletext signal which is sliced and output as part of the ancillary data stream. The teletext data is present during the horizontal blanking interval after the line containing the teletext information. The actual BT.656 bytes that contain teletext data only contain 4 bits of the actual data packet. Note that only the data packet of Figure 18 is sent as ancillary data; the clock run-in is not included in the data stream.

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NOTES:

33. The MSB is bit number: 271 for system C, 279 for system B 525-line and 343 for system B 625-line.

34. The clock run-in is 16 bits wide for both systems and is not included in the BT.656 ancillary data stream.

35. The bit rate is 5.727272 Mbits/second for system B and C on 525/60 systems and 6.9375 and 5.734375 Mbits/second respectively for 625/50 systems.

FIGURE 18. TELETEXT VBI VIDEO SIGNAL

TABLE 7. OUTPUTTING THE SLICED TELETEXT DATA AS BT.656 ANCILLARY DATA

PIXEL INPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1
Data ID	$\overline{P14}$	ep	1	1	0	1	0	0
Data Block Number	$\overline{P14}$	ep	0	0	0	0	0	1
Data Word Count	$\overline{P14}$	ep	0	1	0	1	1	0
Teletext Data (B, 625-line = 43 bytes) (B, 525-line = 35 bytes) (C = 34 bytes)	$\overline{P14}$	ep	0 = 525-line 1 = 625-line	0 = system B 1 = system C	bit 343	bit 342	bit 341	bit 340
	$\overline{P14}$	ep	0	0	bit 339	bit 338	bit 337	bit 336
	:							
	$\overline{P14}$	ep	0	0	bit 7	bit 6	bit 5	bit 4
	$\overline{P14}$	ep	0	0	bit 3	bit 2	bit 1	bit 0
Reserved	$\overline{P14}$	ep	0	0	0	0	0	0
	$\overline{P14}$	ep	0	0	0	0	0	0
CRC	$\overline{P14}$	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

NOTES:

36. ep = even parity for P8-P13.

37. CRC = Sum of P8-P14 of Data ID through last user data word. Preset to all zeros, carry is ignored.

38. For 525-line system B, bits 280-343 are “0”.

39. For system C, bits 272-343 are “0”.

REAL TIME CONTROL INTERFACE

The Real Time Control Interface (RTCI) outputs timing information for a NTSC/PAL encoder as BT.656 ancillary data. This allows the encoder to generate “clean” output video.

RTCI information via BT.656 ancillary data is shown in Table 8. If enabled, this transfer occurs once per line and is completed before the start of the SAV sequence.

The PSW bit is always a “0” for NTSC encoding. During PAL encoding, it indicates the sign of V (“0” = negative; “1” = positive) for that scan line.

TABLE 8. OUTPUTTING RTCI AS BT.656 ANCILLARY DATA

PIXEL INPUT	P15	P14	P13	P12	P11	P10	P9	P8
Preamble	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1
Data ID	$\overline{P14}$	ep	1	1	0	1	0	1
Data Block Number	$\overline{P14}$	ep	0	0	0	0	0	1
Data Word Count	$\overline{P14}$	ep	0	0	0	0	1	1
HPLL Increment	$\overline{P14}$	ep	0	0	0	0	0	0
	$\overline{P14}$	ep	0	0	0	0	0	0
	$\overline{P14}$	ep	0	0	0	0	0	0
	$\overline{P14}$	ep	0	0	0	0	0	0
FSCPLL Increment	$\overline{P14}$	ep	PSW	0	bit 31	bit 30	bit 29	bit 28
	$\overline{P14}$	ep	F2 = 0	F1 = 0	bit 27	bit 26	bit 25	bit 24
	:							
	$\overline{P14}$	ep	0	0	bit 7	bit 6	bit 5	bit 4
	$\overline{P14}$	ep	0	0	bit 3	bit 2	bit 1	bit 0
CRC	$\overline{P14}$	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

NOTES:

40. ep = even parity for P8-P13.

41. CRC = Sum of P8-P14 of Data ID through last user data word. Preset to all zeros, carry is ignored.

Host Interface

All internal registers may be written to or read by the host processor at any time, except for those bits identified as read-only. The bit descriptions of the control registers are listed in Tables 9-48.

The HMP8115 supports the fast-mode (up to 400 kbps) I^2C interface consisting of the SDA and SCL pins. The device acts as a slave for receiving and transmitting data over the serial interface. When the interface is not active, SCL and SDA must be pulled high using external 4kΩ pull-up resistors. The slave address for the HMP8115 is 88_H.

Data is placed on the SDA line when the SCL line is low and held stable when the SCL line is pulled high. Changing the state of the SDA line while SCL is high will be interpreted as either an I^2C bus START or STOP condition as indicated by Figure 20.

During I^2C write cycles, the first data byte after the slave address is treated as the control register sub address and is written into the internal address register. Any remaining data bytes sent during an I^2C write cycle are written to the control registers, beginning with the register specified by the address register as given in the first byte. The address register is then autoincremented after each additional data byte sent on the I^2C bus during a write cycle. Writes to reserved bits within registers or reserved registers are ignored.

In order to perform a read from a specific control register within the HMP8115, an I^2C bus write must first be performed to properly setup the address register. Then an I^2C bus read can be performed to read from the desired control register(s). As a result of needing the write cycle for a read cycle there are actually two START conditions as shown in Figure 21. The address register is then autoincremented after each byte read during the I^2C read cycle. Reserved registers return a value of 00_H.

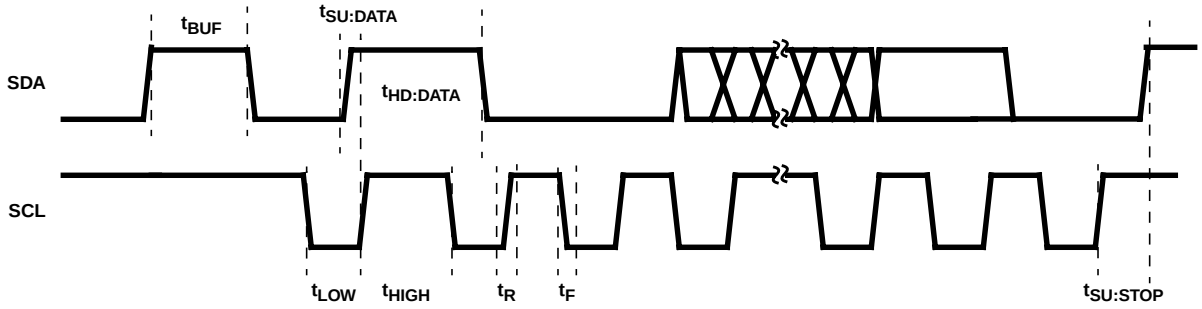


FIGURE 19. I^2C TIMING DIAGRAM

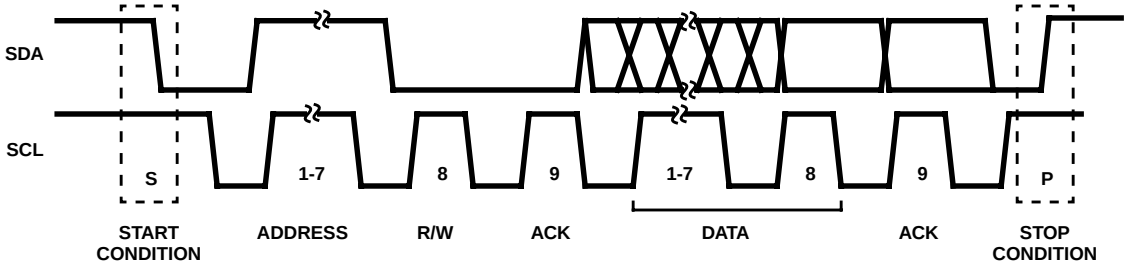


FIGURE 20. I^2C SERIAL DATA FLOW

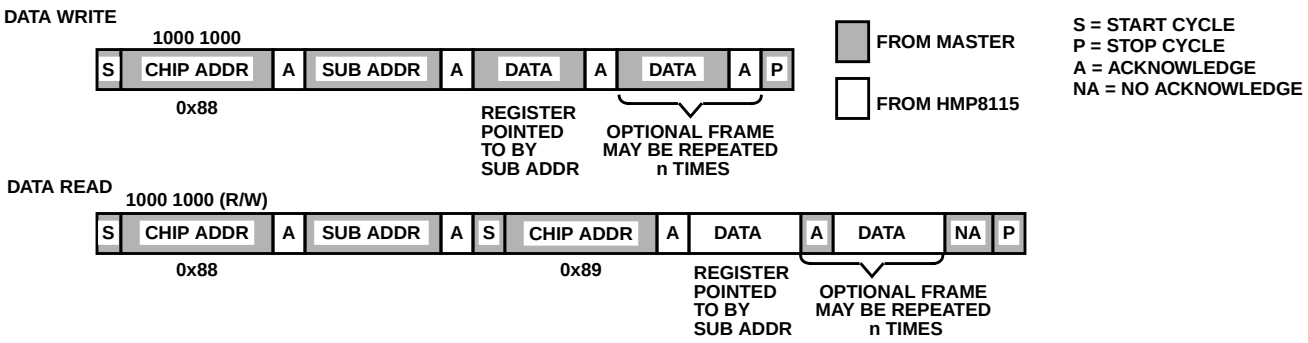


FIGURE 21. REGISTER WRITE/READ FLOW

HMP8115 Control Registers

TABLE 9. 8115 REGISTER SUMMARY

SUB-ADDRESS	CONTROL REGISTER	RESET/ DEFAULT VALUE	USE VALUE	COMMENTS
00_H	PRODUCT ID	15_H		
01_H	INPUT FORMAT	18_H		Defaults to Autodetect of input video standard
02_H	OUTPUT FORMAT	00_H		Defaults to 16-bit YCbCr format
03_H	OUTPUT CONTROL	00_H		Defaults to outputs disabled
04_H	GENLOCK CONTROL	01_H		Defaults to 27MHz CLK2, Rectangular Pixel mode
05_H	ANALOG INPUT CONTROL	00_H		Defaults to input signal select = NTSC/PAL1
06_H	COLOR PROCESSING	52_H		
07_H	RESERVED	-		
08_H	LUMA PROCESSING	04_H		
09_H	Reserved	-		
$0A_H$	SLICED VBI DATA ENABLE	00_H		
$0B_H$	SLICED VBI DATA OUTPUT	00_H		
$0C_H$	VBI DATA STATUS	00_H		
$0D_H$	Reserved	-		
$0E_H$	VIDEO STATUS	00_H		
$0F_H$	INTERRUPT MASK	00_H		
10_H	INTERRUPT STATUS	00_H		
11_H-17_H	Reserved	-		
18_H	BRIGHTNESS	00_H		
19_H	CONTRAST	80_H		
$1A_H$	HUE	00_H		
$1B_H$	SATURATION	80_H		
$1C_H$	COLOR GAIN	40_H		
$1D_H$	Reserved	-		
$1E_H$	SHARPNESS	10_H		
$1F_H$	HOST CONTROL	00_H		
20_H	CLOSED CAPTION_ODD_A	80_H		
21_H	CLOSED CAPTION_ODD_B	80_H		
22_H	CLOSED CAPTION_EVEN_A	80_H		
23_H	CLOSED CAPTION_EVEN_B	80_H		
24_H	WSS_ODD_A	00_H		
25_H	WSS_ODD_B	00_H		
26_H	WSS_CRC_ODD	00_H		
27_H	WSS_EVEN_A	00_H		
28_H	WSS_EVEN_B	00_H		
29_H	WSS_CRC_EVEN	00_H		
$2A_H$-$2F_H$	Reserved	-		

TABLE 9. 8115 REGISTER SUMMARY (Continued)

SUB-ADDRESS	CONTROL REGISTER	RESET/ DEFAULT VALUE	USE VALUE	COMMENTS
30_H	START H_BLANK LOW	$4A_H$	Table 2	
31_H	START H_BLANK HIGH	03_H	Table 2	
32_H	END H_BLANK	$7A_H$	Table 2	
33_H	START V_BLANK LOW	02_H	Table 2	
34_H	START V_BLANK HIGH	01_H	Table 2	
35_H	END V_BLANK	12_H	Table 2	
36_H	END HSYNC	40_H	Table 2	
37_H	HSYNC DETECT WINDOW	FF_H	20_H	Recommend HSYNC DETECT WINDOW= 20_H
38_H-$3F_H$	Reserved	-		
40_H-$7F_H$	Test and Unused	-		

TABLE 10. PRODUCT ID REGISTER

SUB ADDRESS = 00_H			
BIT NO.	FUNCTION	DESCRIPTION	RESET STATE
7-0	Product ID	This 8-bit register specifies the last two digits of the product number. It is a read-only register. Data written to it is ignored.	15_H

TABLE 11. INPUT FORMAT REGISTER

SUB ADDRESS = 01_H			
BIT NO.	FUNCTION	DESCRIPTION	RESET STATE
7	Reserved		0_B
6-5	Video Timing Standard	These bits are read only unless D4 = “0”. 00 = (M) NTSC 01 = (B, D, G, H, I, N) PAL 10 = (M) PAL 11 = Combination (N) PAL; also called (N_C) PAL	00_B
4	Auto Detect Video Standard	0 = Manual selection of video timing standard 1 = Auto detect of video timing standard	1_B
3	Setup Select	Typically, this bit should be a “1” during (M) NTSC and (M, N) PAL operation. Otherwise, it should be a “0”. 0 = Video source has a 0 IRE blanking pedestal 1 = Video source has a 7.5 IRE blanking pedestal	1_B
2-0	Reserved		000_B

TABLE 12. OUTPUT FORMAT REGISTER

SUB ADDRESS = 02_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-5	Output Color Format	000 = 16-bit 4:2:2 YCbCr 001 = 8-bit 4:2:2 YCbCr 010 = 8-bit BT.656 011 = 15-bit RGB 100 = 16-bit RGB 101 = reserved 110 = reserved 111 = reserved	000_B
4-3	RGB Gamma Select	These bits are ignored except during RGB output modes. 00 = Linear RGB (gamma of input source = 2.2) 01 = Linear RGB (gamma of input source = 2.8) 10 = Gamma-corrected RGB (gamma = gamma of input source) 11 = reserved	00_B
2-1	Output Color Select	00 = Normal operation 01 = Output blue field 10 = Output black field 11 = Output 75% color bars	00_B
0	Vertical Pixel Siting	This bit specifies whether or not the chrominance pixels have a half-line pixel offset from their associated luminance pixels. 0 = Half-line offset 1 = Aligned	0_B

TABLE 13. OUTPUT CONTROL REGISTER

SUB ADDRESS = 03_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Video Data Output Enable	This bit is used to enable the P0-P15 outputs. 0 = Outputs 3-stated 1 = Outputs enabled	0_B
6	Video Timing Output Enable	This bit is used to enable the $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$, FIELD, $\overline{\text{VBIVALID}}$, $\overline{\text{DVALID}}$, and $\overline{\text{INTREQ}}$ outputs. 0 = Outputs 3-stated 1 = Outputs enabled	0_B
5	FIELD Polarity	0 = Active low (low during odd fields) 1 = Active high (high during odd fields)	0_B
4	Polarity $\overline{\text{BLANK}}$	0 = Active low (low during blanking) 1 = Active high (high during blanking)	0_B
3	$\overline{\text{HSYNC}}$ Polarity	0 = Active low (low during horizontal sync) 1 = Active high (high during horizontal sync)	0_B
2	$\overline{\text{VSYNC}}$ Polarity	0 = Active low (low during vertical sync) 1 = Active high (high during vertical sync)	0_B
1	$\overline{\text{DVALID}}$ Polarity	0 = Active low (low during valid pixel data) 1 = Active high (high during valid pixel data)	0_B
0	$\overline{\text{VBIVALID}}$ Polarity	0 = Active low (low during VBI data) 1 = Active high (high during VBI data)	0_B

TABLE 14. GENLOCK CONTROL REGISTER

SUB ADDRESS = 04_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Aspect Ratio Mode	0 = Rectangular (BT.601) pixels 1 = Square pixels	0_B
6	Freeze Output Timing Enable	Setting this bit to a “1” freezes the output timing at the end of the field. Resetting this bit to a “0” resumes normal operation at the start of the next field. 0 = Normal operation 1 = Freeze output timing	0_B
5	$\overline{\text{DVALID}}$ Duty Cycle Control (DVLD_DCYC)	This bit is ignored during the 8-bit YCbCr and BT.656 output modes. During 16-bit YCbCr, 15-bit RGB, or 16-bit RGB output modes, this bit is defined as: 0 = $\overline{\text{DVALID}}$ has 50/50 duty cycle at the pixel output datarate 1 = $\overline{\text{DVALID}}$ goes active based on linelock. This will cause $\overline{\text{DVALID}}$ to not have a 50/50 duty cycle. This bit is intended to be used in maintaining backward compatibilty with the HMP8112A $\overline{\text{DVALID}}$ output timing.	0_B
4	$\overline{\text{DVALID}}$ Line Timing Control (DVLD_LTC)	During 16-bit YCbCr, 15-bit RGB, or 16-bit RGB output modes, this bit is defined as: 0 = $\overline{\text{DVALID}}$ present only during active video time on active scan lines 1 = $\overline{\text{DVALID}}$ present the entire scan line time on all scan lines During the 8-bit YCbCr and BT.656 output modes, this bit defines the $\overline{\text{DVALID}}$ output signal as: 0 = Normal timing 1 = $\overline{\text{DVALID}}$ signal ANDed with CLK2	0_B
3	Missing $\overline{\text{HSYNC}}$ Detect Select	This bit specifies the number of missing horizontal sync pulses before the device goes into the horizontal lock acquisition mode. In mode “0”, the default value of the HPLL Adjust register should be used. In mode “1”, the typical values the HPLL Adjust register should be 10_H to 20_H. 0 = 12 pulses 1 = 1 pulse	0_B
2	Missing $\overline{\text{VSYNC}}$ Detect Select	This bit specifies the number of missing vertical sync pulses before the device goes into the vertical lock acquisition mode. 0 = 3 pulses 1 = 1 pulse	0_B
1-0	CLK2 Frequency	This bit indicates the frequency of the CLK2 input clock. 00 = 24.54MHz 01 = 27.0MHz 10 = 29.5MHz 11 = Reserved	01_B

TABLE 15. ANALOG INPUT CONTROL REGISTER

SUB ADDRESS = 05_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-3	Reserved		00000_B
2-0	Video Signal Input Select	000 = NTSC/PAL 1 001 = NTSC/PAL 2 010 = NTSC/PAL 3 011 = S-video 100 = reserved 101 = reserved 110 = reserved 111 = reserved	000_B

TABLE 16. COLOR PROCESSING REGISTER

SUB ADDRESS = 06_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Color Gain Control Select	If a value of “10”, the color gain adjust register is used to specify the amount of color gain to be applied. 00 = No gain control (gain = 1x) 01 = Automatic gain control 10 = Fixed gain control 11 = Freeze automatic gain control	01_B
5-4	Color Killer Select	00 = Force color on 01 = Enable color killer 10 = reserved 11 = Force color off	01_B
3-2	Color Coring Select	Coring may be used to reduce low-level noise around zero (code 128) in the CbCr signals. 00 = No coring 01 = 1 code coring 10 = 2 code coring 11 = 3 code coring	00_B
1	Contrast Control Select	This bit specifies whether the contrast control affects just the Y data (“0”) or both the Y and CbCr data (“1”). To avoid color shifts when changing contrast, this bit should be a “1”. 0 = Contrast controls only Y data 1 = Contrast controls Y and CbCr data	1_B
0	Color Lowpass Filter Select	This bit selects the bandwidth of the CbCr data. 0 = 850kHz 1 = 1.5MHz	0_B

TABLE 17. LUMA PROCESSING REGISTER

SUB ADDRESS = 08_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Y Filtering Select	The chroma trap filter may be used to remove any residual color subcarrier information from the Y channel. During S-video operation, it should be disabled. During PAL operation, it should be enabled. The 3MHz lowpass filter may be used to remove high-frequency noise. 00 = No filtering 01 = Enable chroma trap filter 10 = Enable 3.0MHz lowpass filter 11 = reserved	00_B
5-4	Black Level Y Coring Select	Coring may be used to reduce low-level noise around black in the Y signal. 00 = No coring 01 = 1 code coring 10 = 2 code coring 11 = 3 code coring	00_B
3-2	High Frequency Y Coring Select	Coring may be used to reduce high-frequency low-level noise in the Y signal. 00 = No coring 01 = 1 code coring 10 = 2 code coring 11 = 3 code coring	01_B
1-0	Sharpness Frequency Select	If a value of “01” or “10”, the sharpness adjust register is used to specify the amount of sharpness to be applied. 00 = Bypass sharpness control 01 = Maximum gain at 2.6MHz 10 = Maximum gain at color subcarrier frequency 11 = reserved	00_B

TABLE 18. SLICED VBI DATA ENABLE REGISTER

SUB ADDRESS = $0A_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Sliced Closed Captioning Enable	00 = Closed caption disabled 01 = Closed caption enabled for odd fields: line 21 for NTSC, line 18 for (M) PAL, or line 22 for (B, D, G, H, I, N, N_C) PAL 10 = Closed caption enabled for even fields: line 284 for NTSC, line 281 for (M) PAL, or line 335 for (B, D, G, H, I, N, N_C) PAL 11 = Closed caption enabled for both odd and even fields	00_B
5-4	Sliced WSS Enable	00 = WSS disabled 01 = WSS enabled for odd fields: line 20 for NTSC; line 17 for (M) PAL, or line 23 for (B, D, G, H, I, N, N_C) PAL 10 = WSS enabled for even fields: line 283 for NTSC, line 280 for (M) PAL, or line 336 for (B, D, G, H, I, N, N_C) PAL 11 = WSS enabled for both odd and even fields	00_B
3-2	Sliced Teletext Enable	00 = Teletext disabled 01 = Teletext system B enabled 10 = Teletext system C enabled 11 = reserved	00_B
1-0	Reserved		00_B

TABLE 19. SLICED VBI DATA OUTPUT REGISTER

SUB ADDRESS = $0B_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Sliced Closed Caption BT.656 Output Enable	This bit specifies whether or not to output the caption data registers as BT.656 ancillary data. It is ignored unless captioning is enabled. Access via the I^2C interface is always available. 0 = Do not output as BT.656 ancillary data 1 = Output as BT.656 ancillary data	0_B
6	Sliced WSS BT.656 Output Enable	This bit specifies whether or not to output the WSS data registers as BT.656 ancillary data. It is ignored unless WSS is enabled. Access via the I^2C interface is always available. 0 = Do not output as BT.656 ancillary data 1 = Output as BT.656 ancillary data	0_B
5	Sliced Teletext BT.656 Output Enable	This bit specifies whether or not to output teletext data as BT.656 ancillary data. It is ignored unless teletext is enabled. 0 = Do not output as BT.656 ancillary 1 = Output as BT.656 ancillary data	0_B
4-1	Reserved		0000_B
0	RTCI BT.656 Output Enable	This bit specifies whether or not to output RTCI data as BT.656 ancillary data. 0 = Do not output as BT.656 ancillary 1 = Output as BT.656 ancillary data	0_B

TABLE 20. VBI DATA STATUS REGISTER

SUB ADDRESS = $0C_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Closed Captioning Odd Field Detect Status	This bit is read-only. Data written to this bit is ignored. 0 = Closed captioning not detected 1 = Closed captioning detected	0_B
6	Closed Captioning Even Field Detect Status	This bit is read-only. Data written to this bit is ignored. 0 = Closed captioning not detected 1 = Closed captioning detected	0_B
5	WSS Odd Field Detect Status	This bit is read-only. Data written to this bit is ignored. 0 = WSS not detected 1 = WSS detected	0_B
4	WSS Even Field Detect Status	This bit is read-only. Data written to this bit is ignored. 0 = WSS not detected 1 = WSS detected	0_B
3	VBI Teletext Detect Status	This bit is read-only. Data written to this bit is ignored. 0 = Teletext not detected during vertical blanking interval 1 = Teletext detected during vertical blanking interval	0_B
2-0	Reserved		000_B

TABLE 21. VIDEO STATUS REGISTER

SUB ADDRESS = $0E_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Vertical Lock Status	This bit is read-only. Data written to this bit is ignored. 0 = Not vertically locked 1 = Vertically locked	0_B
6	Horizontal Lock Status	This bit is read-only. Data written to this bit is ignored. 0 = Not horizontally locked 1 = Horizontally locked	0_B
5	Color Lock Status	This bit is read-only. Data written to this bit is ignored. 0 = Not color locked 1 = Color locked	0_B
4	Input Video Detect Status	This bit is read-only. Data written to this bit is ignored. 0 = Input video not detected on selected video input 1 = Input video detected on selected video input	0_B
3-0	Reserved		0000_B

TABLE 22. INTERRUPT MASK REGISTER

SUB ADDRESS = $0F_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Genlock Loss Interrupt Mask	If this bit is a “1”, an interrupt is generated when genlock is lost. 0 = Interrupt disabled 1 = Interrupt enabled	0_B
6	Input Signal Loss Interrupt Mask	If this bit is a “1”, an interrupt is generated when a video signal is no longer detected on the selected video input. 0 = Interrupt disabled 1 = Interrupt enabled	0_B
5	Closed Caption Interrupt Mask	If this bit is a “1”, an interrupt is generated when the Caption_ODD_A and Caption_ODD_B or the Caption_EVEN_A and Caption_EVEN_B data registers contain new data. 0 = Interrupt disabled 1 = Interrupt enabled	0_B
4	WSS Interrupt Mask	If this bit is a “1”, an interrupt is generated when the WSS_ODD_A and WSS_ODD_B or the WSS_EVEN_A and WSS_EVEN_B data registers contain new data. 0 = Interrupt disabled 1 = Interrupt enabled	0_B
3	Teletext Interrupt Mask	If this bit is a “1”, an interrupt is generated when teletext information is first detected at the beginning of each field. 0 = Interrupt disabled 1 = Interrupt enabled	0_B
2-1	Reserved		00_B
0	Vertical Sync Interrupt Mask	If this bit is a “1”, an interrupt is generated at the beginning of each field. 0 = Interrupt disabled 1 = Interrupt enabled	0_B

TABLE 23. INTERRUPT STATUS REGISTER

SUB ADDRESS = 10_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Genlock Loss Interrupt Status	If this bit is a “1”, the reason for the interrupt request was that genlock was lost. To clear the interrupt request, a “1” must be written to this bit.	0_B
6	Input Signal Loss Interrupt Status	If this bit is a “1”, the reason for the interrupt request was that the input video source is no longer present. To clear the interrupt request, a “1” must be written to this bit.	0_B
5	Closed Caption Interrupt Status	If this bit is a “1”, the reason for the interrupt request was that the Caption_ODD_A and Caption_ODD_B or the Caption_EVEN_A and Caption_EVEN_B data registers contain new data. To clear the interrupt request, a “1” must be written to this bit.	0_B
4	WSS Interrupt Status	If this bit is a “1”, the reason for the interrupt request was that the WSS_ODD_A and WSS_ODD_B or the WSS_EVEN_A and WSS_EVEN_B data registers contain new data. To clear the interrupt request, a “1” must be written to this bit.	0_B
3	Teletext Interrupt Status	If this bit is a “1”, the reason for the interrupt request was that teletext data has been detected in the current field. To clear the interrupt request, a “1” must be written to this bit.	0_B
2-1	Reserved		00_B
0	Vertical Sync Interrupt Status	If this bit is a “1”, the reason for the interrupt request was that a new field was started. To clear the interrupt request, a “1” must be written to this bit.	0_B

TABLE 24. BRIGHTNESS REGISTER

SUB ADDRESS = 18_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Reserved		0_B
6-0	Brightness Adjust	These bits control the brightness. They may have a value of +63 (“011 1111”) to -64 (“100 0000”), with positive values increasing brightness. A value of 0 (“000 0000”) has no effect on the data.	0000000_B

TABLE 25. CONTRAST REGISTER

SUB ADDRESS = 19_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Contrast Adjust	These bits control the contrast. They may have a value of 0x (“0000 0000”) to 1.992x (“1111 1111”). A value of 1x (“1000 0000”) has no effect on the data.	80_H

TABLE 26. HUE REGISTER

SUB ADDRESS = $1A_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Hue Adjust	These bits control the color hue. They may have a value of +30 degrees (“0111 1111”) to -30 degrees (“1111 1111”). A value of 0 degrees (“0000 0000”) has no effect on the color data.	00_H

TABLE 27. SATURATION REGISTER

SUB ADDRESS = $1B_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Saturation Adjust	These bits control the color saturation. They may have a value of 0x (“0000 0000”) to 1.992x (“1111 1111”). A value of 1x (“1000 0000”) has no effect on the color data. A value of 0x (“0000 0000”) disables the color information.	80_H

TABLE 28. COLOR GAIN REGISTER

SUB ADDRESS = $1C_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Color Gain Adjust	These bits control the amount of gain control for the color difference (CbCr) signals. They may have a value of 0.5x (“0010 0000”) to 3.98x (“1111 1111”). A value of 1x (“0100 0000”) has no effect on the data. This register is ignored unless the color gain control mode selection is “fixed gain control”.	40_H

TABLE 29. SHARPNESS REGISTER

SUB ADDRESS = $1E_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Reserved		00_B
5-0	Sharpness Adjust	These bits control the amount of gain control of high frequency luminance signals (either 2.6MHz or Fsc). They may have a value of +12dB (“11 1111”) to -12dB (“00 0100”). A value of 0dB (“01 0000”) has no effect on the data. This register is ignored if the sharpness mode selection is “disable sharpness control” or “reserved”.	010000_B

TABLE 30. HOST CONTROL REGISTER

SUB ADDRESS = $1F_H$			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Software Reset	When this bit is set to 1, the entire device except the I^2C bus is reset to a known state exactly like the $\overline{RESET}$ input going active. The software reset will initialize all register bits to their reset state. Once set this bit is self clearing after only 4 CLK periods. This bit is cleared on power-up by the external $\overline{RESET}$ pin.	0_B
6	Reserved		0_B
5	Closed Caption Odd Field Read Status	This bit is read-only. Data written to this bit is ignored. The bit is cleared when the caption data has been read out via the I^2C interface or as BT.656 ancillary data. 0 = No new caption data 1 = Caption_ODD_A and Caption_ODD_B data registers contain new data.	0_B
4	Closed Caption Even Field Read Status	This bit is read-only. Data written to this bit is ignored. The bit is cleared when the caption data has been read out via the I^2C interface or as BT.656 ancillary data. 0 = No new caption data 1 = Caption_EVEN_A and Caption_EVEN_B data registers contain new data.	0_B
3	WSS Odd Field Read Status	This bit is read-only. Data written to this bit is ignored. The bit is cleared when the WSS data has been read out via the I^2C interface or as BT.656 ancillary data. 0 = No new WSS data 1 = WSS_ODD_A and WSS_ODD_B data registers contain new data.	0_B
2	WSS Even Field Read Status	This bit is read-only. Data written to this bit is ignored. The bit is cleared when the WSS data has been read out via the I^2C interface or as BT.656 ancillary data. 0 = No new WSS data 1 = WSS_EVEN_A and WSS_EVEN_B data registers contain new data.	0_B
1-0	Reserved		00_B

TABLE 31. CLOSED CAPTION_ODD_A DATA REGISTER

SUB ADDRESS = 20_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Odd Field Caption Data	If odd field captioning is enabled and present, this register is loaded with the first eight bits of caption data on line 18, 21, or 22. Bit 0 corresponds to the first bit of caption information. Data written to this register is ignored.	80_H

TABLE 32. CLOSED CAPTION_ODD_B DATA REGISTER

SUB ADDRESS = 21_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
15-8	Odd Field Caption Data	If odd field captioning is enabled and present, this register is loaded with the second eight bits of caption data on line 18, 21, or 22. Data written to this register is ignored.	80_H

TABLE 33. CLOSED CAPTION_EVEN_A DATA REGISTER

SUB ADDRESS = 22_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Even Field Caption Data	If even field captioning is enabled and present, this register is loaded with the first eight bits of caption data on line 281, 284, or 335. Bit 0 corresponds to the first bit of caption information. Data written to this register is ignored.	80_H

TABLE 34. CLOSED CAPTION_EVEN_B DATA REGISTER

SUB ADDRESS = 23_H			
BIT NO.	FUNCTION	DESCRIPTION	RESET STATE
15-8	Even Field Caption Data	If even field captioning is enabled and present, this register is loaded with the second eight bits of caption data on line 281, 284, or 335. Data written to this register is ignored.	80_H

TABLE 35. WSS_ODD_A DATA REGISTER

SUB ADDRESS = 24_H			
BIT NO.	FUNCTION	DESCRIPTION	RESET STATE
7-0	Odd Field WSS Data	If odd field WSS is enabled and present, this register is loaded with the first eight bits of WSS information on line 17, 20, or 23. Bit 0 corresponds to the first bit of WSS information. Data written to this register is ignored.	00_H

TABLE 36. WSS_ODD_B DATA REGISTER

SUB ADDRESS = 25_H			
BIT NO.	FUNCTION	DESCRIPTION	RESET STATE
15-14	Reserved		00_B
13-8	Odd Field WSS Data	If odd field WSS is enabled and present, this register is loaded with the second six bits of WSS information on line 17, 20, or 23. Data written to this register is ignored.	000000_B

TABLE 37. WSS_CRC_ODD DATA REGISTER

SUB ADDRESS = 26_H			
BIT NO.	FUNCTION	DESCRIPTION	RESET STATE
7-6	Reserved		00_B
5-0	Odd Field WSS CRC Data	If odd field WSS is enabled and present during NTSC operation, this register is loaded with the six bits of CRC information on line 20. It is always a “000000” during PAL operation. Data written to this register is ignored.	000000_B

TABLE 38. WSS_EVEN_A DATA REGISTER

SUB ADDRESS = 27_H			
BIT NO.	FUNCTION	DESCRIPTION	RESET STATE
7-0	Even Field WSS Data	If even field WSS is enabled and present, this register is loaded with the first eight bits of WSS information on line 280, 283, or 336. Bit 0 corresponds to the first bit of WSS information. Data written to this register is ignored.	00_H

TABLE 39. WSS_EVEN_B DATA REGISTER

SUB ADDRESS = 28_H			
BIT NO.	FUNCTION	DESCRIPTION	RESET STATE
15-14	Reserved		00_B
13-8	Even Field WSS Data	If even field WSS is enabled and present, this register is loaded with the second six bits of WSS information on line 280, 283, or 336. Data written to this register is ignored.	000000_B

TABLE 40. WSS_CRC_EVEN DATA REGISTER

SUB ADDRESS = 29_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Reserved		00_B
5-0	Even Field WSS CRC Data	If even field WSS is enabled and present during NTSC operation, this register is loaded with the six bits of CRC information on line 283. It is always a “000000” during PAL operation. Data written to this register is ignored.	000000_B

TABLE 41. START H_BLANK LOW REGISTER

SUB ADDRESS = 30_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Assert $\overline{BLANK}$ Output Signal	This 8-bit register is cascaded with Start H_Blank High Register to form a 10-bit start_horizontal_blank REGISTER. It specifies the horizontal count (in 1x clock cycles) at which to assert $\overline{BLANK}$ each scan line. Bit 0 is always a “0”, so the start of horizontal blanking may only be done with two pixel resolution. The leading edge of $\overline{HSYNC}$ is count 000_H.	$4A_H$

TABLE 42. START H_BLANK HIGH REGISTER

SUB ADDRESS = 31_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
15-10	Reserved		000000_B
9-8	Assert $\overline{BLANK}$ Output Signal	This 2-bit register is cascaded with Start H_Blank Low Register to form a 10-bit start_horizontal_blank register. It specifies the horizontal count (in 1x clock cycles) at which to assert $\overline{BLANK}$ each scan line. The leading edge of $\overline{HSYNC}$ is count 000_H.	11_B

TABLE 43. END H_BLANK REGISTER

SUB ADDRESS = 32_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Negate $\overline{BLANK}$ Output Signal	This 8-bit register specifies the horizontal count (in 1x clock cycles) at which to negate $\overline{BLANK}$each scan line. Bit 0 is always a “0”, so the end of horizontal blanking may only be done with two pixel resolution. The leading edge of $\overline{HSYNC}$ is count 000_H.	$7A_H$

TABLE 44. START V_BLANK LOW REGISTER

SUB ADDRESS = 33_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Assert $\overline{BLANK}$ Output Signal	This 8-bit register is cascaded with Start V_Blank High Register to form a 9-bit start_vertical_blank register. It specifies the line number to assert $\overline{BLANK}$ each field. For NTSC operation, it occurs on line (n + 5) on odd fields and line (n + 268) on even fields. For PAL operation, it occurs on line (n + 5) on odd fields and line (n + 318) on even fields.	02_H

TABLE 45. START V_BLANK HIGH REGISTER

SUB ADDRESS = 34_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
15-9	Reserved		0000000_B
8	Assert $\overline{BLANK}$ Output Signal	This 1-bit register is cascaded with Start V_Blank Low Register to form a 9-bit start_vertical_blank register.	1_B

TABLE 46. END V_BLANK REGISTER

SUB ADDRESS = 35_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Negate $\overline{BLANK}$ Output Signal	This 8-bit register specifies the line number to negate $\overline{BLANK}$ each field. For NTSC operation, it occurs on line (n + 5) on odd fields and line (n + 268) on even fields. For PAL operation, it occurs on line (n + 5) on odd fields and line (n + 318) on even fields.	12_H

TABLE 47. END HSYNC REGISTER

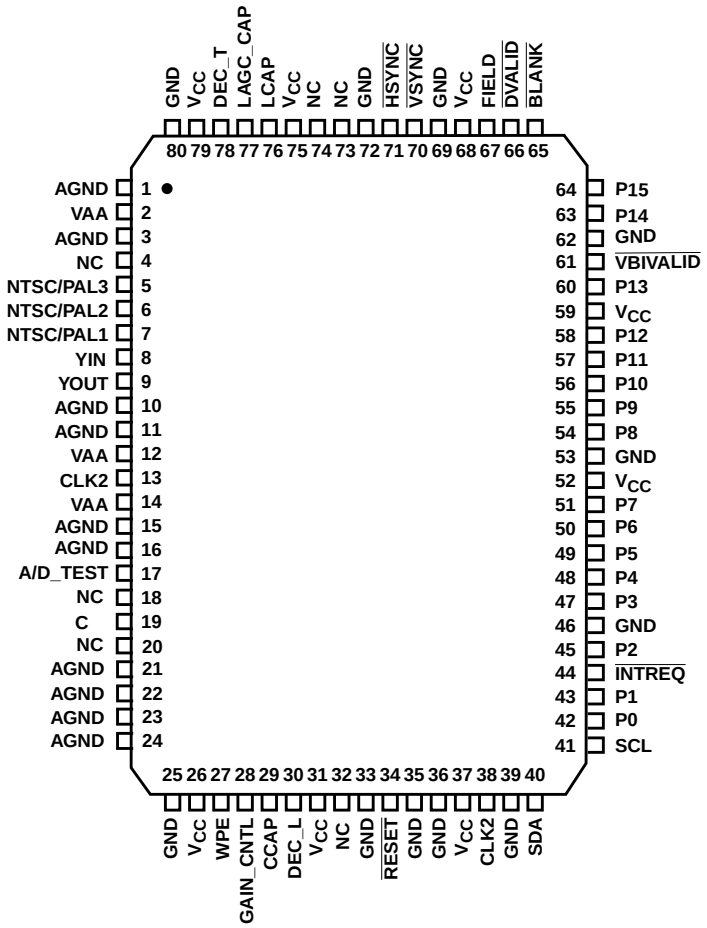
SUB ADDRESS = 36_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Negate $\overline{HSYNC}$ Output Signal	This 8-bit register specifies the horizontal count at which to negate $\overline{HSYNC}$ each scan line. Values may range from 0 (0000 0000) to 510 (1111 1111) CLK2 cycles. The leading edge of $\overline{HSYNC}$ is count 00_H.	40_H

TABLE 48. HSYNC DETECT WINDOW REGISTER

SUB ADDRESS = 37_H			
BIT NO.	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Horizontal Sync Detect Window	This 8-bit register specifies the width of the window (in 1x clock samples) to look for horizontal sync pulses each line. The window is centered about where the horizontal sync pulse should be located. If the horizontal sync pulse falls inside this window, the digital PLL will lock to it. If the horizontal sync pulse falls outside this window, the digital PLL is immediately reset to have the same timing. Recommend using a value of 20_H to optimize the response time of the digital PLL.	FF_H

Pinout

80 LEAD PQFP
TOP VIEW



Pin Description

PIN NAME	PIN NUMBER	INPUT/ OUTPUT	DESCRIPTION
P0-P15	42, 43, 45, 47-51, 54-58, 60, 63, 64	O	Pixel output pins. See Table 3.
$\overline{\text{HSYNC}}$	71	O	Horizontal sync output. $\overline{\text{HSYNC}}$ is asserted during the horizontal sync intervals. The polarity of $\overline{\text{HSYNC}}$ is programmable. This pin is three-stated after a $\overline{\text{RESET}}$ or software reset and should be pulled high through a 10K resistor.
$\overline{\text{VSYNC}}$	70	O	Vertical sync output. $\overline{\text{VSYNC}}$ is asserted during the vertical sync intervals. The polarity of $\overline{\text{VSYNC}}$ is programmable. This pin is three-stated after a $\overline{\text{RESET}}$ or software reset and should be pulled high through a 10K resistor.
FIELD	67	O	FIELD output. The polarity of FIELD is programmable. This pin is three-stated after a $\overline{\text{RESET}}$ or software reset and should be pulled high through a 10K resistor.
$\overline{\text{BLANK}}$	65	O	Composite blanking output. $\overline{\text{BLANK}}$ is asserted during the horizontal and vertical blanking intervals. The polarity of is programmable. This pin is three-stated after a $\overline{\text{RESET}}$ or software reset and should be pulled high through a 10K resistor.
$\overline{\text{DVALID}}$	66	O	Data valid output. $\overline{\text{DVALID}}$ is asserted during CLK2 cycles that contain valid pixel data. This pin is three-stated after a $\overline{\text{RESET}}$ or software reset and should be pulled high through a 10K resistor.
CLK2	38, 13	I	2x pixel clock inputs. All CLK2 pins must be connected together. This clock must be a continuous, free-running clock.
$\overline{\text{RESET}}$	34	I	Reset control input. A logical zero for a minimum of four CLK2 cycles resets the device. $\overline{\text{RESET}}$ must be a logical one for normal operation.
SDA	40	I/O	I^2C interface data input/output.
SCL	41	I	I^2C interface clock input.
WPE	27	I	White Peak Enable. When enabled (“1”), the video gain is reduced when the A/D output code exceeds 248. When disabled (“0”), the video amplifier will clip when the A/D output code reaches code 255.
$\overline{\text{VBIVALID}}$	61	O	Vertical Blanking Interval Valid output. $\overline{\text{VBIVALID}}$ is asserted during CLK2 cycles that contain valid VBI (Vertical Blanking Interval) data such as Closed Captioning, Teletext, and Wide Screen Signalling data. The polarity of $\overline{\text{VBIVALID}}$ is programmable. This pin is three-stated after a $\overline{\text{RESET}}$ or software reset and should be pulled high through a 10K resistor.
$\overline{\text{INTREQ}}$	44	O	Interrupt Request Output. This is an open-drain output and requires an external 10K pull-up resistor to V_{CC}.
NTSC/PAL 1	7	I	Composite Video Input. This input must be AC-coupled to the video signal (using a 1µF capacitor) and terminated with a 75Ω resistor, as shown in the Applications section. These components should be as close to this pin as possible for best performance. If not used, this pin should be connected to AGND through a 0.1µF capacitor.
NTSC/PAL 2	6	I	Composite Video Input. This input must be AC-coupled to the video signal (using a 1µF capacitor) and terminated with a 75Ω resistor, as shown in the Applications section. These components should be as close to this pin as possible for best performance. If not used, this pin should be connected to AGND through a 0.1µF capacitor.
NTSC/PAL 3 (Y)	5	I	Composite video or Luminance (Y) video input. This input must be AC-coupled to the video signal (using a 1µF capacitor) and terminated with a 75Ω resistor, as shown in the Applications section. These components should be as close to this pin as possible for best performance. If not used, this pin should be connected to AGND through a 0.1µF capacitor.

Pin Description (Continued)

PIN NAME	PIN NUMBER	INPUT/ OUTPUT	DESCRIPTION
C	19	I	Chrominance (C) video input. This input must be AC-coupled to the video signal (using a 1µF capacitor) and terminated with a 75Ω resistor, as shown in the Applications section. These components, and the corresponding anti-aliasing lowpass filter, should be as close to this pin as possible for best performance. If not used, this pin should be connected to AGND through a 0.1µF capacitor.
YOUT	9	O	Analog output of the video multiplexer. This output should be lowpass filtered and input via the YIN pin, as shown in the Applications section. The anti-aliasing lowpass filter should be as close to YOUT and YIN as possible for best performance.
YIN	8	I	Analog input to the ADC.
GAIN_CTRL	28	I	Gain Control Input. A DC voltage is used to set the video amplifier's gain, as shown in Figure 2. The reference circuit should be as close to this pin as possible for best performance.
DEC_T	78	I	Decoupling for A/D Converter Reference. A 0.1µF capacitor should be connected between this pin and AGND, as shown in the Applications section. This capacitor should be as close to this pin as possible for best performance.
DEC_L	30	I	Decoupling for A/D Converter Reference. A 0.1µF capacitor should be connected between this pin and AGND, as shown in the Applications section. This capacitor should be as close to this pin as possible for best performance.
LAGC_CAP	77	I	Capacitor connection for Luminance AGC Circuit. Controls the AGC loop time constant. A 0.01µF capacitor should be connected between this pin and AGND, as shown in the Applications section. This capacitor should be as close to this pin as possible for best performance.
LCAP	76	I	Capacitor connection for Luminance Clamp Circuit. Controls the clamp loop time constant. A 0.047µF capacitor should be connected between this pin and AGND, as shown in the Applications section. This capacitor should be as close to this pin as possible for best performance.
CCAP	29	I	Capacitor connection for Chrominance Clamp Circuit. Controls the clamp loop time constant. A 0.047µF capacitor should be connected between this pin and AGND, as shown in the Applications section. This capacitor should be as close to this pin as possible for best performance.
V_{CC}	26, 31,37, 52, 59, 68, 75, 79	I	Digital power supply pins. All V_{CC} pins must be connected together.
GND	25, 33, 35, 36, 39, 46, 53, 62, 69, 72, 80	I	Digital ground pins. All GND pins must be connected together.
VAA	2, 12,14	I	Analog power supply pins. All VAA pins must be connected together.
AGND	1, 3, 10, 11, 15,16, 21, 22, 23, 24	I	Analog ground pins. All AGND pins must be connected together.
A/D TEST	17	O	A/D test pin. This pin must be left floating for proper operation.
NC	4, 18, 20, 32, 73, 74		No Connect pins. These pins must be left floating for proper operation.

Applications Information

PCB LAYOUT CONSIDERATIONS

A PCB board with a minimum of 4 layers is recommended, with layers 1 and 4 (top and bottom) for signals and layers 2 and 3 for power and ground. The PCB layout should implement the lowest possible noise on the power and ground planes by providing excellent decoupling.

The optimum layout places the HMP8115 as close as possible to the power supply connector and the video input connector.

Component Placement

External components should be positioned as close as possible to the appropriate pin, ideally such that traces can be connected point to point. Chip capacitors are recommended where possible, with radial lead ceramic capacitors the second-best choice.

Power supply decoupling should be done using a 0.1µF ceramic capacitor in parallel with a 0.01µF chip capacitor for each group of V_{AA} and V_{CC} pins to ground. These capacitors should be located as close to the power and ground pins as possible, using short, wide traces.

Digital Ground Plane

All GND pins on the HMP8115 should be connected to the digital ground plane of the board.

Analog Ground Plane

A separate analog ground plane for the HMP8115 is recommended. All AGND pins on the HMP8115 should be connected to the analog ground plane. This analog ground plane should be connected to the board's digital ground plane at a single point.

Analog Power Plane

The HMP8115 should have its own V_{AA} power plane that is isolated from the common power plane of the board, with a gap between the two power planes of at least 1/8 inch. All V_{AA} pins on the HMP8115 must be connected to this analog power plane. The analog power plane should be connected to the board's normal V_{CC} power plane at a single point though a low-resistance ferrite bead, such as a Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001. The ferrite bead provides resistance to switching currents, improving the performance of HMP8115. A single 47µF capacitor should also be used between the analog power plane and the ground plane to control low-frequency power supply ripple.

If a separate linear regulator is used to provide power to the analog power plane, the power-up sequence should be designed to ensure latchup will not occur. A separate linear regulator is recommended if the power supply noise on the V_{AA} pins exceeds 200mV.

Analog Signals

Traces containing digital signals should not be routed over, under, or adjacent to the analog output traces to minimize crosstalk. If this is not possible, coupling can be minimized by routing the digital signals at a 90 degree angle to the analog signals. The analog input traces should also not overlay the V_{AA} power plane to maximize high-frequency power supply rejection.

EVALUATION BOARD

HMPVIDEVAL/ISA

The HMPVIDEVAL/ISA evaluation board allows connecting the HMP8115 into a PC ISA slot for evaluation. It includes the HMP8115 NTSC/PAL decoder, 3MB of VRAM, and a NTSC/PAL encoder. The board accepts composite or S-video input and displays video on a standard TV. The ISA bus and evaluation software allow easy performance evaluation of the HMP8115 using tools such as the Tektronix VM700 video test system.

RELATED APPLICATION NOTES

Application Notes are also available on the Intersil Multimedia web site at http://www.semi.harris.com/mmedia.

AN9644: Composite Video Separation Techniques

AN9716: Widescreen Signalling (WSS)

AN9717: YCbCr to RGB Considerations

AN9728: BT.656 Video Interface for ICs

AN9738: Video Module Interface (VMI) for ICs

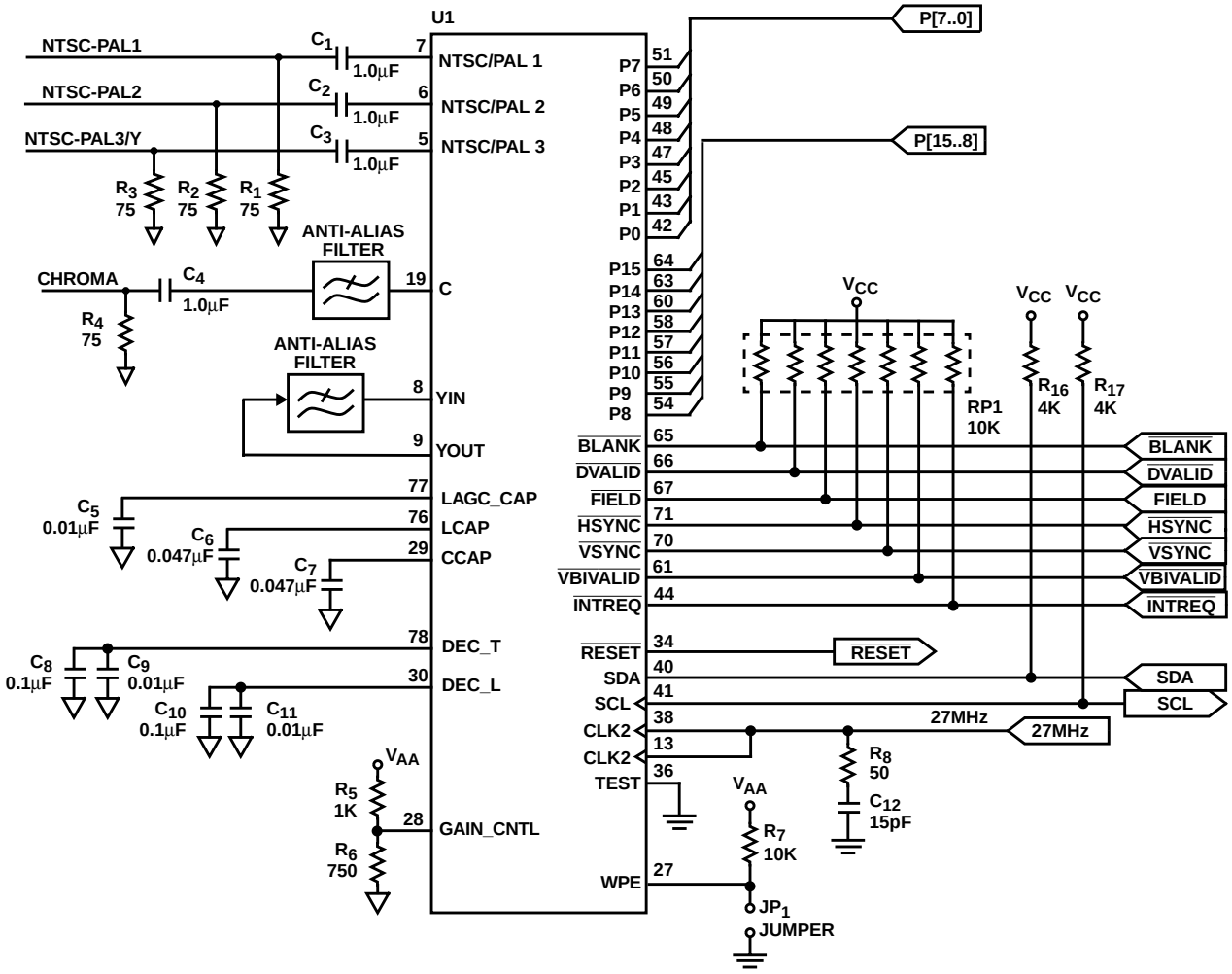


FIGURE 22. HMP8115 REFERENCE SCHEMATICS

Absolute Maximum Ratings

Digital Supply Voltage (V_{CC} to GND) 7.0V
Analog Supply Voltage (VAA to GND) 7.0V
Digital Input Voltages . . . . . GND - 0.5V to V_{CC} + 0.5V
ESD Classification . . . . . Class 1

Operating Temperature Range

HMP8115CN . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, See Note 42) θ_{JA} ($^oC/W$)
PQFP Package 42
Maximum Power Dissipation
HMP8115CN 1.9W
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Junction Temperatures . . . . . 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

42. θ_{JA} is measured with the component mounted on an evaluation PC board in free air. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Electrical Specifications

$V_{CC} = V_{AA} = 5.0V$, $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
POWER SUPPLY CHARACTERISTICS						
Power Supply Voltage Range	V_{CC}, V_{AA}	(Note 43)	4.75	5	5.25	V
Total Power Supply Current	I_{TOT}	CLK2 = 29.5MHz, V_{CC} = VAA = 5.25V Outputs Not Loaded	-	280	315	mA
Digital Power Supply Current	I_{CC}		-	105	115	mA
Analog Power Supply Current	I_{AA}		-	175	200	mA
Total Power Dissipation	P_{TOT}	CLK2 = 29.5MHz, V_{CC} = VAA = 5.25V, Outputs Not Loaded	-	1.47	1.66	W
DC CHARACTERISTICS: DIGITAL I/O (EXCEPT CLK2 and I^2C INTERFACE)						
Input Logic High Voltage	V_{IH}	V_{CC} = Max	2.0	-	-	V
Input Logic Low Voltage	V_{IL}	V_{CC} = Min	-	-	0.8	V
Output Logic High Voltage	V_{OH}	I_{OH} = -4mA, V_{CC} = Max	2.4	-	-	V
Output Logic Low Voltage	V_{OL}	I_{OL} = 4mA, V_{CC} = Min	-	-	0.4	V
Input Leakage Current	I_{IH}, I_{IL}	V_{CC} = Max Input = 0V or 5V	-	-	10	µA
Input/Output Capacitance	C_{IN}, C_{OUT}	f = 1MHz, (Note 43) All Measurements Referenced to Ground, $T_A = 25^oC$	-	8	-	pF
Three-State Output Current Leakage	I_{OZ}		-	-	10	µA
DC CHARACTERISTICS: CLK2 DIGITAL INPUT						
Input Logic High Voltage	V_{IH}	V_{CC} = Max	0.7xV_{CC}	-	-	V
Input Logic Low Voltage	V_{IL}	V_{CC} = Min	-	-	0.3xV_{CC}	V
Input Leakage Current	I_{IH}	V_{CC} = Max Input = 0V or V_{CC}	-	-	10	µA
	I_{IL}		- 450	-	-	µA
Input Capacitance	C_{IN}	CLK2 = 1MHz, (Note 43) All Measurements Referenced to Ground, $T_A = 25^oC$	-	8	-	pF

Electrical Specifications $V_{CC} = V_{AA} = 5.0V$, $T_A = 25^oC$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS: I^2C INTERFACE						
Input Logic High Voltage	V_{IH}	V_{CC} = Max	$0.7xV_{CC}$	-	-	V
Input Logic Low Voltage	V_{IL}	V_{CC} = Min	-	-	$0.3xV_{CC}$	V
Output Logic High Voltage	V_{OH}	I_{OH} = -1mA, V_{CC} = Max	3.0	-	-	V
Output Logic Low Voltage	V_{OL}	I_{OL} = 3mA, V_{CC} = Min	0	-	0.4	V
Input Leakage Current	I_{IH}, I_{IL}	V_{CC} = Max Input = 0V or 5V	-	-	10	µA
Input/Output Capacitance	C_{IN}, C_{OUT}	SCL = 400kHz, (Note 43) All Measurements Referenced to GND, $T_A = 25^oC$	-	8	-	pF
AC CHARACTERISTICS: DIGITAL I/O (EXCEPT I^2C INTERFACE)						
CLK2 Frequency			20	-	29.5	MHz
CLK2 Waveform Symmetry		(Note 43)	40	-	60	%
CLK2 Pulse Width High	t_{PWH}		13	-	-	ns
CLK2 Pulse Width Low	t_{PWL}		13	-	-	ns
Data and Control Setup Time	t_{SU}	(Note 44)	10	-	-	ns
Data and Control Hold Time	t_{HD}		0	-	-	ns
CLK2 to Output Delay	t_{DVLD}		0	5	8	ns
Data and Control Rise/Fall Time	t_r, t_f	(Note 43)	-	2	6	ns
AC CHARACTERISTICS: I^2C INTERFACE						
SCL Clock Frequency	f_{SCL}		0	-	400	kHz
SCL Pulse Width Low	t_{LOW}		1.3	-	-	µs
SCL Pulse Width High	t_{HIGH}		0.6	-	-	µs
Data Hold Time	$t_{HD:DATA}$		0	-	-	ns
Data Setup Time	$t_{SU:DATA}$		100	-	-	ns
SDA, SCL Rise Time	t_R	(Note43)	-	-	300	ns
SDA, SCL Fall Time	t_F		-	-	300	ns
ANALOG INPUT PERFORMANCE						
Composite Video Input Amplitude (Sync Tip to White Level)		Input Termination of 75Ω and 1.0µF AC-Coupled	0.5	1.0	2.0	V_{P-P}
Luminance (Y) Video Input Amplitude (Sync Tip to White Level)		Input Termination of 75Ω and 1.0µF AC-Coupled	0.5	1.0	2.0	V_{P-P}
Chrominance (C) Video Input Amplitude (Burst Amplitude)		Input Termination of 75Ω and 1.0µF AC-Coupled, (Note 43)	0.143	0.286	0.6	V_{P-P}
Video Input Impedance	R_{AIN}	Note 43	200	-	-	kΩ

Electrical Specifications $V_{CC} = V_{AA} = 5.0V$, $T_A = 25^oC$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Video Input Bandwidth	BW	$1V_{P-P}$ Sine Wave Input to -3dBc Reduction, (Note 43)	5	-	-	MHz
ADC Input Range	A_{IN} FULL SCALE		-	1	-	V_{P-P}
	A_{IN} OFFSET		-	1.5	-	V
ADC Integral Nonlinearity	INL	Best Fit Linearity	-	2	-	LSB
ADC Differential Nonlinearity	DNL		-	0.35	-	LSB
VIDEO PERFORMANCE						
Differential Gain	DG	Modulated Ramp (Note 43)	-	2	-	%
Differential Phase	DP		-	1	-	Deg.
Hue Accuracy		75% Color Bars (Note 43)	-	2	-	Deg.
Color Saturation Accuracy			-	2	-	%
Luminance Nonlinearity		NTC-7 Composite (Note 43)	-	2	-	%
SNR	$SNRL_{WEIGHTED}$	Pedestal Input (Note 43)	-	50	-	dB
GENLOCK PERFORMANCE						
Horizontal Locking Time	t_{LOCK}	Time from Initial Lock Acquisition to an Error of 1 Pixel. (Note 43)	2	3	-	Fields
Long-Term horizontal Sync Lock Range		Range over specified pixel jitter is maintained. Assumes line time changes by amount indicated slowly between over one field. (Note 43)	-	-	5	%
Number of Missing Horizontal Syncs Before Lost Lock Declared	$H_{SYNC\ LOST}$	Programmable via register 04_H (Note 43)	1 or 12	1 or 12	1 or 12	Hsyncs
Number of Missing Vertical Syncs Before Lost Lock Declared	$V_{SYNC\ LOST}$		1 or 3	1 or 3	1 or 3	Vsyncs
Long-Term Color Subcarrier Lock Range		Range over color subcarrier locking time and accuracy specifications are maintained. Subcarrier frequency changes by amount indicated slowly over 24 hours. (Note 43)	-	±200	±400	Hz
Vertical Sample Alignment		(Notes 43, 45)	-	1/8	-	Pixel
			-	10	-	ns

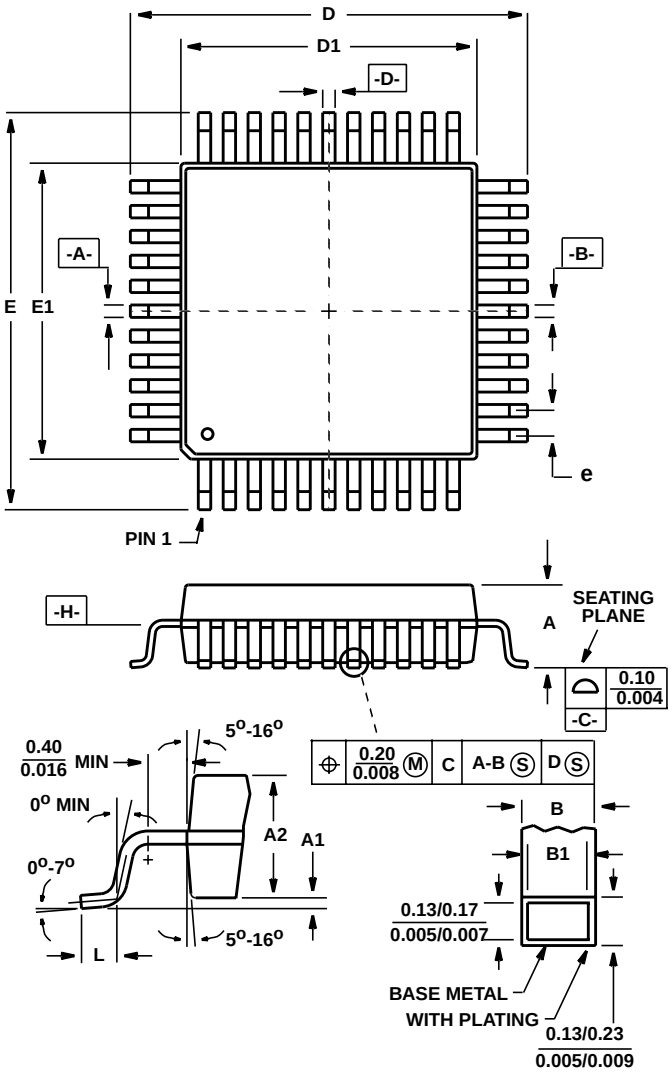
NOTES:

43. Guaranteed by design or characterization.

44. Test performed with $C_L = 40pF$, $I_{OL} = 4mA$, $I_{OH} = -4mA$. Input reference level is 1.5V for all inputs. $V_{IH} = 3.0V$, $V_{IL} = 0V$.

45. This should not be confused with Clock Jitter, since the HMP8115 does not generate the sample clock. Thus, clock jitter is solely dependent on the source of the CLK2 signal. The Vertical Sample Alignment parameter specifies how accurately samples align vertically from one scan line to the next.

Metric Plastic Quad Flatpack Packages (MQFP/PQFP)



Q80.14x20 (JEDEC MO-108CB-1 ISSUE A)
80 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.134	-	3.40	-
A1	0.010	-	0.25	-	-
A2	0.100	0.120	2.55	3.05	-
B	0.012	0.018	0.30	0.45	6
B1	0.012	0.016	0.30	0.40	-
D	0.904	0.923	22.95	23.45	3
D1	0.783	0.791	19.90	20.10	4, 5
E	0.667	0.687	16.95	17.45	3
E1	0.547	0.555	13.90	14.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	80		80		7
e	0.032 BSC		0.80 BSC		-
ND	24		24		-
NE	16		16		-

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NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. “N” is the number of terminal positions.

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For information regarding Intersil Corporation and its products, see web site **http://www.intersil.com**

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029