FLASH-ROM MODULE 16MByte (4M x 32-Bit) ,72pin-SODIMM, 3.3V Part No. HMF4M32B8VG

GENERAL DESCRIPTION

The HMF4M32B8VG is a high-speed flash read only memory (FROM) module containing 4,194,304 words organized in a x32bit configuration. The module consists of eight 2M x 8 FROM mounted on a 72-pin, single-sided, FR4-printed circuit board. Commands are written to the command register using standard microprocessor write timings.
Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other flash or EPROM devices.
Output enable (/OE) and write enable (/WE) can set the memory input and output.
When FROM module is disable condition the module is becoming power standby mode, system designer can get low-power design. All module components may be powered from a single +3.0V DC power supply.

FEATURES

- Access time : 90, 100 and 120ns
- High-density 16MByte design
- High-reliability, low-power design
- Single + 3V ± 0.3V power supply
- Easy memory expansion
- Hardware reset pin(RESET#)
- FR4-PCB design
- Low profile 72-pin SODIMM
- Minimum 100,000 write/erase cycle
- Flexible sector architecture
- Embedded algorithms
- Erase suspend / Erase resume

OPTIONS MARKING

- Timing

80ns access	-80
90ns access	-90
120ns access	-120

- Packages

72-pin SODIMM	B

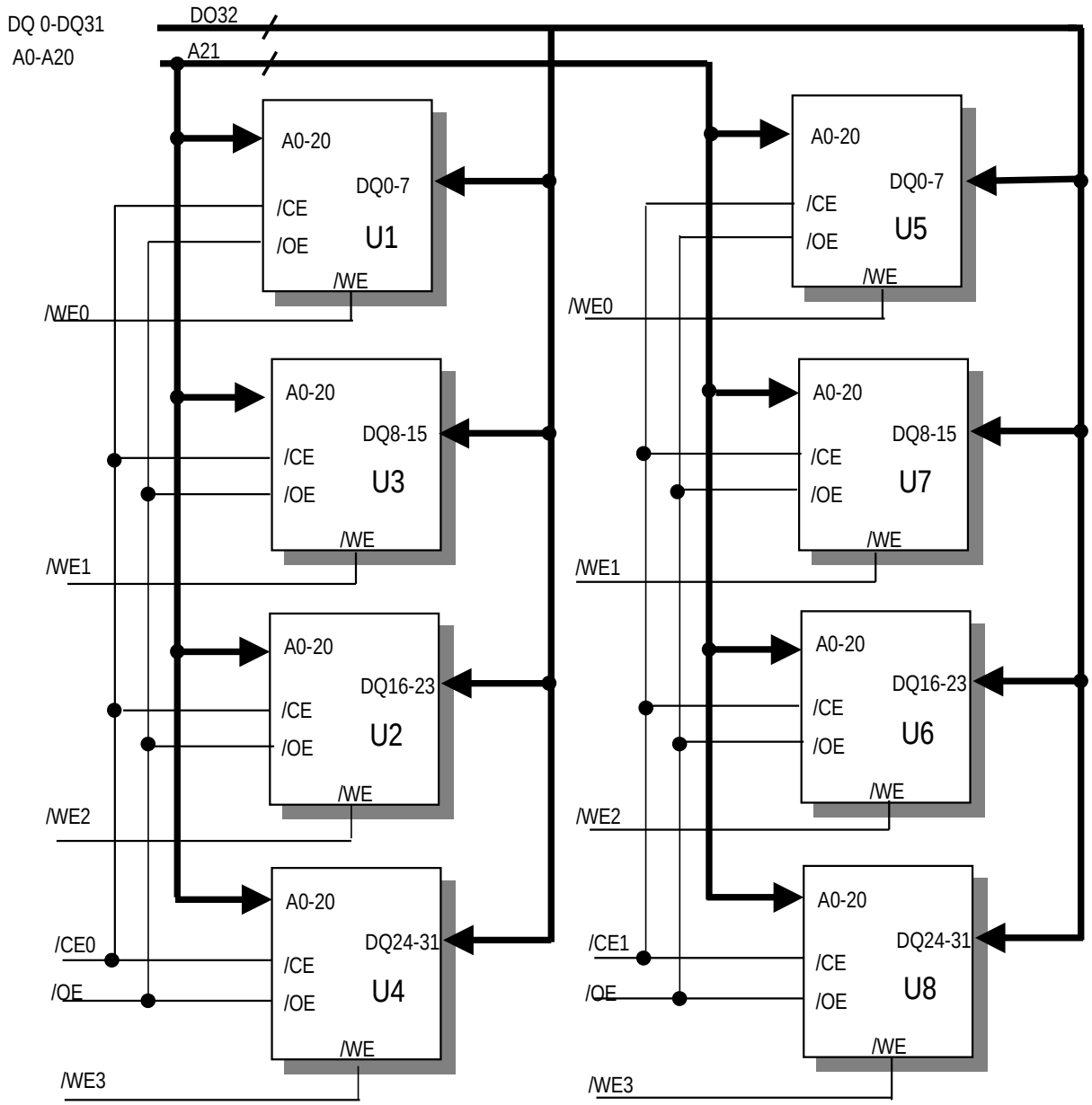
PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	25	DQ22	49	DQ8
2	DQ0	26	DQ7	50	DQ24
3	DQ16	27	DQ23	51	DQ9
4	DQ1	28	A7	52	DQ25
5	DQ17	29	A12	53	DQ10
6	DQ2	30	Vcc	54	DQ26
7	DQ18	31	A8	55	DQ11
8	DQ3	32	A9	56	DQ27
9	DQ19	33	/WE3	57	DQ12
10	Vcc	34	/WE2	58	DQ28
11	A10	35	A13	59	Vcc
12	A0	36	A14	60	DQ29
13	A1	37	A15	61	DQ13
14	A2	38	A16	62	DQ30
15	A3	39	Vss	63	DQ14
16	A4	40	/CE0	64	DQ31
17	A5	41	/CE2	65	DQ15
18	A6	42	/CE3	66	A19
19	A11	43	/CE1	67	VSS(PD1)
20	DQ4	44	/WE0	68	VSS(PD2)
21	DQ20	45	/WE1	69	VSS(PD3)
22	DQ5	46	A17	70	/RESET
23	DQ21	47	/OE	71	A20
24	DQ6	48	A18	72	Vss

72-PIN SODIMM

TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	/OE	/CE	/WE	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
READ	L	L	H	Dout	ACTIVE
WRITE or ERASE	H	L	L	Din	ACTIVE

NOTE: X means don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5V to +4.0V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5V to +4.0V
Power Dissipation	P_D	8W
Storage Temperature	T_{STG}	-65°C to +150°C
Operating Temperature	T_A	-40°C to +85°C

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of th e device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP.	MAX
Supply Voltage	V_{CC}	2.7V	-	3.6V
Ground	V_{SS}	0	0	0
Input High Voltage	V_{IH}	0.7xV_{CC}	-	Vcc+0.3V
Input Low Voltage	V_{IL}	-0.5	-	0.8V

DC CHARACTERISTICS (CMOS Compatible)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LI}	Input Leakage Current	V_{IN}=Vss to Vcc, Vcc=Vcc max	-1.0		+1.0	uA
I_{LIT}	A9 , /RESET Input Leakage Current	Vcc= Vcc max ; A9,/RESET=12.5V			35	uA
I_{LO}	Output Leakage Current	V_{OUT}= Vss to Vcc, Vcc= Vcc max	-1.0		+1.0	uA

I_{CC1}	Vcc Active Read Current (Note1)	/CE=V_{IL}, /OE=V_{IL} All Outputs open	5MHZ		9	16	mA
			1MHZ		2	4	
I_{CC2}	Vcc Active Write Current (Note 2 and 4)	/CE=V_{IL}, /OE=V_{IH}			20	30	mA
I_{CC3}	Vcc Standby Current	Vcc=Vcc max ; /CE,Reset=Vcc±0.3V			0.2	5	uA
I_{CC4}	Vcc Standby Current During Reset	Vcc=Vcc max ; /Reset=Vcc±0.3V			0.2	5	uA
I_{CC5}	Automatic Sleep Mode(Note3)	V_{IH}=Vcc±0.3V; V_{IL}=Vss±0.3V			0.2	5	uA
V_{IL}	Input Low Voltage			-0.5		0.8	V
V_{IH}	Input High Voltage			0.7xVcc		Vcc+0.3	V
V_{ID}	Voltage for Autoselect and Temporary Unprotect	Vcc=3.3V		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL}=4.0mA, Vcc=Vcc min				0.45	V
V_{OH1}	Output High Voltage	I_{OH}=-2.0mA, Vcc=Vcc min		0.85xVcc			V
V_{OH2}		I_{OH}=-100uA, Vcc= Vcc min		Vcc-0.4			V
V_{LKO}	Low Vcc Lock-Out Voltage			2.3		2.5	V

Notes :

1. The Icc current listed includes both the DC operating current ane the frequency dependent component(at 5 MHz). The read current is typically 9mA (@VCC=3.0V. /OE at V_{1H})
2. Icc active while Embedded Erase or Embedded Program is progress.
3. Automatic sleep mode enables the low power mode when adder sses remain stable for t_{ACC}+30ns. Typical sleep mode current is 200nA.
4. Not 100% tested.

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER		TYP	MAX	UNIT	COMMENTS
Block Erase Time		0.7	15	sec	Excludes 00h programming prior to erasure
Chip Erase Time		25	-	sec	
Byte Programming Time		9	300	us	Excludes system level overhead
Word Programming Time		11	360	us	
Chip Programming Time	Byte Mode	18	54	sec	
	Word Mode	12	36	sec	

Notes :

1. 25^{O}C, Vcc=3.0V, 100,000 cycles, typical pattern.
2. System-level overhead is defined as the time required to excute the four-bus-cycle command necessary to program

each byte. In the preprogramming step of the internal Erase Routine, all bytes are programmed to 00H before erasure.

CAPACITANCE

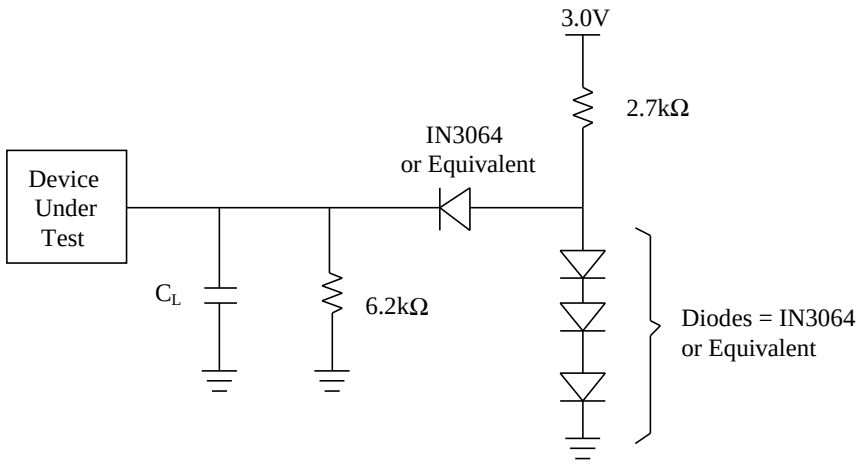
PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST SETUP	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0V	7.5	9	pF

Notes :

1. Sampled, not 100% tested
2. Test conditions T_A = 25° C, f=1.0 MHz, VCC=3.3V.

TEST SPECIFICATIONS

TEST CONDITION	VALUE	UNIT
Output load	1TTL gate and C_L=100pF	
Input rise and full times	5	ns
Input pulse levels	0.0 - 3.0	V
Input timing measurement reference levels	1.5	V
Output timing measurement reference levels	1.5	V



Note : C_L = 100pF including jig capacitance

AC CHARACTERISTICS

u Erase / Program Operations

PARAMETER SYMBOLS		DESCRIPTION	C_L=100Pf						UNIT
			-80		-90		-120		
JEDEC	STANDARD		Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	80		90		120		ns
t_{AVWL}	t_{AS}	Address Setup Time	0		0		0		ns
t_{WLAX}	t_{AH}	Address Hold Time	45		45		50		ns
t_{DVWH}	t_{DS}	Data Setup Time	35		45		50		ns
t_{WHDX}	t_{DH}	Data Hold Time	0		0		0		ns
	t_{OES}	Output Enable Setup Time	0		0		0		ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write	0		0		0		ns
t_{ELWL}	t_{CS}	/CE Setup Time	0		0		0		ns
t_{WHEH}	t_{CH}	/CE Hold Time	0		0		0		ns
t_{WLWH}	t_{WP}	Write Pulse Width	35		35		50		ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	30		30		30		ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	9		9		9		µs
t_{WHWH2}	t_{BERS}	Block Erase Operation	0.7		0.7		0.7		sec
	t_{VCS}	Vcc Setup Time	50		50		50		µs
	t_{RB}	Recovery time from RY/BY	0		0		0		ns
	t_{BUSY}	Program/Erase Valid to RY/BY Delay	90		90		90		ns

Note:

1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more Information

u Alternate /CE Controlled Erase/ Program Operations

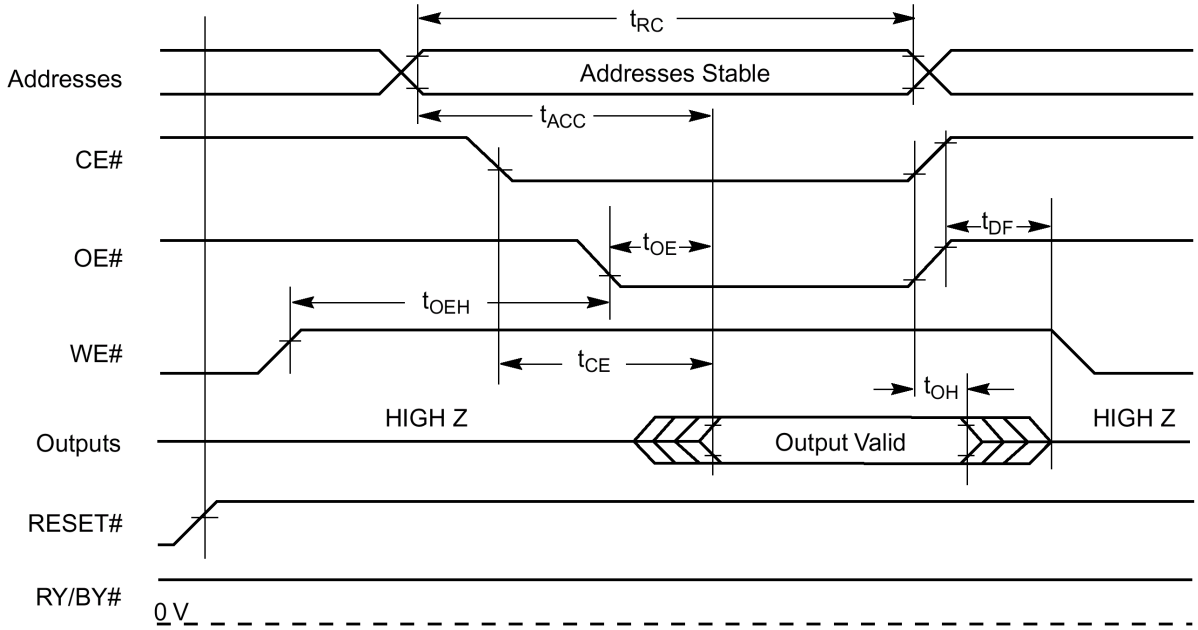
PARAMETER SYMBOLS		DESCRIPTION	C_L=100pF						UNIT
			-80		-90		-120		
JEDEC	STANDARD		Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	80		90		120		ns
t_{AVEL}	t_{AS}	Address Setup Time	0		0		0		ns
t_{ELAX}	t_{AH}	Address Hold Time	45		45		50		ns
t_{DVEH}	t_{DS}	Data Setup Time	35		45		50		ns
t_{EHDX}	t_{DH}	Data Hold Time	0		0		0		ns
	t_{OES}	Output Enable Setup Time	0		0		0		ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write	0		0		0		ns
t_{WLEL}	t_{WS}	/OE High to /WE Low	0		0		0		ns
t_{EHWH}	t_{WH}	/WE Hold Time	0		0		0		ns

t_{ELEH}	t_{CP}	/CE Pulse Width	35		35		50		ns
t_{EHEL}	t_{CPH}	/CE Pulse Width High	30		30		30		ns
	t_{BUSY}	Program/Erase Valid RY//BY Delay	90		90		90		ns
	t_{RB}	Recovery Time from RY//BY	0		0		0		ns

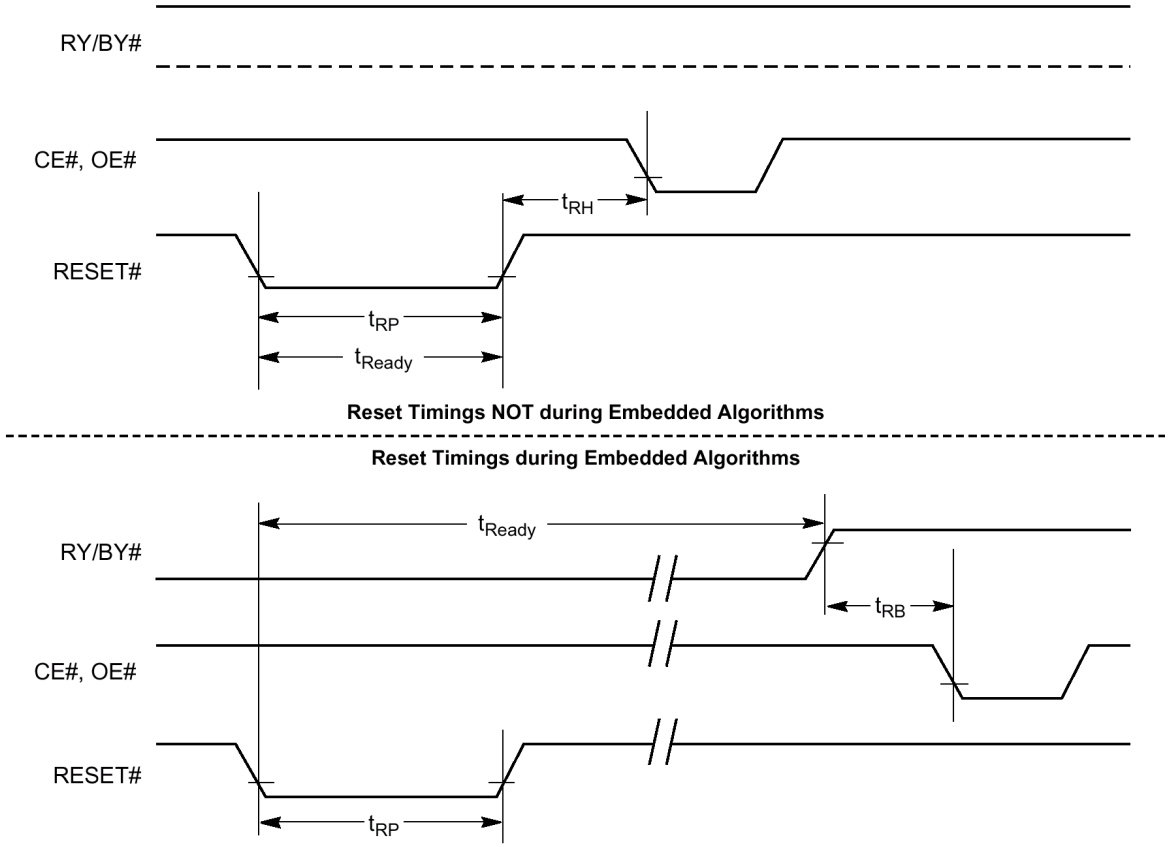
Note:

1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more Information .

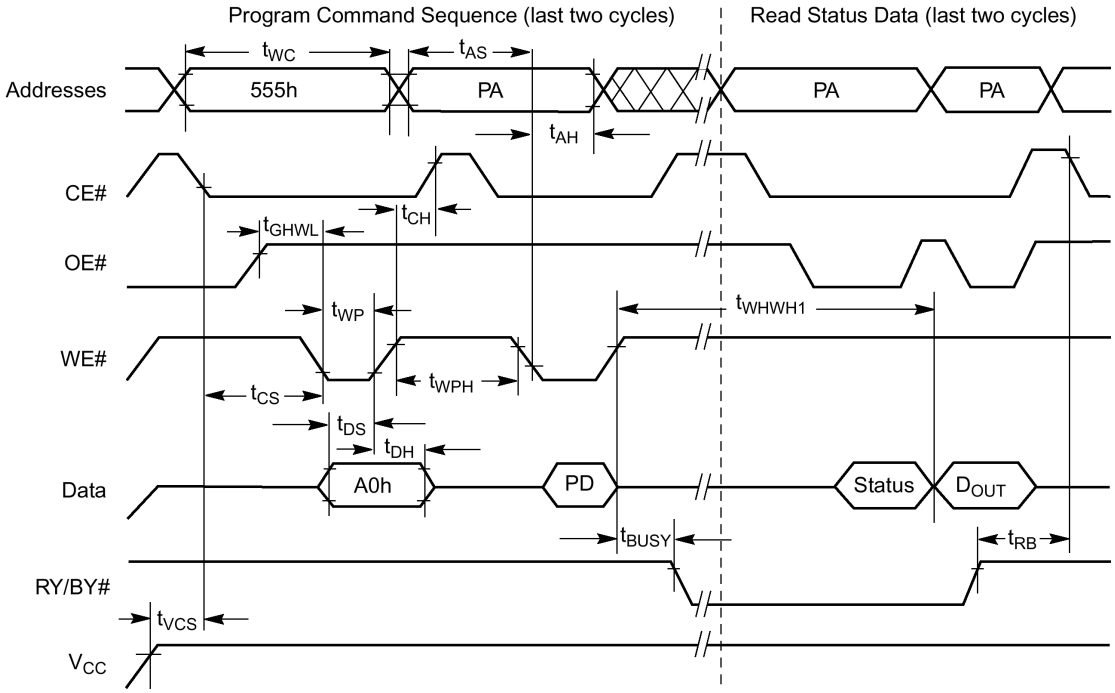
u READ OPERATIONS TIMING



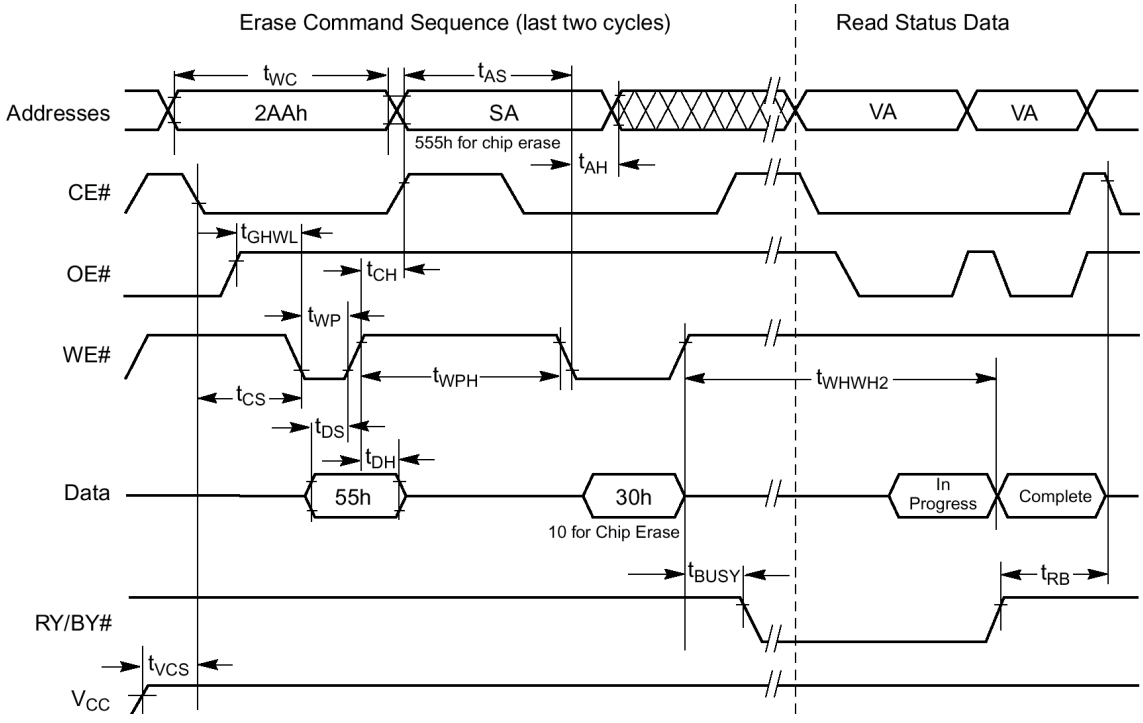
u RESET TIMING



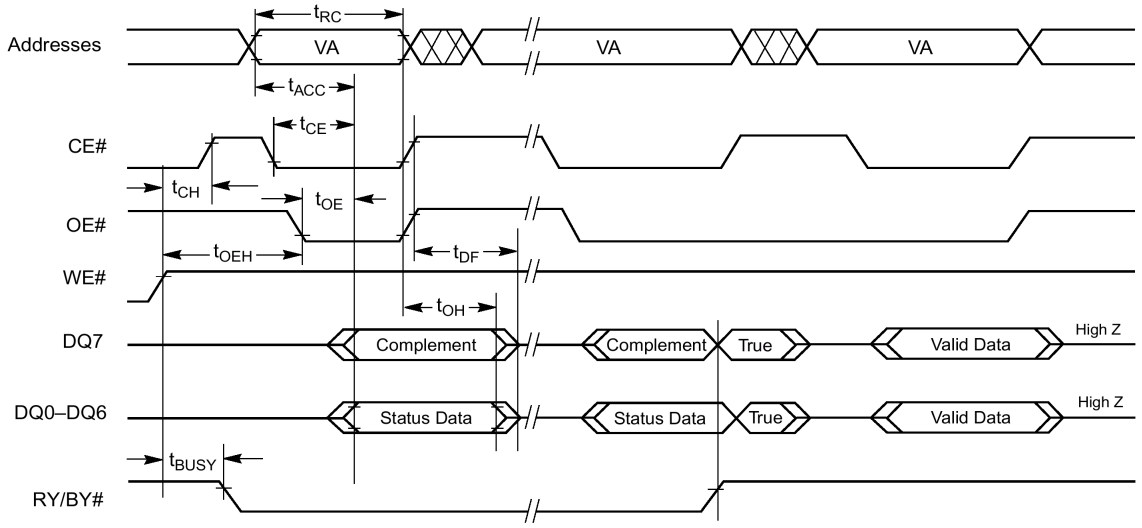
u PROGRAM OPERATIONS TIMING



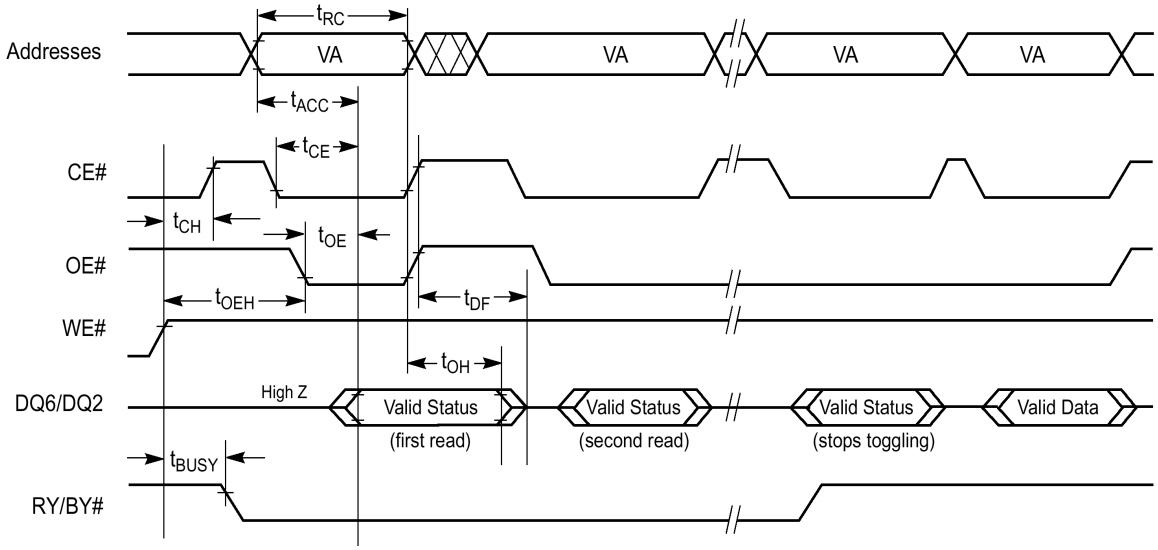
u CHIP/SECTOR ERASE OPERATION TIMINGS



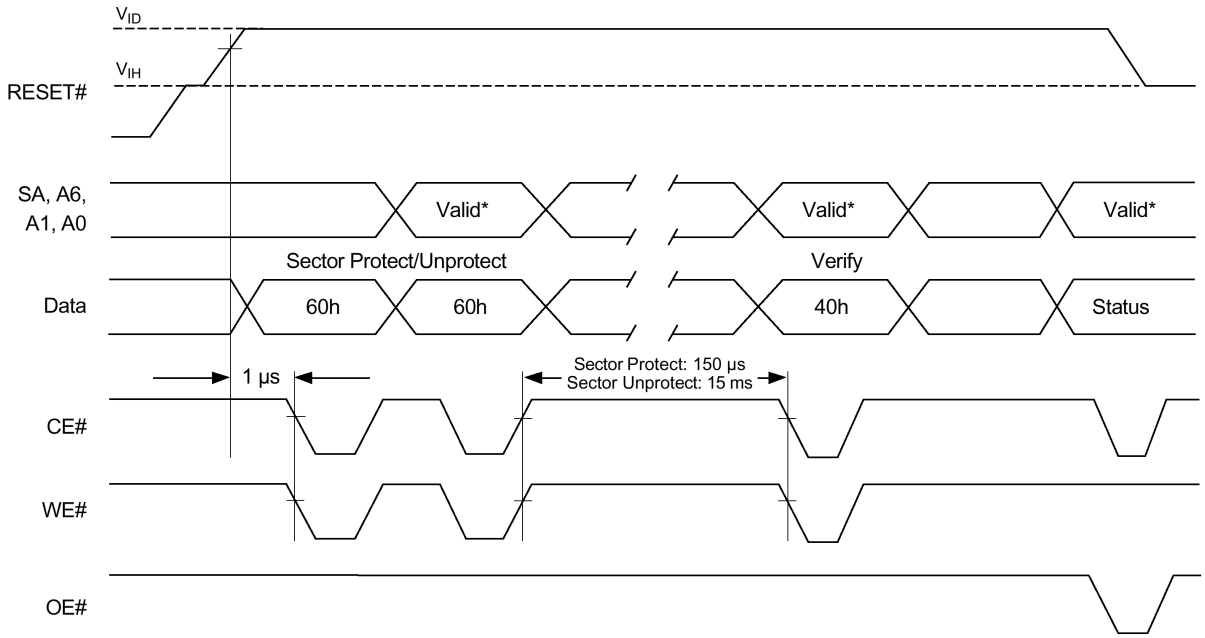
u DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)



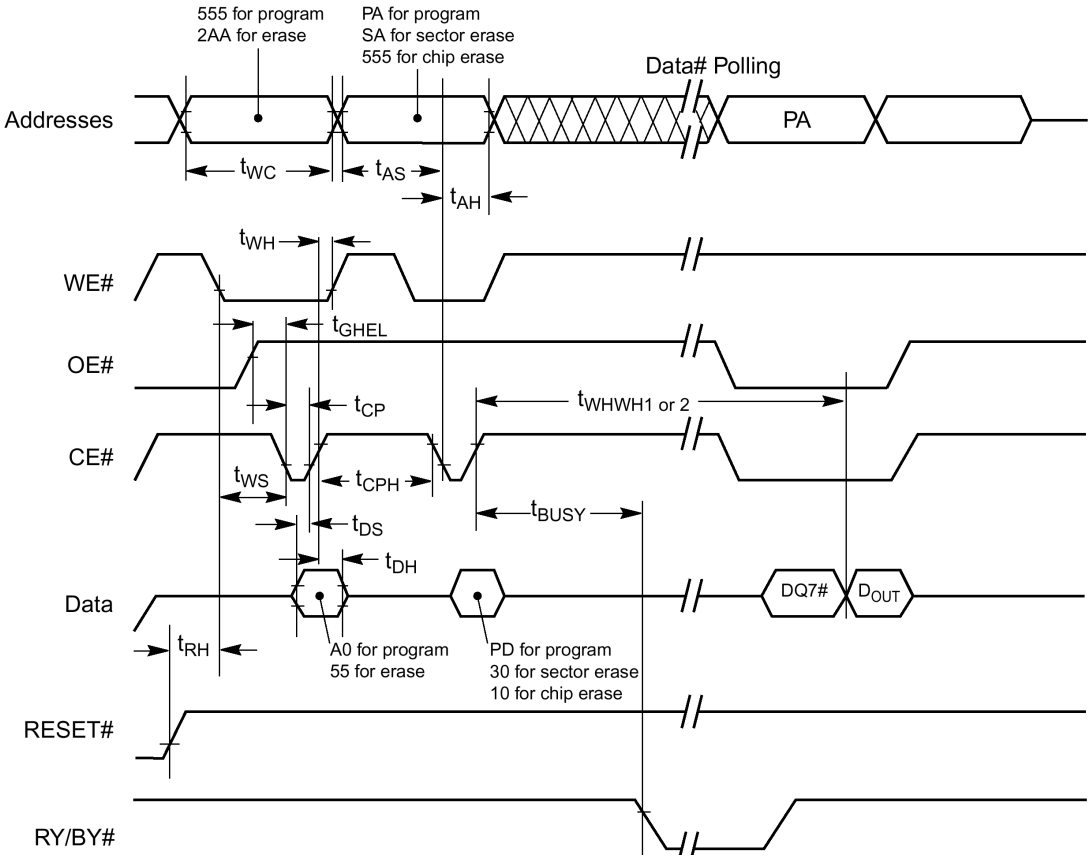
u TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



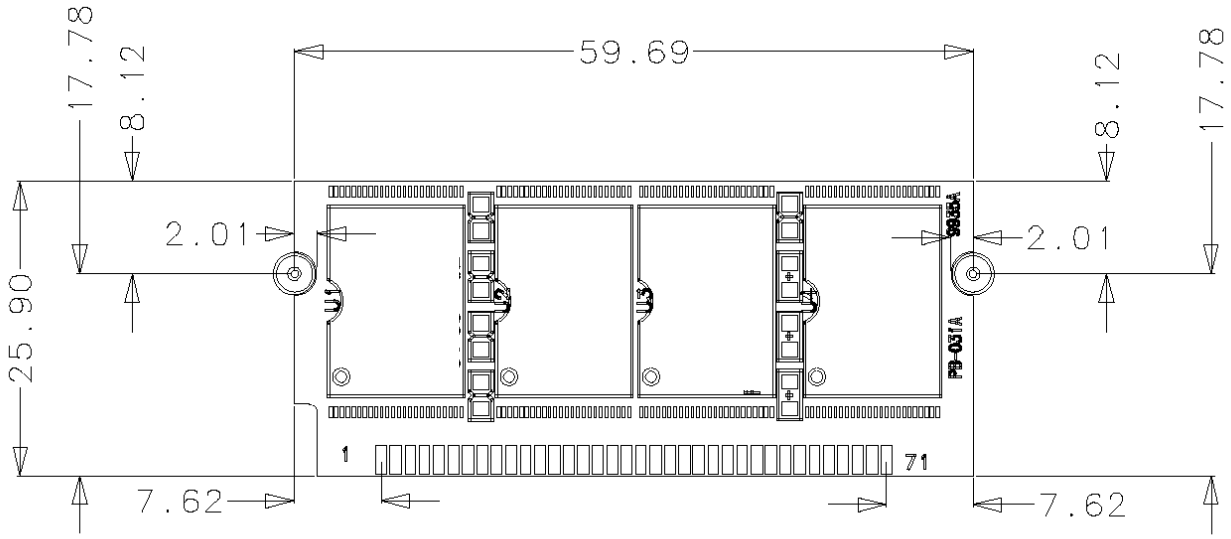
u SECTOR PROTECT UNPROTECT TIMEING DIAGRAM

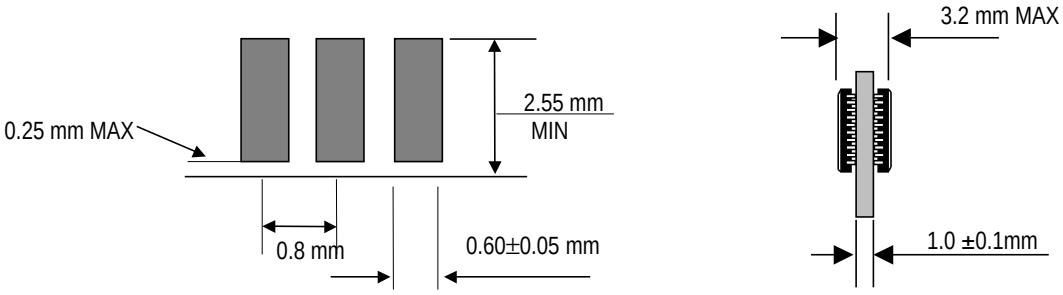


u ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS



PACKAGE DIMENSIONS





(Solder & Gold Plating)

ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	SPEED
HMF4M32B8VG-80	16MByte	x 32	72 Pin-SODIMM	8EA	3.3V	80ns
HMF4M32B8VG-90	16MByte	x 32	72 Pin-SODIMM	8EA	3.3V	90ns
HMF4M32B8VG-120	16MByte	x 32	72 Pin-SODIMM	8EA	3.3V	120ns