64Mbyte (16Mx36) FP/with Parity Mode 4K Ref. 72pin-SIMM Design

Part No. HMD16M36M12G

GENERAL DESCRIPTION

The HMD16M36M12G is a 16M x 36bit dynamic RAM high-density memory module. The module consists of eight CMOS 16M x 4bit DRAMs in 32-pin SOJ or TSOP packages and four CMOS 16Mx1bit DRAMs in SOJ or TSOP packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM components. The module is a Single In-line Memory Module with edge connections and is intended for mounting in to 72-pin edge connector sockets. All module components may be powered from a single 5V DC power supply and all inputs and outputs are TTL-compatible.

FEATURES

- Part Identification
  HMD16M36M12G
  ---4K Cycles/64ms Ref, Gold
- Access times : 50, 60ns
- High-density 64MByte design
- Single + 5V ±0.5V power supply
- JEDEC standard Pdpin & pinout
- TTL compatible inputs and outputs
- /CAS-before-/RAS & Hidden Refresh capability
- /RAS-only refresh capability
- Fast Page Mode Operation

OPTIONS MARKING

- Timing
  - 50ns access -5
  - 60ns access -6
- Packages
  - 72-pin SIMM M

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}
5	50ns	13ns	90ns
6	60ns	15ns	110ns

PRESENCE DETECT PINS(Optional)

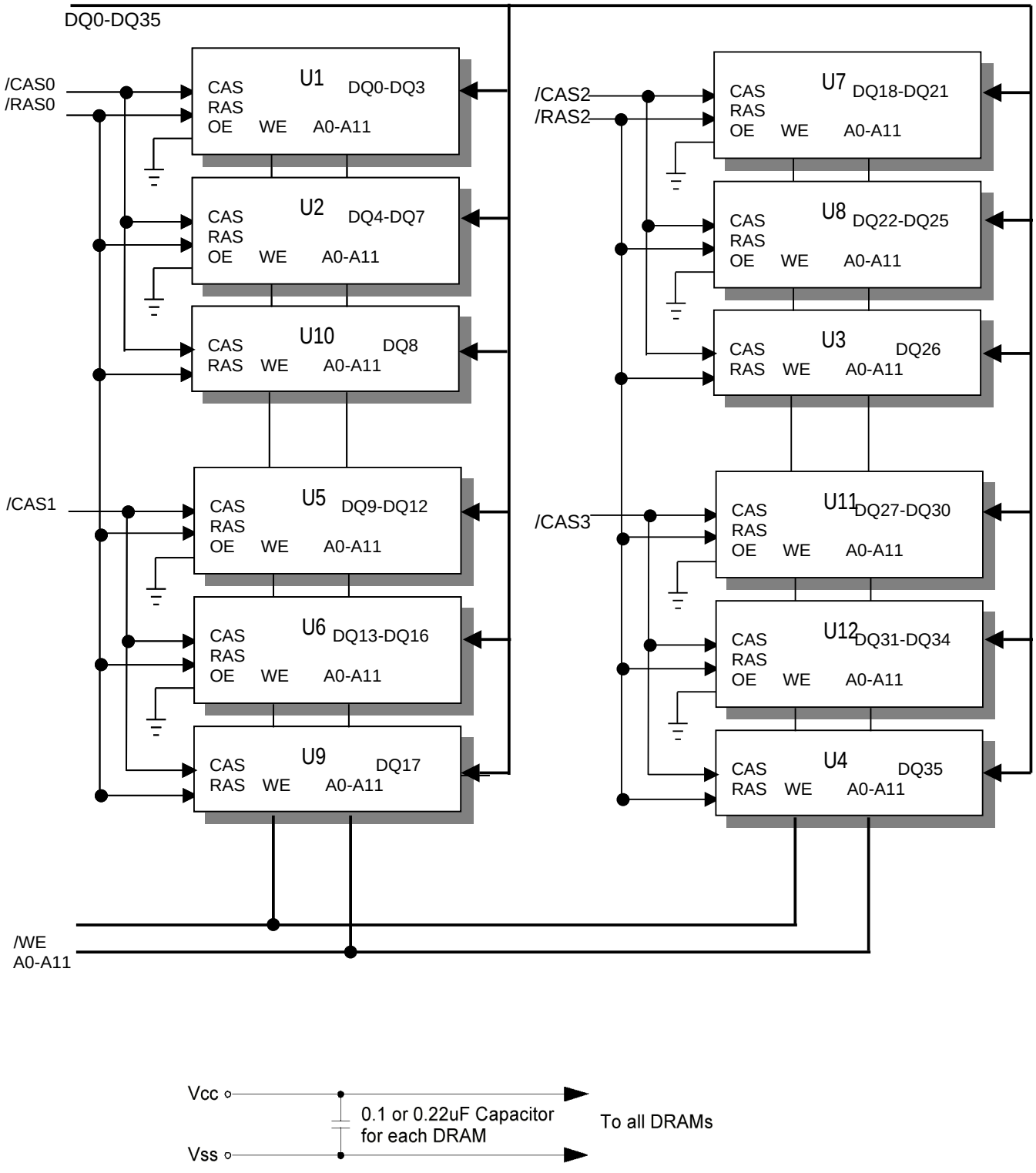
Pin	50ns	60ns
PD1	Vss	Vss
PD2	NC	NC
PD3	Vss	NC
PD4	Vss	NC

PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	25	DQ24	49	DQ9
2	DQ0	26	DQ7	50	DQ27
3	DQ18	27	DQ25	51	DQ10
4	DQ1	28	A7	52	DQ28
5	DQ19	29	A11	53	DQ11
6	DQ2	30	Vcc	54	DQ29
7	DQ20	31	A8	55	DQ12
8	DQ3	32	A9	56	DQ30
9	DQ21	33	NC	57	DQ13
10	Vcc	34	/RAS2	58	DQ31
11	NC	35	DQ26	59	Vcc
12	A0	36	DQ8	60	DQ32
13	A1	37	DQ17	61	DQ14
14	A2	38	DQ35	62	DQ33
15	A3	39	Vss	63	DQ15
16	A4	40	/CAS0	64	DQ34
17	A5	41	/CAS2	65	DQ16
18	A6	42	/CAS3	66	NC
19	A10	43	/CAS1	67	PD1
20	DQ4	44	/RAS0	68	PD2
21	DQ22	45	NC	69	PD3
22	DQ5	46	NC	70	PD4
23	DQ23	47	/WE	71	NC
24	DQ6	48	NC	72	Vss

72PIN SIMM TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-1V to 7.0V
Voltage on Vcc Supply Relative to Vss	Vcc	-1V to 7.0V
Power Dissipation	P_D	12W
Storage Temperature	T_{STG}	-55°C to 125°C
Short Circuit Output Current	I_{OS}	50mA

w Permanent device damage may occur if " Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0 to 70 °C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS

SYMBOL	SPEED	MIN	MAX	UNITS
I_{CC1}	-5	-	1080	mA
	-6	-	960	mA
I_{CC2}	Don't care	-	24	mA
I_{CC3}	-5	-	1080	mA
	-6	-	960	mA
I_{CC4}	-5	-	840	mA
	-6	-	600	mA
I_{CC5}	Don't care	-	12	mA
I_{CC6}	-5	-	1080	mA
	-6	-	960	mA
$I_{I(L)}$	Don't care	-10	10	µA
$I_{O(L)}$		-5	5	µA
V_{OH}		2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * (/RAS , /CAS , Address cycling @t_{RC}=min.)

I_{CC2} : Standby Current (/RAS=/CAS=V_{IH})

I_{CC3} : /RAS Only Refresh Current * (/CAS=V_{IH}, /RAS, Address cycling @t_{RC}=min)

I_{CC4} : Fast Page Mode Current * (/RAS=V_{IL}, /CAS, Address cycling @t_{PC}=min)

I_{CC5} : Standby Current (/RAS=/CAS=Vcc-0.2V)

I_{CC6} : /CAS-Before-/RAS Refresh Current * (/RAS and /CAS cycling @t_{RC}=min)

I_{IL} : Input Leakage Current (Any input 0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)

I_{OL} : Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V

V_{OH} : Output High Voltage Level (I_{OH}= -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE**: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address cad be changed maximum once while /RAS=V_{IL}. In I_{CC4}, address can be changed maximum once within one page mode cycle.

CAPACITANCE (T_A=25°C, Vcc = 5V, f = 1Mz)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Input Capacitance (A0-A11)	C_{IN1}	-	50	pF
Input Capacitance (/W)	C_{IN2}	-	66	pF
Input Capacitance (/RAS0)	C_{IN3}	-	38	pF
Input Capacitance (/CAS0-/CAS3)	C_{IN4}	-	24	pF
Input/Output Capacitance (DQ0-31)	C_{DQ1}	-	17	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C , Vcc = 5V±10%, See notes 1,2.)

PARAMETER	SYMBOL	-5		-6		UNIT
		MIN	MAX	MIN	MAX	
Random read or write cycle time	t_{RC}	84		104		ns
Access time from /RAS	t_{RAC}		50		60	ns
Access time from /CAS	t_{CAC}		13		15	ns
Access time from column address	t_{AA}		25		30	ns
/CAS to output in Low-Z	t_{CLZ}	3		3		ns
Output buffer turn-off delay	t_{OFF}	3	13	3	15	ns
Transition time (rise and fall)	t_T	1	50	1	50	ns
/RAS precharge time	t_{RP}	30		40		ns
/RAS pulse width	t_{RAS}	50	10K	60	10K	ns
/RAS hold time	t_{RSH}	13		15		ns
/CAS hold time	t_{CSH}	38		45		ns
/CAS pulse width	t_{CAS}	8	10K	10	10K	ns
/RAS to /CAS delay time	t_{RCD}	20	37	20	45	ns
/RAS to column address delay time	t_{RAD}	15	25	15	30	ns

/CAS to /RAS precharge time	t_{CRP}	5		5		ns
Row address set-up time	t_{ASR}	0		0		ns
Row address hold time	t_{RAH}	10		10		ns
Column address set-up time	t_{ASC}	0		0		ns
Column address hold time	t_{CAH}	8		10		ns
Column address hold referenced to /RAS	t_{AR}	50		55		ns
Column Address to /RAS lead time	t_{RAL}	25		30		ns
Read command set-up time	t_{RCS}	0		0		ns
Read command hold referenced to /CAS	t_{RCH}	0		0		ns
Read command hold referenced to /RAS	t_{RRH}	0		0		ns
Write command hold time	t_{WCH}	10		10		ns
Write command hold referenced to /RAS	t_{WCR}	50		55		ns
Write command pulse width	t_{WP}	10		10		ns
Write command to /RAS lead time	t_{RWL}	13		10		ns
Write command to /CAS lead time	t_{CWL}	8		10		ns
Data-in set-up time	t_{DS}	0		0		ns
Data-in hold time	t_{DH}	8		10		ns
Data-in hold referenced to /RAS	t_{DHR}	50		55		ns
Refresh period	t_{REF}		64		64	ns
Write command set-up time	t_{WCS}	0		0		ns
/CAS setup time (C-B-R refresh)	t_{CSR}	5		5		ns
/CAS hold time (C-B-R refresh)	t_{CHR}	10		10		ns
/RAS precharge to /CAS hold time	t_{RPC}	5		5		ns
Access time from /CAS precharge	t_{CPA}		28		35	ns
Fast page mode cycle time	t_{PC}	40		45		ns
/CAS precharge time (Fast page)	t_{CP}	8		10		ns
/RAS pulse width (Fast page)	t_{RASP}	50	200K	60	200K	ns
/W to /RAS precharge time(C-B-R refresh)	t_{WRP}	10		10		ns
/W to /RAS hold time (C-B-R refresh)	t_{WRH}	10		10		ns
/CAS precharge(C-B-R counter test)	t_{CPT}	20		30		ns

NOTES

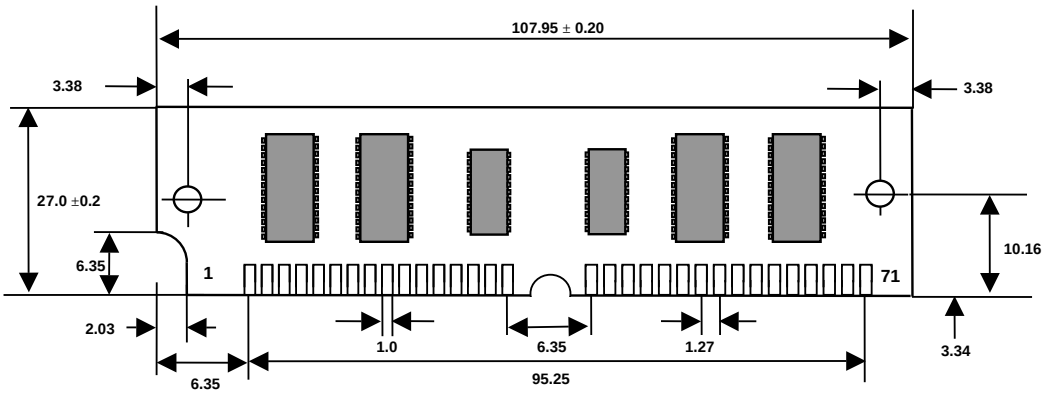
1. An initial pause of 200μs is required after power-up followed by any 8 /RAS-only or /CAS-before-/RAS refresh cycles before proper device operation is achieved.
2. $V_{IH\ (min)}$ and $V_{IL\ (max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$

6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} anf t_{AWD} are non restrictive operating parameter.
   They are included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the /CAS leading edge in early write cycles and to the /W leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit. then access time is controlled by t_{AA}.

PACKAGING INFORMATION

SIMM Design

Unit : mm



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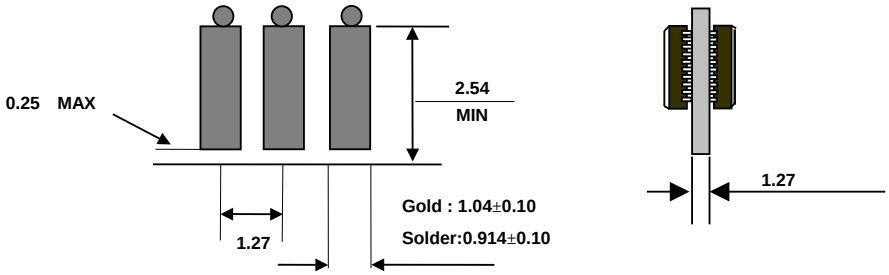

ORDERING INFORMATION

Part Number	Density	Org.	Package	Ref.	Vcc	MODE	SPEED
HMD16M36M12G-5	64MByte	x 36	72 Pin-SIMM-Gold	4K	5V	FPM / Parity	50ns
HMD16M36M12G-6	64MByte	x 36	72 Pin-SIMM-Gold	4K	5V	FPM / Parity	60ns